THE LEADER IN...

TECHNOLOGY

PERFORMANCE

AND INNOVATION

GOULD Electronics

Gould Inc.

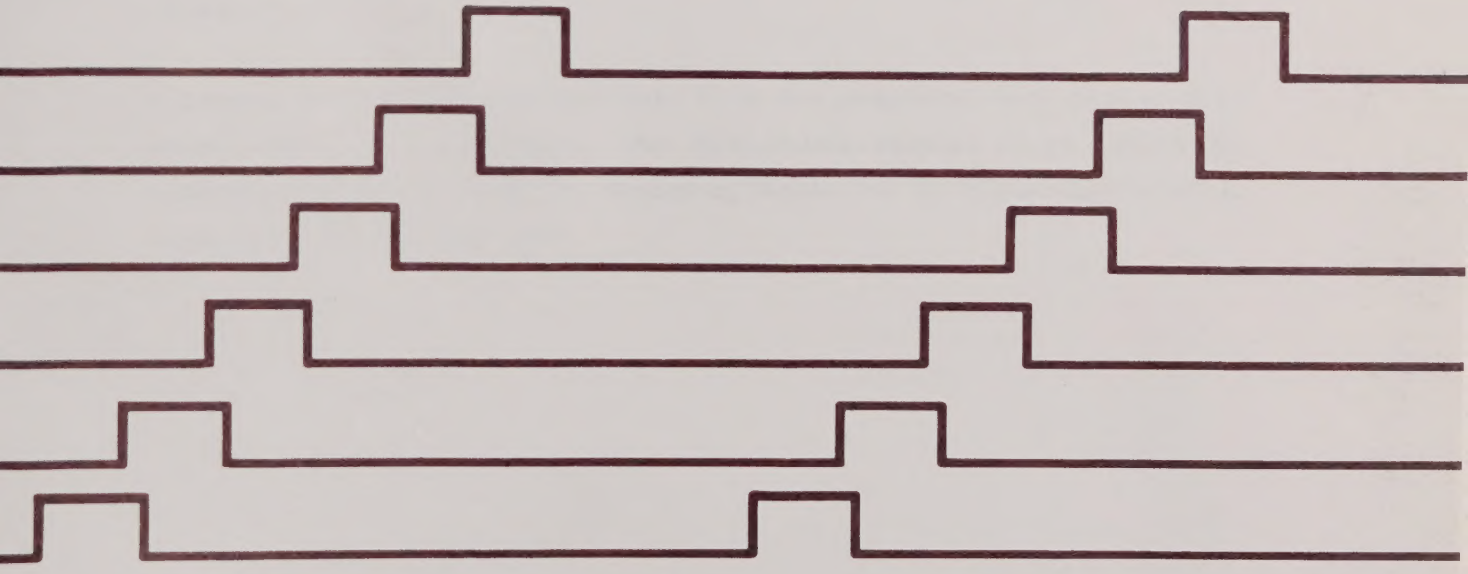
Design & Test Systems Division

Part Number: 0114-0100-10

January 1983
Revision 1.0

Gould Biomation K101-D Logic Analyzer

Operating Manual



GOULD

Electronics & Electrical Products

PREFACE

Congratulations on purchasing the Gould Biomation K101-D Logic Analyzer. Your new instrument is a high-performance, state-of-the-art tool, optimized to help you solve digital system problems quickly and easily.

This **Operating Manual** contains instructional and reference material on the K101-D. Section 1, the General Introduction, describes the information in this manual and explains the organization.

The **Operating Manual** is meant to be the single reference necessary for use of the K101-D logic analyzer. It gives detailed operating and specification information. Tab dividers and special sections are provided for the insertion of related literature and new information.

A related publication, the **Gould Biomation K101-D/K102-D Logic Analyzers Users Training Guide,** presents an instructional course on the K101-D and a related logic analyzer, the K102-D. The **Training Guide** has more extensive concepts and examples. Its material includes step by step procedures.

Although the two manuals overlap, they are complementary rather than substitutes for each other. The **Operating Manual** is an essential companion to the K101-D; the **Training Guide** can be exceedingly useful, especially for the new user.

TABLE OF CONTENTS

FOR K101-D MANUAL

Section			Page
PREFACE			i
1	**GENERAL INFORMATION**		1-1
	1.1	Introduction	1-1
	1.2	General Description	1-2
		1.2.1 Information Flow	1-2
		1.2.2 Applications for the K101-D	1-5
	1.3	Overview of the Manual	1-7
2	**PRINCIPLES OF LOGIC ANALYSIS**		2-1
	2.1	Overview	2-1
	2.2	Capabilities and Tools of the K101-D	2-4
		2.2.1 Specifying the Recording Process	2-4
		2.2.2 Recording Using the Specifications	2-8
		2.2.3 Reviewing and Analyzing the Results	2-9
		2.2.4 Default Capability	2-13
		2.2.5 Summary	2-13
	2.3	Building Blocks	2-14
	2.4	General Approach to Using the K101-D	2-14
		2.4.1 Probes	2-15
		2.4.2 Polarity and Threshold	2-15
		2.4.3 Data Format	2-16
		2.4.4 Clocking of Inputs	2-17
		2.4.5 Tracing and Acquisition	2-17
		2.4.6 Making the Recording	2-19
		2.4.7 Displaying and Analyzing the Data	2-19
	2.5	Communication Interface	2-20
	2.6	Collect -> Reduce -> Organize	2-22
		2.6.1 The Collect/Reduce/Organize Matrix	2-22
		2.6.2 Physical Setup	2-24
		2.6.3 Specify Recording Parameters	2-25
		2.6.4 Make a Recording or Recordings	2-26
		2.6.5 Recording Analysis	2-26
		2.6.6 End Result	2-27
	2.7	A Final Word	2-27

TABLE OF CONTENTS (Cont'd)

Section			Page
3	**DETAILED DESCRIPTION**		3-1
	3.1	Introduction	3-1
	3.2	Detailed Description	3-1
	3.3	Specifications	3-4
		3.3.1 Signal Inputs	3-4
		3.3.2 Clocking Selection	3-7
		3.3.3 Trace Memory	3-16
		3.3.4 Data Formats	3-17
		3.3.5 Trace Control	3-17
		3.3.6 Arm Modes	3-20
		3.3.7 Displays	3-21
		3.3.8 Auxiliary Measurements	3-23
		3.3.9 Interfaces/Rear Panel Connectors	3-25
		3.3.10 Confidence Tests	3-25
		3.3.11 Accessories Supplied	3-26
		3.3.12 Miscellaneous	3-26
4	**USER CONTROLS AND DISPLAYS**		4-1
	4.1	Overview and Strategy	4-1
	4.2	Brief Description of Keyboard and Front Panel Inputs	4-2
		4.2.1 Probe Connectors	4-2
		4.2.2 CRT Display Screen	4-2
		4.2.3 Power, DVM, and Probe Test	4-2
		4.2.4 Keyboard	4-2
		4.2.5 Power Check	4-5
	4.3	Power Up	4-5
	4.4	Using the Keyboard	4-6
		4.4.1 FIELD Keys	4-6
		4.4.2 SPECIFY Keys	4-6
		4.4.3 ACQUIRE Keys	4-7
		4.4.4 DISPLAY Keys	4-7
		4.4.5 GPIB Keys	4-7
		4.4.6 GENERAL Keys	4-7
	4.5	Keyboard Detailed Description	4-8
		4.5.1 FIELD Key Area	4-8
		4.5.2 SPECIFY Key Area	4-11
		4.5.3 ACQUIRE Keys	4-19

Section			Page
		4.5.4 DISPLAY Keys	4-20
		4.5.5 GENERAL Keys	4-23
		4.5.6 GPIB Keys	4-38
	4.6	Displays	4-38
		4.6.1 Overview	4-38
		4.6.2 Default Displays	4-50
		4.6.3 Status Information	4-51
		4.6.4 Display Formatting and Measurement Features	4-53
5	**SPECIFYING RECORDING PARAMETERS**		5-1
	5.1	Overview and Strategy	5-1
		5.1.1 Data Flow	5-1
		5.1.2 Ending the Recording Cycle	5-2
		5.1.3 Organization of Section 5	5-2
	5.2	Probe Connection	5-2
		5.2.1 Input Signals and Data Format	5-3
		5.2.2 Order of Connection	5-3
		5.2.3 Physical Connection	5-3
	5.3	Specification Categories	5-5
	5.4	Logic Polarity	5-5
	5.5	Input Mode Screen	5-7
		5.5.1 Input Mode Selection	5-7
		5.5.2 Threshold Level Selection	5-16
		5.5.3 Arm Mode Selection	5-16
	5.6	Clock Select Screens	5-18
		5.6.1 General Description	5-18
		5.6.2 Clocking Mode Overview	5-19
		5.6.3 Enable Clocks	5-22
		5.6.4 Internal Mode	5-24
		5.6.5 External Single-Phase Mode	5-26
		5.6.6 External Multiphase Mode	5-28
		5.6.7 Mixed Single-Phase Mode	5-28
		5.6.8 Mixed Multiphase Mode	5-32
		5.6.9 Internal Extended Mode	5-32
	5.7	Data Format Screens	5-35
		5.7.1 Fixed Formats	5-36
		5.7.2 Mixed Radices, Fixed Sequence	5-36

TABLE OF CONTENTS (Cont'd)

Section			Page
		5.7.3 Mixed Radices, User-Defined Sequence	5-39
		5.7.4 Device Mnemonics	5-41
	5.8	Trace Control Screens	5-43
		5.8.1 Types of Trace Control	5-44
		5.8.2 General Approach to Trace Control	5-48
	5.9	Interface	5-48
6	**MAKING A RECORDING**		6-1
	6.1	Overview and Strategy	6-1
		6.1.1 Arming Specifications	6-1
		6.1.2 Manual Control	6-2
		6.1.3 Monitoring the Recording Process	6-2
	6.2	Arming Choices	6-3
		6.2.1 Manual Arm Mode	6-3
		6.2.2 Auto Arm Mode	6-3
		6.2.3 Auto Stop by Compare Arm Mode	6-6
	6.3	Manual Control	6-8
		6.3.1 Advance	6-8
		6.3.2 Manual Stops	6-9
7	**RECORDING ANALYSIS**		7-1
	7.1	Overview and Strategy	7-1
	7.2	Overview of Keys	7-2
		7.2.1 Display Keys	7-2
		7.2.2 The Edit Keys	7-5
		7.2.3 Display Manipulation	7-5
		7.2.4 Cursor Keys	7-5
	7.3	Display Formats	7-5
	7.4	Data Display	7-6
		7.4.1 Data Searches	7-6
		7.4.2 Memory Comparison	7-7
		7.4.3 Reference Editing	7-7
	7.5	Graph Display	7-11
		7.5.1 Selecting Vertical Display Limits	7-13
		7.5.2 Horizontal Display Expansion	7-13
	7.6	Timing Display	7-14
		7.6.1 Vertical Display Expansion and Paging	7-14

TABLE OF CONTENTS (Cont'd)

Section			Page
		7.6.2 Horizontal Display Expansion	7-14
		7.6.3 Modifying the Timing Display	7-15
		7.6.4 Labelling Timing Displays	7-15
	7.7	Auxiliary Measurements	7-15
		7.7.1 DVM (Digital Voltmeter)	7-15
		7.7.2 Frequency Counter	7-18
		7.7.3 Date and Time	7-18
		7.7.4 Total Trace Time	7-18
		7.7.5 Trace Level Tracking	7-19
	7.8	Use of these Techniques	7-21
		7.8.1 The Iterative Approach	7-21
		7.8.2 Use of Search and Compare	7-21
		7.8.3 Use of Automatic Arm Mode	7-22
	7.9	Summary	7-22
8	**APPLICATIONS**		8-1
	8.1	General	8-1
	8.2	Clocking	8-1
		8.2.1 Timing Analysis	8-1
		8.2.2 State Analysis	8-7
		8.2.3 Combined State and Timing Analysis: Mixed Single-/Multi-Phase	8-21
		8.2.4 Time Relationship	8-22
	8.3	Trace Control	8-27
		8.3.1 Introduction	8-27
		8.3.2 Basic Building Blocks	8-27
		8.3.3 Advanced Applications	8-29
9	**COMMUNICATIONS**		9-1
	9.1	Overview	9-1
	9.2	Operation	9-2
		9.2.1 GPIB Interface Operation	9-2
		9.2.2 RS-232-C Interface Operation	9-8
	9.3	Codes and Commands	9-11
		9.3.1 Description	9-11
		9.3.2 Keystroke Record	9-13
		9.3.3 Command Records	9-24

TABLE OF CONTENTS (Cont'd)

Section			Page
	9.3.4	Memory Modification Records	9-36
	9.3.5	Display Message Record	9-39
	9.3.6	Status Record	9-40
9.4	Using a Printer with the K101-D		9-44
	9.4.1	Printer Terminal with a Keyboard	9-44
	9.4.2	Printing by Using the K101-D Keyboard	9-44
	9.4.3	Summary -- Use of GPIB Interface and Printer	9-44
	9.4.4	Summary -- Use of RS-232-C Interface and Printer	9-45
9.5	General Purpose Interface Bus (GPIB)		9-47
	9.5.1	Description	9-47
	9.5.2	GPIB Interface Connection	9-47
	9.5.3	GPIB Interface Messages	9-47
	9.5.4	GPIB Status Information Parallel Poll	9-49
	9.5.5	GPIB Status Information Serial Poll	9-51
	9.5.6	GPIB Status Byte	9-51
	9.5.7	GPIB References	9-53
9.6	The RS-232-C Interface		9-54
	9.6.1	Protocols	9-54
	9.6.2	RS-232-C Interface Connection	9-55
	9.6.3	RS-232 References	9-56
10	**MEASUREMENT CONFIDENCE**		10-1
10.1	Introduction		10-1
10.2	Probe Test		10-2
	10.2.1	Probe Connection	10-2
	10.2.2	Polarity and Threshold	10-5
	10.2.3	Data Format	10-13
	10.2.4	Clock and Input	10-26
	10.2.5	Trace Control	10-72
	10.2.6	Advanced Trace Control	10-126
	10.2.7	Record	10-139
10.3	Power Up Test		10-157
	10.3.1	K101-D ROM Test	10-157
	10.3.2	K101-D RAM Test	10-157
	10.3.3	Power Supply Test	10-160
	10.3.4	CMOS RAM Test	10-160

TABLE OF CONTENTS (Cont'd)

Section		Page
	10.3.5 USART Errors	10-161
	10.3.6 Keyboard Test	10-161
10.4	Self Test	10-161
	10.4.1 Confidence Test	10-164
	10.4.2 K101-D MPU RAM/ROM	10-164
	10.4.3 Data Boards	10-165
	10.4.4 Voltage Test	10-171
	10.4.5 Clock	10-171
	10.4.6 Trace Control	10-174
	10.4.7 Keyboard	10-177
	10.4.8 CRT Alignment	10-177
	10.4.9 Parameters	10-179
11	**RELATED LITERATURE**	11-1
12	**REFERENCE MATERIAL**	12-1
13	**GLOSSARY**	13-1
14	**INPUT CONNECTION GUIDE AND SETUP GUIDE**	14-1
14.1	Introduction	14-1
14.2	Input Connection Guides	14-2
	14.2.1 SN74L192 Decade Counter	14-2
	14.2.2 8085A Microprocessor	14-4
14.3	Set Up Guides	14-4
	14.3.1 Default Menu	14-11
	14.3.2 SN74L102 Setup	14-11
	14.3.3 8085A Setup	14-16
14.4	Suggested Connection for Popular Microprocessors	14-21
15	**INDEX**	
16	**ACCESSORIES**	16-1

ILLUSTRATIONS

Figure		Page
1-1	Flow of Information and Control in the K101-D Logic Analyzer	1-3
1-2	Using the K101-D During System Design and Production	1-6
2-1	Basic Process for Using the K101-D Logic Analyzer	2-2
2-2	Iterative Approach to Problem Solving	2-3
2-3	Combinational Binary Specification of Inputs	2-6
2-4	Data Display	2-11
2-5	Timing Diagram Display	2-12
2-6	Graphic Display	2-12
2-7	Screen Display of Status Information	2-21
2-8	Mnemonic Disassembly Display	2-21
2-9	The Collect, Reduce, and Organize Matrix	2-23
3-1	T_1: Time from Active Edge on One Input to Active Edge on Other Input	3-11
3-2	T_2: Time From Active Edge on One Input to Nonactive Edge on Other Input	3-11
3-3	T_3: Time From Nonactive Edge on One Input to Active Edge on Other Input	3-11
3-4	XK↑ + YK↑	3-12
3-5	XK↑ + YK↓	3-12
3-6	XK↓ + YK↑	3-13
3-7	XK↓ + YK|	3-13
3-8	XJ↑ · YJ↑	3-13
3-9	XJ↑ · YJ|	3-14
3-10	XJ| · YJ↑	3-14
3-11	XJ| · YJ↓	3-14
3-12	Master and Sample Skew Requirements	3-15
4-1	K101-D Front Panel	4-3
4-2	K101-D Keyboard	4-4
4-3	GENERAL Area Keys	4-24
4-4	Numeric Data and QUICK Keys	4-26
4-5	Hexadecimal Keys	4-27
4-6	ASCII Keys	4-28
4-7	Input Mode Keys	4-30
4-8	Trace Control Keys	4-31
4-9	Logic Polarity Keys	4-32

ILLUSTRATIONS (Cont'd)

Figure		Page
4-10	Data Format Keys	4-33
4-11	Edit Keys	4-34
4-12	Data Entry Keys	4-35
4-13	Graph Keys	4-36
4-14	Timing Data Entry Keys	4-37
4-15	Types of Displays on the K101-D	4-39
4-16	Clock Select Default Display	4-40
4-17	Input Mode Default Display	4-41
4-18	Trace Control Default Display	4-42
4-19	Logic Polarity Default Display	4-43
4-20	Data Format Default Display	4-44
4-21	Graph Default Display	4-45
4-22	Timing Default Display	4-46
4-23	Data Default Display	4-47
4-24	Interface Default Display	4-48
4-25	Compare A/B Display	4-52
4-26	Typical Timing Data Page -- Six Lines	4-54
4-27	User Defined Timing Input	4-54
4-28	Horizontal Expansion	4-55
4-29	Data Display Cursor Location	4-58
4-30	Equal Compare of Memories A and B	4-58
4-31	Search Pattern with "Semi-Care"	4-60
4-32	Search Result Status	4-60
4-33	Editing Memory B	4-62
4-34	Inserting a Word in Memory B	4-62
4-35	Deleting a Word	4-64
4-36	Message Displayed During Graph Point Calculations	4-64
4-37	Two Full Cycles of Six 8-bit Binary Counters	4-67
4-38	The Data Format Used for Figures 4-39 and 4-40	4-67
4-39	Graph of Two Full 8-bit Binary Counter Cycles	4-68
4-40	Expanding the Display	4-68
5-1	Input Connection Guide	5-4
5-2	Logic Polarity Assignment	5-6
5-3	The Input Mode Screen Parameters	5-8
5-4	Temporary Sample Registers	5-11
5-5	Glitch Mode Used for Noise Spikes	5-11
5-6	Typical Glitch Pattern	5-13

ILLUSTRATIONS (Cont'd)

Figure		Page
5-7	Latch Register Holds Event for Sampling (Latch Mode)	5-13
5-8	Diagram of Demultiplex Logic	5-15
5-9	Setting Threshold Levels and Arm Modes	5-17
5-10	Enable Clocks	5-23
5-11	Diagram of Enable Clocking in Latch or Demux Mode	5-25
5-12	Internal Mode Clock Select Screen	5-25
5-13	Illegal Clock Display	5-27
5-14	Master Clock Expression	5-27
5-15	External Multiphase Mode Clock Select Screen	5-29
5-16	Mixed Single-Phase Mode Clock Select Screen	5-29
5-17	Example of Skew Accumulation from Mixed Mode Clocking	5-31
5-18	Mixed Multiphase Mode Clock Select Screen	5-31
5-19	Internal Extended Mode Clock Select Screen	5-33
5-20	Fixed Hexadecimal Display	5-37
5-21	Fixed Octal Display	5-37
5-22	Fixed Binary Display	5-38
5-23	Mixed Format, Fixed Sequence Data Format Screen	5-38
5-24	Mixed Format, User Sequence Data Format Screen	5-40
5-25	Device Mnemonics Display	5-42
5-26	"Device Not Available" Message	5-42
5-27	Trace Control Parameter Specification	5-45
5-28	Trace Control Form	5-50
6-1	Input Mode Screen	6-5
7-1	Data Display	7-3
7-2	Graph Display	7-3
7-3	Timing Display	7-4
7-4	Data Searches	7-8
7-5	Search Tabulation	7-9
7-6	Memory Comparison	7-9
7-7	Reference Editing	7-10
7-8	Insert	7-12
7-9	Delete	7-12
7-10	Trace Sequence Modification	7-16
7-11	Trace Label Assignment	7-16
7-12	Auxiliary Measurements	7-17
8-1	Typical Timing Analysis Measurements	8-3
8-2	Shortest Time Limit	8-3

Figure		Page
8-3	Appropriate Sampling Frequency	8-5
8-4	Missed Pulses Due to Low Sampling Frequency	8-5
8-5	Sampling at More Than 2X Input Frequency	8-6
8-6	Window Versus Sampling Frequency	8-6
8-7	Typical Setup	8-8
8-8	Typical Timing Display	8-9
8-9	Trailing Edge Detection	8-12
8-10	Alternate to Trailing Edge Detection	8-12
8-11	Boolean Expressions	8-14
8-12	Basic Clock Building Blocks	8-14
8-13	X↑ = Y↑	8-16
8-14	X↑ + Y↓	8-16
8-15	X↓ + Y↑	8-17
8-16	X↓ + Y↓	8-17
8-17	X↑ · Y↑	8-19
8-18	X↑ · Y↓	8-19
8-19	X↓ · Y↑	8-20
8-20	X↓ · Y↓	8-20
8-21	Sample Location	8-25
8-22	Time Alignment of Section Inputs as Sampled in Figure 8-21	8-25
8-23	Data Format Used to Make the Following Data Display	8-26
8-24	The Time-Aligned Section A, B, and C Words (10) in Location P-1 (513)	8-26
8-25	Fill Memory with Samples from Anywhere in Data Stream	8-30
8-26	Wait for a Specific Event to Occur, Then Record (Four Cases)	8-31
8-27	Record What Happens Immediately After an Event (Case A)	8-32
8-28	Record What Happens Immediately Before an Event (Case B)	8-33
8-29	Record What Happens Around an Event (Case C)	8-34
8-30	Record What Happens Long After an Event (Case D)	8-35
8-31	Capture a Segment of Samples; Record from Here to There	8-36
8-32	Exclude Recording a Segment of Samples; Don't Record from Here to There	8-37
8-33	Selectively Record Only One Kind of Sample (Two Cases)	8-38
8-34	Follow a Path, Then Record	8-39
8-35	Record, then Follow a Path	8-40

ILLUSTRATIONS (Cont'd)

Figure		Page
8-36	Check for Event 1 or Event 2 and Take a Different Path Depending on Which Event Occurred	8-41
8-37	Check for Event 1 or Event 2 and Take the Same Path Regardless of Which Event Occurred	8-42
8-38	Check for Correct Timing Between Two Events	8-43
8-39	Continuously Monitor for Correct Operation	8-44
8-40	Check for Correct Pulse Width or Skew	8-46
8-41	Record a Nested Subroutine	8-48
8-42	Capture Multiple Subroutines	8-50
8-43	Record Main Program Only	8-54
8-44	Check for Unknown Errors in Real Time	8-56
8-45	Record and Check for Correct Execution	8-59
8-46	Isolate Program Execution Essentials	8-60
9-1	GPIB Interface Setup Menu	9-3
9-2	RS-232-C Interface Setup Menu	9-9
9-3	The K101-D Records	9-12
9-4	Record Formats	9-26
9-5	Memory Modification Records	9-37
9-6a	The Message Record Format	9-39
9-6b	Status Record Format	9-41
9-7	PPR States	9-50
9-8	Null Modem Wiring Diagrams	9-57
9-9	Complete Null Modem	9-58
10-1	Resulting Probe Test Recording Using a TTL Threshold	10-5
10-2	Typical Probe Test Recording Using an ECL Threshold	10-6
10-3	Fixed Location Pattern	10-8
10-4	Pattern Changes with Threshold Changes	10-10
10-5	Effect of Rise and Fall Time	10-10
10-6	Information Flow	10-12
10-7	Setup	10-14
10-8	Clock Select for Delete Example	10-16
10-9	Trace Control for Delete Example	10-16
10-10	Data Display, Probe Inputs AF Through A8	10-18
10-11	Graph of Data of Figure 10-10	10-18
10-12	Data Format/Word Recognizer Changes	10-20
10-13	New Data Display for Figure 10-12 Data Format	10-20
10-14	Change of Input Channel Graphed	10-20

ILLUSTRATIONS (Cont'd)

Figure		Page
10-15	AF Through A8 Displayed In Both Hex and Binary	10-23
10-16	Data Display for Figure 10-15	10-23
10-17	Fixed Binary Format, All Inputs CF Through A0	10-21
10-18	Graph First 14 Columns as Fixed Binary Data	10-25
10-19	Time Relationship of Clock and Data Signals	10-26
10-20	Set Up Internal Sampling	10-28
10-21	Clock Select for Sample Internally	10-30
10-22	Data Format for Sample Internally	10-30
10-23	Pattern Asynchronously Sampled Every 100 ns	10-31
10-24	Sample Clock = AJ↑	10-32
10-25	Setup Sample, Single External Clock	10-33
10-26	Clock Select for AJ↑	10-36
10-27	Recording for Sample Clock = AJ↑ or AJ↓	10-36
10-28	Setup Guide Sample on Pair of External CLocks	10-38
10-29	Sample Clock = AJ↓ + AK↑	10-40
10-30	Recording for Sample Clock = AJ↓ + AK↑	10-40
10-31	Sample Clock = AJ↑ + AK↓	10-41
10-32	Recording for Sample Clock = AJ↑ + AK↓	10-41
10-33	Sample Clock = AJ↓ + AK↓	10-42
10-34	Recoding for Sample Clock = AJ↓ + AK↓	10-42
10-35	Setup Latch (Enable) on a Single Input	10-44
10-36	Enable = AR↑	10-46
10-37	Clock Select for Enable = AR↑	10-48
10-38	Input Mode for Latch on Single Input	10-48
10-39	Recording of Asynchronously Sampled Latched Inputs for Enable = AR↑	10-50
10-40	Function of Input Signal Transitions Latch Enable Signal	10-50
10-41	Recording for Enable = AR↓	10-51
10-42	Enable = AS↑ Every Other Transition Latched	10-53
10-43	Time Recording for Enable = AS↑	10-53
10-44	Enable = AS↓, Inputs Latched When AS↓ True	10-54
10-45	Recording for Enable = AS↓	10-54
10-46	Enable = AR↑ + AS↑	10-56
10-47	Recording for Enable = AR↑ + AS↑	10-56
10-48	Enable = AR↓ + AJ↑	10-58
10-49	Recording for Enable = AR↓ + AS↑	10-58
10-50	Enable = AR↑ + AS↓	10-59

ILLUSTRATIONS (Cont'd)

Figure		Page
10-51	Recording for Enable = AR↑ + AS↓	10-59
10-52	Enable = AR↓ + AS↓	10-61
10-53	Recording for Enable = AR↓ + AS↓	10-61
10-54	AF Through A8 Latched by AR↑	10-63
10-55	AF Through AS Latched by AR↓	10-65
10-56	AF Through A8 Latched by AS↑	10-65
10-57	AF Through AS Latched by AS↓	10-67
10-58	AF Through A8 Latched by AR↑ + AS↑	10-68
10-59	AF Through A8 Latched by AR↓ + AS↑	10-69
10-60	AF Through AS Latched by AR↑ + AS↓	10-70
10-61	AF Through A8 Latched by AR↓ + AS↓	10-71
10-62	Setup Guide: Fill Memory with Samples from Anywhere in Data Stream	10-73
10-63	Fill Memory From Anywhere in the Data Stream	10-76
10-64	First Level, Record Immediately After Event 01	10-78
10-65	Second Level, Record Immediately After Event 01	10-78
10-66	Event 01 Recorded by Trace Level 0	10-79
10-67	Words Recorded by Trace Level 1	10-79
10-68	First Traced Sample	10-81
10-69	Last Three Displayed Words Sampled	10-82
10-70	Event Placed at Location 246	10-84
10-71	Setup Guide: Record What Happens Around an Event	10-86
10-72	Recording of Selected Words	10-88
10-73	Setup Guide: Capture a Segment of Samples: Record from Here to There	10-90
10-74	First Word (01) Recorded by Level 0	10-93
10-75	Words of Segment Recorded by Level 1	10-93
10-76	Setup Guide: Exclude Recording a Segment of Samples: Don't Record from Here to There	10-95
10-77	Six Pulses Sampled and Not Recorded	10-97
10-78	Word 01 Selected to be Recorded	10-99
10-79	Setup Guide: Follow a Path, Then Record	10-100
10-80	Four Pulses Sequence for Recording	10-103
10-81	Trace on Four Levels Before Recording	10-103
10-82	Setup Guide: Record, Then Follow a Path	10-105
10-83	Verify Expected Execution Path	10-107
10-84	Setup Guide: Check for Event 1 or Event 2	10-109

ILLUSTRATIONS (Cont'd)

Figure		Page
10-85	Setup Guide: Take the Same Path Regardless of Which Event Occurred	10-112
10-86	Sometimes 10 Will Occur on Level 0	10-114
10-87	Sometimes 01 Will Occur on Level 0	10-114
10-88	Setup Guide: Check Correct Timing Between Two Events	10-116
10-89	Setup Guide: Continuously Monitor for Correct Operation	10-119
10-90	Tracing Halted	10-121
10-91	Setup Guide: Repeatedly Check Word 80	10-123
10-92	Time Interval Error, Tracing Stopped	10-125
10-93	Setup Guide: Continuously Check Execution Path and Timing	10-127
10-94	Capture One Word on Each Level until Stopped	10-130
10-95	Transfer Certain Samples into Memory	10-132
10-96	Changing Sample Selection	10-132
10-97	Record While Waiting	10-134
10-98	End Level 3 Forces	10-134
10-99	Setup Guide: Segments, Patterns, and Total Trace Time	10-136
10-100	Only Three Words are Traced into Memory	10-138
10-101	Setup Guide: Manual Arm	10-140
10-102	Probe Test Timing Display	10-142
10-103	Status Field Display	10-144
10-104	Completion of Auto Arming Recording Cycle	10-146
10-105	Automatic Arming Process Stopped	10-149
10-106	Asynchronous Recordings Differences	10-151
10-107	Effect of Specified Sample Rate and Trace Condition	10-151
10-108	267 Recordings Compared Before Match	10-152
10-109	Identical Recordings	10-152
10-110	Comparison Between Location 500 and 514	10-154
10-111	Inequality Outside Window	10-154
10-112	Inequality Within Window	10-156
10-113	Samples in Window Same Arming Stops	10-156
10-114	ROM Test Grid	10-159
10-115	RAM Test Grid	10-159
10-116	Power Supply Error Messages	10-162
10-117	USART Error Messages	10-162
10-118	Main Menu When First Entering Self-Test	10-163

ILLUSTRATIONS (Cont'd)

Figure		Page
10-119	MPU RAM/ROM Test Submenu	10-163
10-120	Data Board Tests Submenus	10-166
10-121	Data Board A Submenu	10-166
10-122	Typical Calibrate Display	10-172
10-123	Voltage Test Submenu	10-172
10-124	Clock Test Submenu	10-173
10-125	Trace Control Test Submenu	10-175
10-126	First Keyboard Test Display	10-178
10-127	Alignment Test Grid	10-178
10-128	Parameters Display Screen	10-180
14-1	K101-D Front Panel	14-3
14-2	Types SN54192, SN54L192, SN54LS192, SN74192, SN74L192, and SN74LS192 Synchronous 4-Bit Up/Down Counters (Dual Clock with Clear)	14-5
14-3	Decade Counter Connection Guide	14-6
14-4	8085A Pinout Diagram	14-7
14-5	8085A Connection Guide	14-8
14-6	Default Setup	14-12
14-7	"Shorthand" Version of Default Setup	14-14
14-8	Decade Counter Setup	14-17
14-9	8085A Setup Guide	14-19
14-10	8080 Family	14-22
14-11	8085 Family	14-23
14-12	NSC 800	14-24
14-13	8086	14-25
14-14	8088	14-26
14-15	Z80 Family	14-27
14-16	68000	14-28
14-17	6502	14-29
14-18	6512	14-30
14-19	6800/6802	14-31
14-20	6809	14-32

LIST OF TABLES

Table		Page
3-1	Clock Input Specifications	3-10
3-2	Setup Times for a Combination of Two Clock Inputs	3-10
4-1	GPIB Entry Possibilities	4-12
4-2	Clock Entry Possibilities	4-13
4-3	Input Mode Entry Possibilities	4-14
4-4	Trace Control Entry Possibilities	4-16
4-5	Key Groups	4-29
9-1	Keycode Selection Table (Keystroke Record Only)	9-15
9-2	DIRECT Keys and QUICK Keys (Keystroke Record Only)	9-17
9-3	Summary of K101-D Command Records	9-25
9-4	K101-D Status Byte Messages: GPIB Interface	9-42
9-5	K101-D Status Byte Messages: RS-232-C Interface	9-43
9-6	Recording Status Codes	9-43
9-7	GPIB Interface Capabilities	9-48
10-1	Probe Test Exercises	10-3
10-2	Power Up Test Error Messages	10-158
13-1	Logical Relationships of Selected K101-D Terms	13-2

WARNING: THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY, AND IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. AS TEMPORARILY PERMITTED BY REGULATION, IT HAS NOT BEEN TESTED FOR COMPLIANCE WITH THE LIMITS FOR CLASS A COMPUTING DEVICES PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE IN WHICH CASE, THE USER AT HIS OWN EXPENSE, WILL BE REQUIRED TO CORRECT THE INTERFERENCE.

OPERATING MANUAL

MODEL K101-D LOGIC ANALYZER

NOTICE

This design and related information contained here in is the sole property of Gould Inc., Instruments Division, Santa Clara, California, U.S.A. Prior permission to reproduce this information or the products disclosed herein must be obtained in writing.

Section 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual is designed to systematically acquaint you with the features and operation of the Gould K101-D Logic Analyzer. The text describes basic building blocks for test operations, which can be combined in a number of ways for different applications. These building blocks will make it easy for you to use the K101-D to solve a variety of hardware/software problems. Once you become familiar with the basic operations of the K101-D and the test operation building blocks, you will be able to create the exact configuration necessary to solve your specific problem in a fraction of the time that other techniques now require.

The K101-D can record and analyze both digital data patterns and timing information. The data can be displayed to show both timing and logical relationships in a variety of formats. As you use the K101-D, you will be able to obtain new perspectives on the nature of the problem you are investigating. This in turn will often lead you to powerful insights into the actual causes.

You will find that it is relatively easy to use the K101-D. When the basic approach and capabilities of the K101-D are understood, the details and ramifications of how it can be used fall into place. The manual focuses on the way the individual building blocks provided by the instrument can be combined to provide insights for problem solution.

The K101-D is a tool for problem solving; you have to decide how to use this tool. You should be familiar with the K101-D and with the system that needs to be analyzed. In some cases, a two-person team, one strong

in hardware and the other in software, may make especially good use of the K101-D.

1.2 **GENERAL DESCRIPTION**

The K101-D is a high performance, general purpose, digital test instrument designed to offer users powerful capabilities to examine real time execution of program flows; system timing characteristics; the interaction of system elements; and hardware/software integration and verification. Applications include hardware and firmware design and debugging, automated test equipment, field service, and education.

1.2.1 INFORMATION FLOW

Logic analysis emphasizes selected or meaningful data, rather than raw data. Therefore, when the term "data" is used in this manual, it generally refers to selected data. The theme of this manual is how to turn raw data into meaningful information. In Figure 1-1 the term "information" is used to emphasize this theme.

Figure 1-1 shows the general flow of information and control in the K101-D, and how the user controls the information flow. First, the user selects the desired data and clocking signals to be examined. The raw data are collected with the K101-D probes and entered into the sample registers and data pipelines. When necessary, the data are delayed and aligned to present a meaningful combination. The trace control logic can be used to evaluate the selected data according to criteria set by the user. Based on that evaluation, selected information is shifted into high speed main memory. At the end of the recording process the selected information in main memory is copied automatically to display memory A.

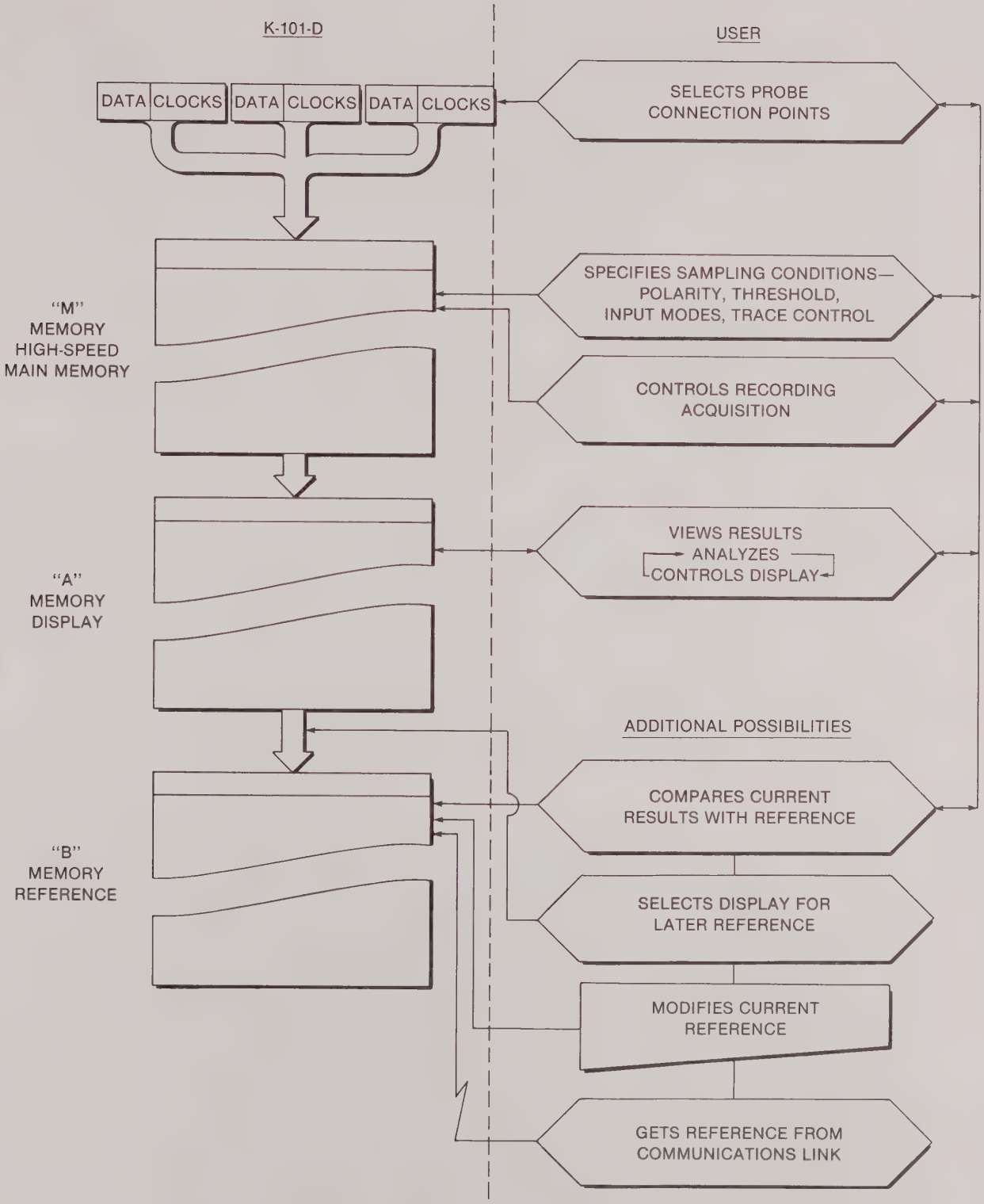


Figure 1-1. Flow of Information and Control in the K101-D Logic Analyzer.

The basis of selection can be simple or sophisticated. It is possible to program the instrument to evaluate several million events and select only a crucial half-dozen or so of those events for later examination. This process is accomplished by specifying a chain of unique interactions of time and data patterns that define the desired information capture.

As Figure 1-1 shows, reference memory B is the same size as display memory A. The user can choose to enter information into memory B from memory A, from a keyboard, or from a communications link. The reference memory is available for comparison with the information in memory A.

In the next step the user analyzes the information. The recorded events in display memory A are examined to see how the captured information corresponds to what was expected. The user can (a) search through the events for certain patterns or relationships, (b) measure time relations between events, and (c) compare prior events in memory B with current ones in memory A. Each sampled input that meets the trace specifications and remains in memory is available for analysis. Therefore, it is possible to look beyond the trace specification fields to examine related information or find unexpected relationships.

The process is both iterative and interactive. The user may want to develop a design, verify system functioning, troubleshoot a problem, or set up a long exercise and look for possible trouble. The user sets up the K101-D to sample the desired signals, selects the trace criteria, displays the captured events, and analyzes them. The user then factors in what has been learned and repeats the cycle until a solution is reached.

1.2.2 APPLICATIONS FOR THE K101-D

Although sequential triggering is sufficient for many hardware applications, it has limitations when applied to microprocessor- and software-oriented work. Without multiple levels of trace control, it is very difficult to follow the execution of separated, interactive, or deeply nested subroutines in order to isolate the exact timing or program activity that you want to record. The K101-D has 16 levels of trace control. There is also a need for some method of following program branches and program restarts without filling record memory with unwanted data. With its concurrent logic (the commands to ADVANCE, JUMP, STOP, and conditionally TRACE), the K101-D can effectively address these and many other problems.

The K101-D can be used effectively throughout the development, production, and service phases of programs for almost any digital system (see Figure 1-2). Some of these uses are listed below.

a. During development of hardware: to check timing relationships (the rise and fall of signals in proper sequence), to detect glitches, to verify data execution paths, and to record desired information.

b. During development of software: to check portions of the software that are hardware dependent; to check timing relationships for writing commands to devices and reading data or status from devices.

c. During integration: to verify individual functions and troubleshoot the system. In the final stages of integration, when problems become more subtle and intractable, the K101-D can be used to isolate and trace a wide variety of obscure difficulties. This instrument allows you to thoroughly investigate the complex relationships between the hardware and software.

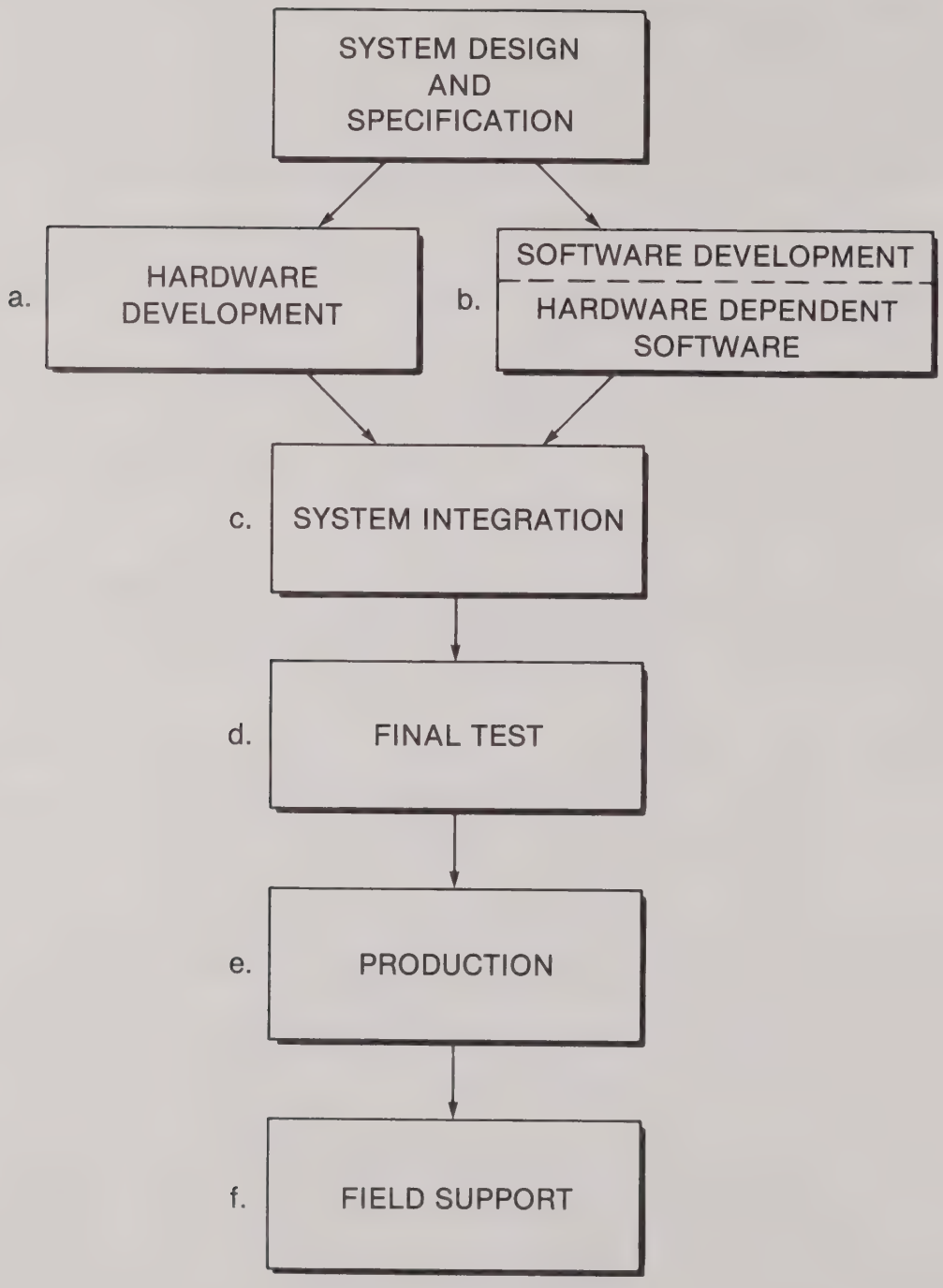


Figure 1-2. Using the K101-D During System Design and Production.

d. During final test the K101-D can be incorporated into the test setup to monitor performance. The unit can be set to cycle automatically, testing and retesting day and night, checking for erroneous operation.

e. During production: to test and verify performance.

f. During service, two K101-D analyzers can be coupled via a data link so that a technician at a remote site can consult with the home office or other authoritative technical source to resolve unusually difficult problems.

1.3 OVERVIEW OF THE MANUAL

This manual is organized to assist you with the different phases of system problem solving, starting with an initial statement of the problem, followed by collection and analysis of system data, and leading either directly to a solution or to successively more precise restatements of the problem to guide further testing until a solution is found.

Since the K101-D allows you to solve many system problems in a fraction of the time required by less sophisticated instruments, you may find that you do not use your K101-D every day. This manual is designed so that you can quickly recover your familiarity with the K101-D by referring to the appropriate sections of the manual.

For convenience, the sections of the manual can be thought of as groups. This section, General Information (Section 1), gives general information about the functions and applications of the K101-D. Section 2 (Principles of Logic Analysis) develops those principles with reference to the K101-D. Sections 3 and 4 (Detailed Description and User Controls and Displays, respectively) describe in detail the functions of the logic analyzer and how to make use of them from the front panel.

At the heart of the manual are Sections 5 through 7: Specifying Recording Parameters, Making a Recording, and Recording Analysis, respectively. These three sections explain how to set up the recording conditions, control the recording process, and analyze the results. They present the practical development of themes in the second section, Principles of Logic Analysis.

Section 8 (Applications) contains detailed, worked out examples of clocking and trace control. It starts with very simple examples and gradually builds up to complex ones. Section 8 helps to consolidate the knowledge presented in prior sections and is of great practical help in learning how to use the K101-D.

Section 9 (Communications) is a complete, self-contained explanation of the two communication modes useable with the K101-D. It explains the process of communication and how to operate the logic analyzer remotely.

Section 10 (Measurement Confidence) explains the Self-Test, Power Up Test, and the Probe Test. The Self-Test allows the user to check the device with the equivalent of the quality assurance test performed in the factory. The Probe Test is far more than a basic checkout of the probes. It uses an internal pattern generator to allow stepping through a variety of sequences of sampling, recording and analyzing data. Because the patterns are known, using the capablities of the Probe Test is an excellent way to learn to use the K101-D.

The last six sections of the manual, Sections 11 through 16, are entitled Related Literature, Reference Material, Glossary, Input Connection Guide and Setup Guide, Index, and Accessories, respectively. Related Literature provides a place for material such as application notes and copies of magazine articles.

The glossary gives useful explanations of terms and also provides a conceptual overview that shows how some of the basic concepts are interrelated.

Section 2

PRINCIPLES OF LOGIC ANALYSIS

2.1 OVERVIEW

The problems that can be solved with the K101-D range from very simple, obvious symptoms to extremely complex and subtle patterns of system behavior. Despite the potential complexity of the problems that can be investigated, the basic process involved in using the K101-D is straightforward. A conceptual diagram of this process is given in Figure 2-1.

As you may anticipate, you need to know (a) something about the way the system to be analyzed is expected to behave, (b) some details of the system hardware and software, and (c) how to use the K101-D. You do not need to know "everything" about these items. In fact, you learn as you go. In the basic process you can build upon your current knowledge, try something with the K101-D, then refine your original analysis. This is an iterative approach and is depicted in Figure 2-2. Notice that each time you analyze the problem, the data collected with the K101-D add to your base of knowledge and lead you to the solution of the problem.

Remember that the K101-D does not solve the problem. It is a tool for problem solving; you must define how to use the tool. This manual is designed to assist you in using the K101-D in practical applications. The material is organized with respect to the three categories of effort as defined in Figure 2-1: setup and data collection, data reduction, and data organization.

Logic analyzers are a class of instruments specifically designed to simultaneously monitor and record digital information from several different signals over a number of consecutive time periods. Introduced in 1973 (less than three years after the first microprocessor), these

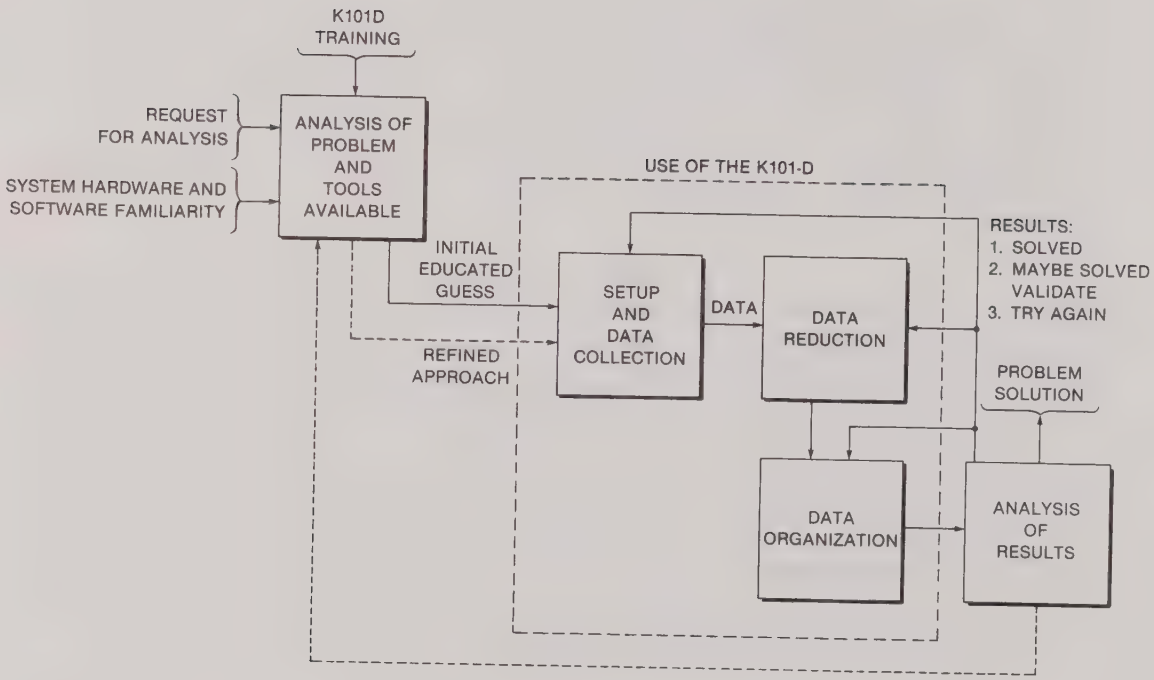


Figure 2-1. Basic Process for Using the K101-D Logic Analyzer.

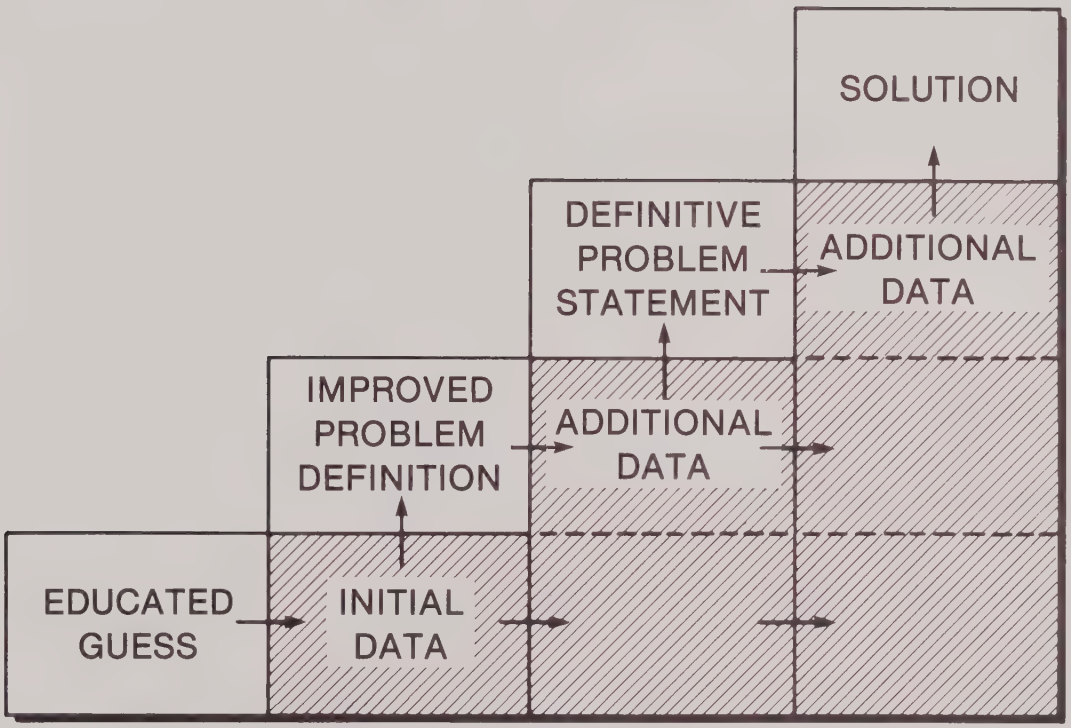


Figure 2-2. Iterative Approach to Problem Solving.

instruments can sample digital data transitions synchronously to obtain data domain (logic state) recordings of program activity, or asynchronously to obtain time domain recordings of signal pulse widths and relative timing skews. The K101-D incorporates powerful data formatting, search, and compare functions to assist you in analyzing recorded data. Such data recordings show dynamic software execution in the system under test and provide complete information on the types of instructions executed.

2.2 **CAPABILITIES AND TOOLS OF THE K101-D**

2.2.1 SPECIFYING THE RECORDING PROCESS

There are two basic recording modes at your command: recording based on a triggering event or based on a delay. These modes can be used together. When making a recording based on a triggering event, the recording can precede, surround, or follow the event. This feature is useful for determining the results of an event, or which event led to a fault. Delayed recording enables you to record information that occurs after a trigger event. This recording method is similar to delay sweep triggering on a scope; however, the logic analyzer's delay intervals are much more precise because they can be controlled either by clock pulses or by repetitions of a trigger event.

When we discuss trace control logic later, we will show how these two basic approaches can be combined in a group of specifications that allows the user to define a complete procedure for monitoring events within the system under test. The conditions for monitoring and for tracing can be defined to follow the expected course of events in the system under test and to follow bypaths when unexpected events occur. Trace control is specified independently of the monitoring logic, so that you can, for example, not trace when all is proceeding as expected and trace when the monitoring logic you have specified takes an unexpected twist.

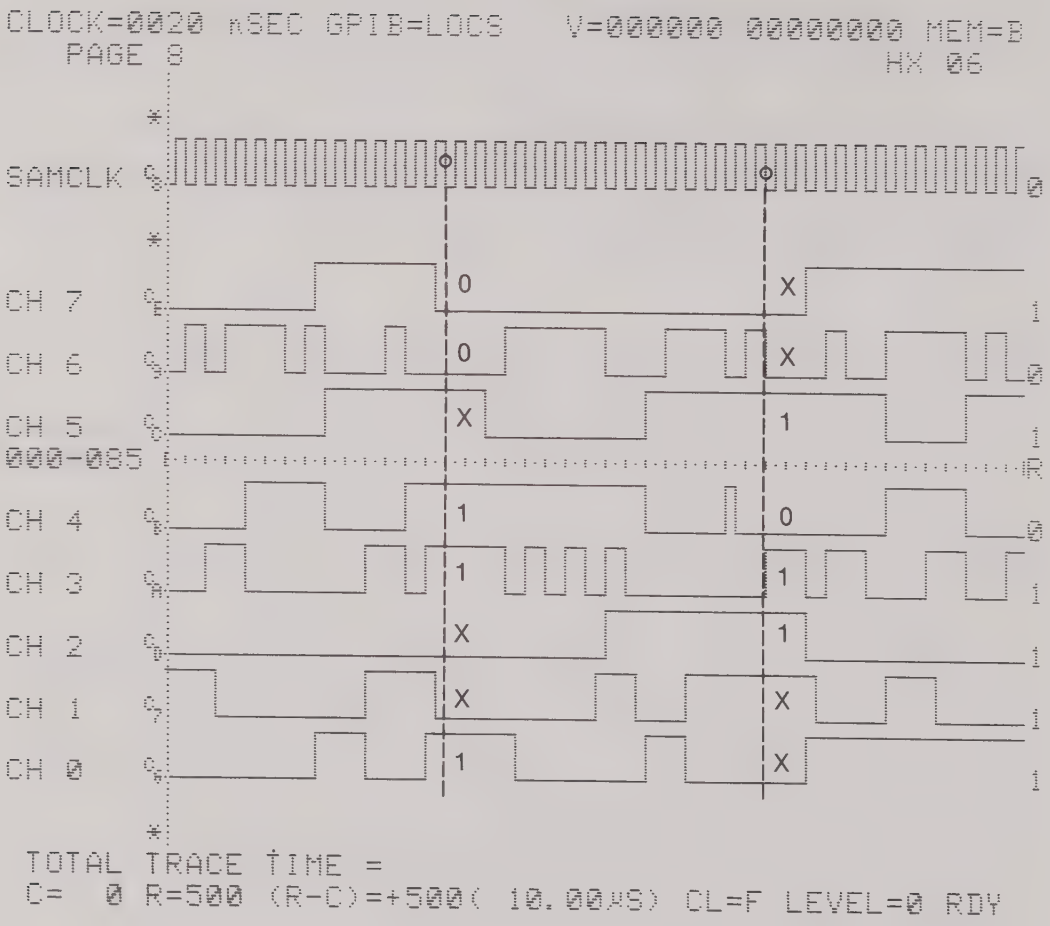
There are two basic kinds of data that the logic analyzer can follow, timing data and state data. Examples of timing data are the timing relationships of input and output signals of a device, PC card, backplane, or interface. Examples of state data are the information transferred on address and data lines of a computer system. The logic analyzer can follow both kinds of data at the same time and show their interrelationship.

With the K101-D, you can very precisely specify clocking information to monitor events with internal or external clocking or a combination of both. These clocking modes are suitable for monitoring state data, timing data, or for precise rejection (filtering) of irrelevant data. This allows you to focus on events that happen at particular conjunctions of internal and external events in the system under test.

Keep in mind that the K101-D is a digital sampling instrument. It continuously monitors signal states and detects and stores them as binary values in semiconductor memory. The instrument ignores all analog waveform features (other than logic level), including rise and fall times, peak and offset voltages, ringing (unless very pronounced), and noise.

Figure 2-3 gives an example of the digital approach to events in the system under test. Two possible combinations of states have been specified in binary (using combinations of one, zero, and "Don't Care") as triggering events to start making recordings. The clocking and timing patterns are shown as idealized digital events. With analog instrumentation, one would have to interpret the waveforms to define the events digitally.

Logic analyzers generally provide several standard threshold voltages as well as a variable voltage threshold. This feature allows recording of data from various IC families such as ECL, TTL, or CMOS. In the K101-D, groups of input signals can use different thresholds for recording



Note: The analyzer can start tracing on event 1, event 2, or the combination of both. Input selections; 1 high, 0 low, x don't care.

Channel	7	6	5	4	3	2	1	0
Event 1	0	0	X	1	1	X	X	1
Event 2	X	X	1	0	1	1	X	X

Figure 2-3. Combinational Binary Specification of Inputs.

signals from mixed logic circuits. Polarity is specified for each input signal.

The K101-D has four modes for detecting input: Sample, Glitch, Latch, and Demux (Demultiplex). In Sample mode, inputs are sampled only at each active edge of the sample clock, and any threshold transitions between clock edges are ignored. Glitch mode is used to catch those transitions that may occur between the clock edges.

Latch mode is an organizational technique which latches a sample when it becomes valid and holds it for later sampling. This capablity is useful because of the way the K101-D can use data patterns for controlling logic flow and tracing. With Latch mode, related data patterns that occur at different times can be combined as one sample event. That event can be used for logic control or can be traced for information, or both used and traced. Demux mode is a predefined form of Latch mode. It is used for such cases as demultiplexing an address and associated data when they appear sequentially on the same bus.

The four basic input modes can be combined with the clocking specification to provide additional choices. For example, a combination of clocks could be used with Latch mode to detect a key conjunction of events that occurs only rarely.

Conversely, some combinations of input modes and clocking specifications can lead to problems, such as the missed sampling of some events or the distorted recording of others.

As mentioned earlier, logic control and conditional tracing can be controlled by using data pattern comparisons or delays or combinations of both. Use of a data pattern is a form of combinatorial triggering. Each input signal of the 48 possible signals can be specified in terms of a three position switch, set at one (1), zero (0), or "Don't Care" (x). Thus you can trigger from one input signal by setting all others

to "Don't Care," or trigger an action using a combination of settings that might vary from simple to complex.

These patterns of one and zero, which are evaluated for control of the recording process and possible tracing, are the result of previous specifications. Specifications of polarity, threshold, input mode, and clocking result in a signal or one or zero in a sampling register, available in combination with all other signals. With Latch mode and similar techniques, you can evaluate, as one combined event, activities that actually happen at different times in the system under test.

The patterns can be treated as a sequence of binary signals, but for convenience in dealing with the data you can choose from several modes of formatting. Data can be looked at as a fixed sequence of binary, octal, or hexadecimal characters, or can be specified as individual numeric characters or ASCII or EBCDIC characters, either in fixed order or in user-specified order. When data are captured for tracing they can be viewed in the format specified. The data pattern available for control use is determined by the specified data format.

2.2.2 RECORDING USING THE SPECIFICATIONS

As the logic analyzer receives and evaluates data, it continually decides what trace control actions to take. For example, it decides whether to trace in memory the current data pattern, whether to stop the recording process, and whether to move from the current set of trace control specifications to another set. The user can specify up to 16 sets of trace control specifications.

By combining delays and combinatorial triggering, you can have a great deal of control. Consider three basic examples. In the first case, you wish to see what leads up to a particular set of events in the system under test. You specify those events as a data pattern and tell the trace control logic to trace until that data pattern is seen and then

stop. When the recording is made, data flow into the trace memory and are replaced by later events, since only about 500 events can be saved. Suddenly, the data pattern of interest is seen and the trace control logic stops the recording process, freezing the current traced information, which you can review.

In the second case, you wish to view events both before and a while after the crucial event. You specify that a delay count start when the crucial data pattern is encountered, and that the recording stop when the count of events is done. The resulting record will show events before and after the crucial event.

In the third case, you are interested only in what happens after the event. The triggering event then is used to start tracing with a delay set to stop tracing when memory is full.

Each of these three examples is simple to specify, and each could be done with one or two sets of specifications, leaving fourteen or fifteen other sets still available. By using basic setups such as these for building blocks, you can perform such tasks as checking that three or four events happen in the correct sequence in the system under test, skipping over a million or so events of no interest, and then specifying four or five possible events that you want to trace in case the event happens.

2.2.3 REVIEWING AND ANALYZING THE RESULTS

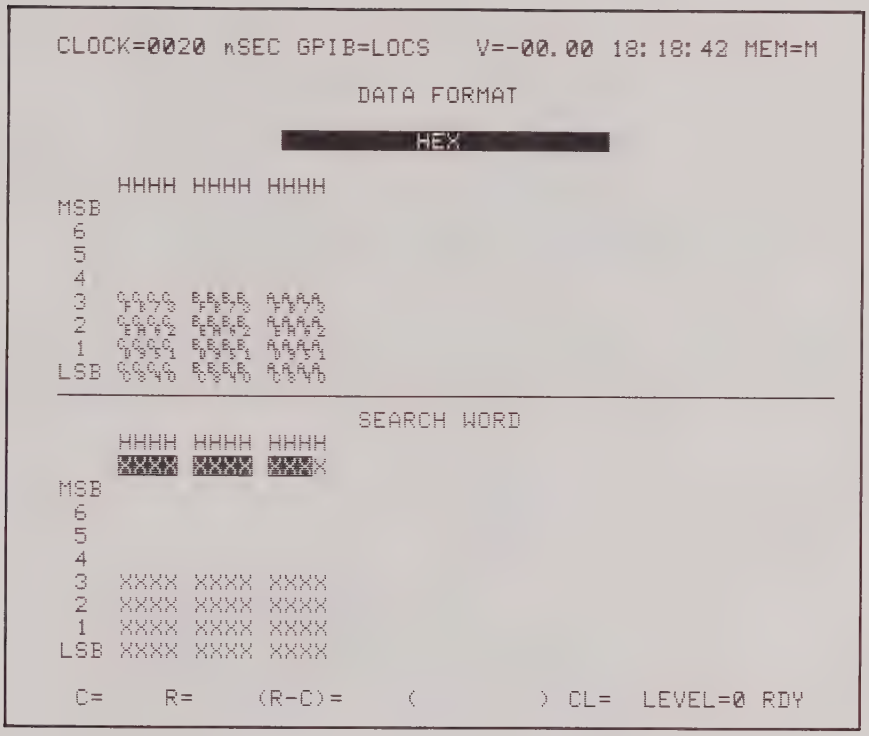
To review recordings, the K101-D provides three main data display formats designed to show specific kinds of information. The Data display shows the actual events as captured. It uses the data format you specify and allows you to see all captured events in memory. This display is also called a state display, because is is a record of states from the system under test (see Figure 2-4 for an example).

The Timing display is a diagram that shows each individual input signal as a horizontal line, presenting it in terms of its rise and fall (one or zero) over time. This allows for quick correlation between events. Various tools are available for manipulating and evaluating the timing diagram. The fastest available clocking rate in the K101-D is 10 nanoseconds. Because events are sampled and stored as ones or zeros and the timing diagram is reconstructed from the stored samples, an uncertainty of ±1 sample is always present at each transition. However, the timing diagram can support resolution of timing among input signals to 10 nanoseconds across all inputs (see Figure 2-5 for an example).

The third display is a graphic display of the stored data, showing the relative magnitudes of data over time, making it easy to get a general grasp or overview of events. Various tools are available for manipulating this display to expand it or clip it, and to help evaluate it (see Figure 2-6 for an example).

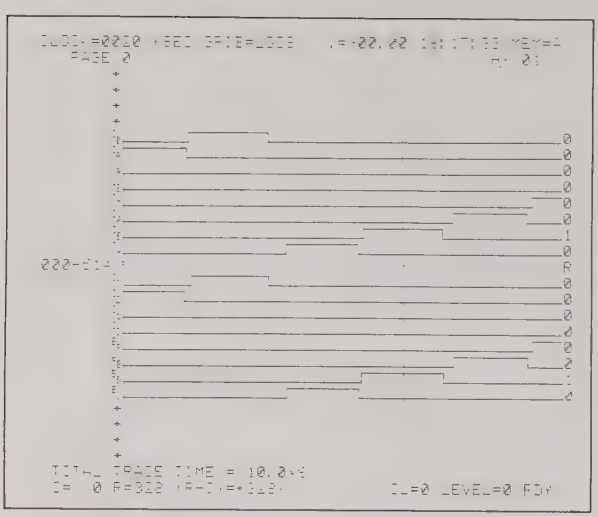
The state data from a recording can be saved in a reference memory and then compared with a newer recording. Reference data can be seen in all three modes mentioned, as state data, timing diagrams, or graphic display. A search function can look at data in either the current display memory or the reference memory, and a compare function can compare the two. It is also possible to edit the reference memory in order to facilitate comparison, by developing a particular desired sequence of events or idealized result and comparing it to the actual results.

Recordings of these types can give you new perspectives for viewing design anomalies in both hardware and software interactions. This capability is based on the precision with which you can specify the content and sampling methods that produce these recordings and variety of methods available to work with and evaluate the recorded data.



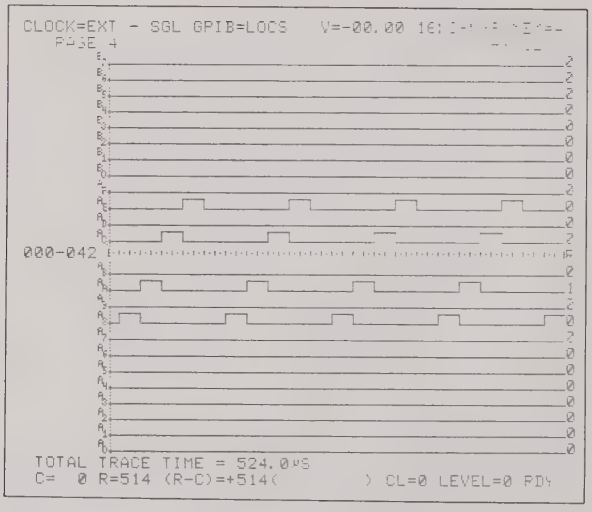
Note: Data in this display are grouped in columns of four bits (input signals) each. Twelve hexadecimal digits contain the state of all 48 inputs. The three-digit decimal number on the left gives the memory location containing the data on the right. The same data could be grouped in other ways, for example in columns of three using 16 octal characters.

Figure 2-4. Data Display.



Note: Sixteen input signals are displayed here in expanded form. The vertical line is one of two cursors. The display can be scrolled left or right.

Figure 2-5. Timing Diagram Display.



Note: This display is a way of showing the magnitude of recorded state data as a general pattern of data over time. It is the only display that can show the entire recording on one screen.

Figure 2-6. Graphic Display.

Remember that you can use the logic analyzer to view what is happening from several perspectives. The more varied the perspectives, the more likely you are to find the problem.

2.2.4 DEFAULT CAPABILITY

There are default or standard setups for specification of all recording parameters and for the viewing of results. In a typical recording session, it would be very unusual to specify every recording parameter in detail, or to make use of every evaluation technique when you analyze results.

2.2.5 SUMMARY

The K101-D is set up for recording by specifying the following:

a. Signal input polarity
b. Signal input threshold level
c. Input mode: Sample, Glitch, Latch, or Demux
d. Clocking: internal, external, or mixed
e. Data format
f. Trace control conditions

Then the recording is made and the results are evaluated. Analysis of results is supported by the following:

a. Data display
b. Timing display
c. Graphic display
d. Display manipulation and enhancement tools
e. Comparison with prior results or other reference
f. Search function
g. Edit function

2.3 BUILDING BLOCKS

There are several operational steps that are commonly used together for specific applications and can be organized into identifiable sets. These specific sets of operations may be viewed as basic building blocks you can then further assemble in a number of different ways for more complex analysis. The three examples of trace control described in paragraph 2.2.2 are representative examples of some basic building blocks. Where appropriate, subsequent sections of this manual refer to the building blocks.

2.4 GENERAL APPROACH TO USING THE K101-D

With the general overview of the capabilities of the K101-D as a background, we will now discuss the general approach to using it and examine some of the steps in greater detail.

The K101-D can tell you what is happening in the system under test. You also need to know what should be happening. Sometimes the problem in the system will only involve hardware, sometimes software, and frequently both.

You will receive the greatest possible benefits in using the K101-D with your digital system if you understand the definition and characteristics of the signals of your system and their relationships. This will enable you to efficiently connect the logic analyzer to the target system, monitor its activity, and recognize what is in error. When lacking system documentation or verification, the K101-D is a tool you can use for general measurements to increase your understanding of the system under test and guide you to more specific and efficient recordings.

For maximum productivity, you should quickly capture meaningful and relevant information as needed to test specific hypotheses about system activity. You must be able to specify precisely how the logic analyzer

is to collect, reduce, and organize the data. Specifically, you must connect to the target system and any other instrumentation being used, select the correct polarity and threshold, clock the inputs to reduce the incoming data to comprehensive samples of program activity, use trace control to select events of interest, and organize the collected data for display and analysis.

2.4.1 PROBES

Physical connection between the logic analyzer and your system is made through special high-performance probes, each capable of inputting several data and control lines from individual IC and wire leads, DIP clips, or the optional microprocessor disassembly accessories. Individual wire leads give total flexibility in connecting anywhere in your system; a DIP clip or microprocessor disassembly accessory make connection fast and simple. In general, you need to know the pin assignments of your system and the signals expected on these pins.

2.4.2 POLARITY AND THRESHOLD

You can tell the logic analyzer what rules to follow in making polarity decisions, i.e., which way is up (polarity) and where to draw the line (threshold). In positive polarity logic, voltages above the threshold are defined as a one and voltages below as a zero. In negative polarity logic, above is a zero and below, a one. (If you don't specify, the logic analyzer uses positive polarity.) Polarity is simply indicated by a "+" for positive and a "-" for negative. The polarity of each channel can be individually defined.

The threshold voltage level divides a waveform into two states: one above and one below the threshold. The analyzer gives you the ability to choose preprogrammed values, such as TTL = +1.4 V, or lets you input any value within a range (variable). Threshold values apply to a grouping of channels matching each probe pod of two clocks and eight

sample inputs. This selectability for each probe allows you to simultaneously test segments of your system that use different logic levels.

2.4.3 DATA FORMAT

You will often want to define a data format. Data formatting allows you to flexibly group the data lines, order them in various ways, and look at their values as words in a way that makes sense to you and your application. When properly set up, the logic analyzer groups the input data in a way that is easy for you to understand and analyze. You can choose a fixed format for ease of specification or specify a format in detail for convenience in later use. The same data format is used to set up trigger/trace control words, to display state data, and to set a search pattern. The data input lines can be grouped to form various base number systems (radices) or data codes, such as ASCII. The format can be uniform (the same radix) for all inputs or mixed (several formats used simultaneously).

The basic digital code is binary. Each input line can be viewed in binary format as one of two logic states, one or zero. In octal format, groups of three such binary digits (bits) become a single octal digit. In hexadecimal, four bits become one hex digit. ASCII and EBCDIC are common data formatting codes that convert multiple bits into alphanumeric characters. You can use any of these codes. When using the optional microprocessor disassembly module, the binary information understood by the microprocessor is converted for user convenience into mnemonics, which are easy-to-remember abbreviations of microprocessor operations and data.

The ability to mix formats is especially useful. For example, you may want to see address and data lines in hexadecimal and the control and status lines individually in binary. Additionally, you can define the

other signals, or even the same ones again, in some different format -- whatever you need for your system.

2.4.4 CLOCKING OF INPUTS

You must specify how you want to sample the incoming data and when you want to store the data in memory. The incoming data are repeatedly filtered to yield useful information: clear and concise, without unwanted (data) noise. The two main clocking modes are synchronous and asynchronous (also referred to as external and internal clocking, respectively). Single clocks or multiple clocks in combination can be used to let you see the data exactly as your system does or in greater detail. Up to six clock terms can be combined in a Boolean expression to form one precise clock definition. The K101-D's clocking features give you great capability to be selective and clever in filtering and reducing your incoming data to the most meaningful form.

2.4.5 TRACING AND ACQUISITION

The precision with which you select the area(s) of data flow for the logic analyzer to capture greatly affects how easy it will be to analyze the system under test. Even with only valid and qualified data samples coming into the analyzer you still need to tell the K101-D when to start and stop collecting data as well as exactly what data in the stream you want it to extract. This can be as simple as instructing the logic analyzer to show you a window of data immediately surrounding a specific event or as powerful as selecting out nonconnected segments of data based on complex program flow conditions.

a. Simple triggering, with or without delay. Simple triggering is most useful for hardware debugging and the first pass of software debugging.

In microprocessor systems, especially when following software execution, a better method of pinpointing the trigger is needed. The word you select to trigger on likely occurs many times in your data stream; you can seldom be sure the analyzer will stop exactly where you want it to. If your trigger word isn't unique, a single trigger will cost you time and cause you a lot of trouble.

b. Complex triggering, with or without delay. Complex triggering is especially useful in following the program execution of nested subroutines and for isolating precise skew measurements. This slightly more sophisticated approach lets you look for several trigger words (trigger events), perhaps in a particular sequence, and use the sequence or combination of events to control the recording process.

c. Selective trace. Selective tracing lets you fill memory with only certain data words that are of interest to the problem at hand. You follow many events, but trace very selectively. Unneeded data are not recorded. You can select, say, 500, 20, or no events out of millions of sequential samples.

d. Conditional trace control. This advanced technique fully used the K101-D's capability to control the tracing and storing of data. Conditional trace control combines complex triggering (with or without delays) and selective trace control. You can follow many events, allow for many contingencies, and trace only the events you want to see. The features of conditional trace control give the K101-D its incredible power and give you the ability to follow and understand the activities and ramifications of the program in the system under test.

2.4.6 MAKING THE RECORDING

The start of the recording process is called "arming" and can be controlled manually by you or automatically by the analyzer for powerful extended data analysis and testing capabilities. You select manual or automatic arming and then press the appropriate key when your preparations are complete and the system is ready.

2.4.7 DISPLAYING AND ANALYZING THE DATA

There are several ways in which you can view the data; each one gives you different information by providing a unique perspective. The logic analyzer formats and displays data as state tables, timing diagrams, graphs, or disassembled mnemonics. You select one of these formats by the press of a key. Powerful functions for display manipulation, search, comparison, and editing are available to help you analyze the data. Also shown on the screen is useful status information about the recording process itself. The different formats are described below.

a. Data domain: A state table, or data domain display, contains every item of recorded information. It is the basis for the other displays.

b. Timing: Each line of information that comes into the analyzer is shown as a reconstructed waveform indicating at each sample point whether the line is at a logic high or low.

c. Graph: This display shows an overview of program behavior. The contents of the entire memory can be graphically displayed simultaneously on this screen. The vertical axis plots the numerical value of each data word against its physical location in memory on the horizontal axis. The word you wish to graph can be composed of all channel inputs or some subset of inputs. Graphing helps you easily identify loops, branch

points, areas of memory activity, control/status cycles, address ranges, and repeated word occurrences.

d. Status information: Two lines of status information are always present on the screen. They supply various acquisition and display parameters. When reviewing captured data, the status words indicate which memory is being displayed, what clocking mode was used, and the location of the cursors and the difference between them in time and sample clocks. Two status fields, concerned with trace control levels, indicate where tracing was halted and the trace level at which each word occurred, and provide a real-time readout of the current trace level while the trace is in process (see Figure 2-7).

e. Mnemonic disassembly: This option is available with the microprocessor-specific devices called Real-Time Execution Disassemblers. The disassembly display shows the translation (disassembly) of numerical state data into the English-like mnemonics of assembly language. The displayed data are broken out into address bus data, data bus contents (data or instruction), the mnemonic translation of the microprocessor instruction and operation, and bus activity status information (see Figure 2-8 for an example).

2.5 COMMUNICATION INTERFACE

Using the logic analyzer in conjunction with other "intelligent" equipment greatly extends its capabilities. Automatic testing and computer analysis are possible. Setup parameters, captured data, instrument commands, and recorded information can be transferred between instruments to allow hard copy generation, comparison, storage, further analysis, or remote testing. Communication with other intelligent instruments or computers occurs via an interface channel, either RS-232 or GPIB (see Section 9 for details).

1
2
3
4
5
CLOCK=EXT - MLT GPIB=LOCS V=-00.00 11:20:47 MEM=M
STATUS FIELDS
1) Clock Mode – that was used to make the last or upcoming recording.
2) GPIB – status of GPIB.
3) DVM – real time reading of voltage at DVM lead inputs.
4) Time of Day – real time, 24 hour clock backed by internal battery.
5) Memory – displayed memory or memory that set-up parameters pertain to.
6) Control Cursor – internal memory location of control cursor.
7) Reference Cursor – internal memory location of reference cursor.
8) Cursor Location Difference – difference between C & R cursor in terms of memory locations.
9) Cursor Time Difference – difference between C & R cursors in terms of time (only specified if the master clock was chosen as internal).
10) Cursor Level – which level was used to record each sample.
11) Trace Level – current or last trace level reached during a recording.
12) Arm Mode – status of acquisition cycle.
C= R= (R-C)= ( ) CL= LEVEL=0 RDY
6
7
8
9
10
11
12

Figure 2-7. Screen Display of Status Information.

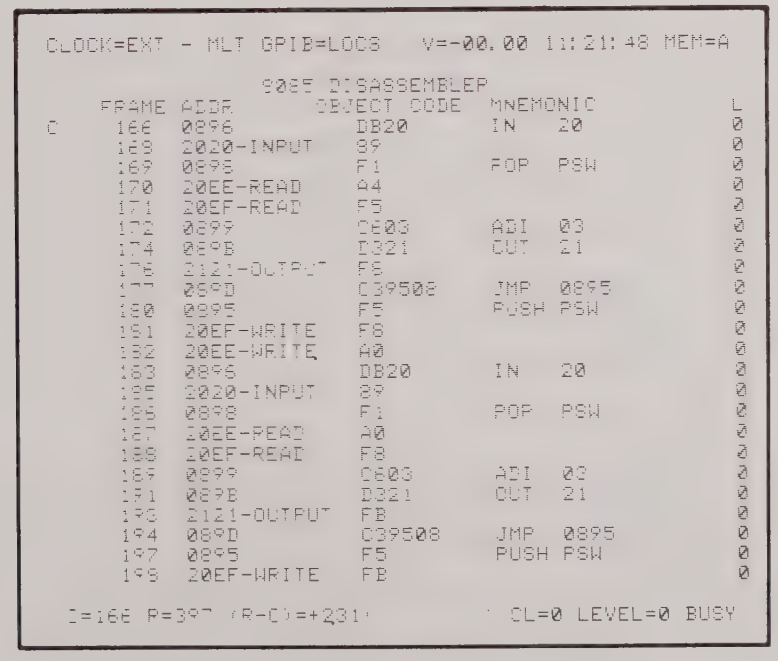


Figure 2-8. Mnemonic Disassembly Display.

The communication capability allows effective remote consultation (in which an off-site expert can assist someone on-site) and rapid distribution of critical data.

2.6 COLLECT -> REDUCE -> ORGANIZE

As stated at the beginning of this section, with the K101-D you approach even the most difficult problems in three general phases: collect, reduce, organize. In practice, these three are interrelated. They are not isolated activities, but are subcategories of data handling. When you collect data, for example, you have already done some mental organization and reduction in order to collect only useful data.

2.6.1 THE COLLECT/REDUCE/ORGANIZE MATRIX

The data handling tools of the K101-D can be thought of in these subcategories. One may regard probe positioning as a method of collecting data, the use of the Graphic display as a way of organizing data, and the selection of the Latch input mode as a way of reducing data to select only special cases. Figure 2-9 shows a matrix in which all the K101-D techniques are placed in the categories of collect, reduce, and organize. Actually, many of the techniques are shown across boundaries because they properly belong in two categories, such as collection and reduction. The general categories of action in which these techniques are grouped, such as physical setup, or specification of recording parameters, are shown on the left.

The major purpose of the Collect/Reduce/Organize matrix is to help you conceptually organize the material discussed in this section and covered in detail in the next five sections. Sections 3 and 4 give reference information and explain how to specify K101-D functions. Sections 5, 6, and 7 discuss the topics shown in the matrix and give information on

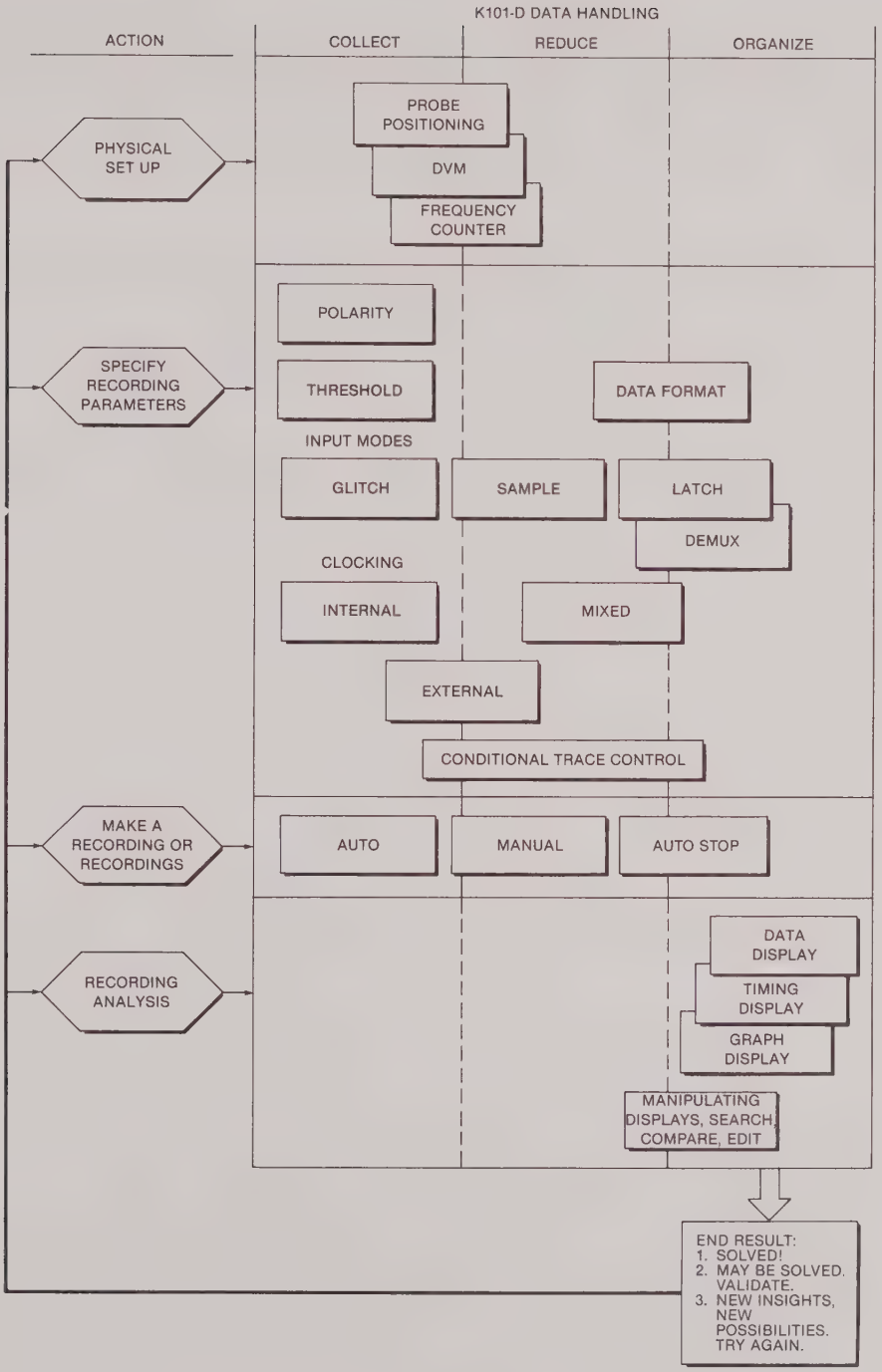


Figure 2-9. The Collect, Reduce, and Organize Matrix.

when and why to use them. This figure and the following discussion (paragraphs 2.6.2 through 2.6.6) preview the material in these sections. The preview explains why techniques are placed in the three categories, and focuses on the question "What can these tools do for me?"

The matrix also serves as a quick overview and reminder when you are using the K101-D. For example, by glancing down the collect column, you can see what techniques would quickly collect basic information. The other two columns can function as reminders of additional techniques useful for further investigation. In a general sense, the techniques shown under the reduce and organize columns depend on the techniques shown under the collect column.

Before reading the preview and explanation, note that the Collect/Reduce/Organize matrix is not rigid. It is meant only to help you learn about the K101-D and to serve as a quick reminder. Feel free to make up your own version.

2.6.2 PHYSICAL SETUP

Generally, this consists of setting the probes at points of the system under test. The task is primarily one of collection, with an element of reduction because from the beginning you do not probe those parts of the system under test that are not relevant to your particular test.

The DVM (digital voltmeter) is also shown here. It is a convenience, useful when needed. You could use it for a one-shot checkout of system values, or to collect information in real-time during the test session. For either use, you examine the values visually at the time the value is shown. Using the DVM involves reduction, because only one location of the system under test may be sampled at any one time. Therefore, using the DVM is shown as primarily collection with an element of reduction.

Use of the frequency counter is an optional part of clocking; it is a basic collection technique, also with an element of reduction.

2.6.3 SPECIFY RECORDING PARAMETERS

Specifying the threshold values and polarity of the input probes is a basic part of collection.

The four input modes are shown across the data handling spectrum. Sampling mode collects basic events based on clocking so both collection and reduction are accomplished. Glitch mode is broader, and collects both glitches and normal samples. Because glitch mode collects more broadly than sample, while sample mode restricts itself to normal samples, glitch mode is shown under collect and sample mode under reduce. Latch mode can be used for either reduction (sophisticated filtering) or organization (sample input skew alignment). Demux mode is primarily an organizational technique, although its use does compact all samples by a factor of two over the memory space otherwise needed to contain the same information. Both Latch and Demux allow you to bring together events that happened at different times and show them in a logical relationship as one sample. The organizational theme is predominate, and both Latch mode and Demux mode are shown in that column.

Clocking has several modes, which are variations of using internal or external clocking or a mixture of the two. Internal and external clocking are basic collection techniques that normalize the sampling. Mixed clocking allows very discriminating sampling of particular events that happen at clocking interactions, and therefore is shown under the reduce and organize columns.

Trace control logic is the heart of the analyzer. There are separate commands for controlling the logic flow and the tracing. The logic flow can monitor millions of events in the system under test, both expected

and unexpected, and trace only the events of interest. Conditional trace control capabilities are extremely powerful tools for collection, reduction, and organization, and are shown across the three categories.

2.6.4 MAKE A RECORDING OR RECORDINGS

Manual recording is a one-time recording which can then be examined with the analytic techniques mentioned below. Automatic recording repeats the collection process automatically. Automatic recording with stop (Auto stop) allows repeated recording controlled by comparisons; it is used to find elusive errors or validate that a problem has been corrected. Because automatic recording can collect so much data in comparison to manual recording, we place it under collect and manual recording under reduce. Auto stop could be considered a reduction technique because it hunts through and discards recordings until it finds a particular case. However, it is placed under organize because using it involves organizing prior knowledge about the system under test. In setting up Auto stop, organization is the primary theme.

2.6.5 RECORDING ANALYSIS

The three display modes (Data, Timing, and Graph) are all under the organize category. Each mode provides unique perspectives (screen organizations) of captured information designed to assist in rapid analysis appropriate to your application. The Data display is useful for reviewing logic state relationships such as detailed program execution. Graph display supresses the details of each sample to a single point to provide an overview of recorded system activity. Timing display emphasizes the duration of individual signals above or below threshold and allows rapid measurement of skews between signals of interest.

The analytic tools are editing, manipulating displays by use of expansion or by using cursors to limit or clip them, and the SEARCH and COMPARE functions. They combine some reduction with organization.

2.6.6 END RESULT

A recording and analysis session results in one of the following:

a. You have solved the problem and you finish the session.

b. You may have solved the problem and want to validate the proposed solution; you return to the logic analyzer with a set of procedures to do so.

c. You return to the problem with new insights and try other possibilities. You can return at any point in the grid.

2.7 **A FINAL WORD**

The purpose of this section was to give you a conceptual framework to help you make better use of the information in the rest of the manual. The following sections present many details about the K101-D and how these details relate to each other. After some practical experience with the logic analyzer, you will find that you develop your own useful building blocks of techniques, and that more details fall into place. Because of the wide range of techniques available to use with this powerful, general purpose analyzer, you will often find that several details are not relevant to your immediate task or application.

Keep in mind that during any one problem solving session with the K101-D, you will typically call upon only a few of the available capabilities.

After you have read more of this manual, and again after you have tried out some tasks with the K101-D, you may find it useful to return to this section and reacquaint yourself with some of this material. The general discussion and comparison of K101-D techniques and capabilities should take on deeper meaning as your knowledge of the logic analyzer increases. As you learn more about the K101-D, keep in mind the subcategories of general problem solving as a guide to your own learning: collect, reduce, and organize.

Section 3

DETAILED DESCRIPTION

3.1 INTRODUCTION

The K101-D Logic Analyzer is a microcomputer-controlled instrument (using the 16-bit Intel 8086), designed for digital circuit analysis and evaluation (see Figure 2-1). The operating system can accommodate up to 256 kilobytes of ROM and 128 kilobytes of RAM. Automatic power up diagnostics, extensive self-test diagnostics, and a probe test using an internal pattern generator are standard features of the K101-D.

This section describes the specific functions and capabilities of the K101-D and gives its detailed specifications. The next section (User Orientation) describes how the the front panel is used to operate the logic analyzer. These two sections complement each other; they cover the same material from two viewpoints: What the instrument can do, and How to tell it what to do.

3.2 DETAILED DESCRIPTION

The unit has 48 data inputs which feed a pipeline of three high-speed registers, each 52 bits wide (48 data bits plus 4 trace-level tracking bits). The user places the probes and specifies the conditions for recognizing signals from them. Data from the pipeline registers are evaluated for transfer to the actual trace memory M (which is 512 words of 52 bits each) according to the current conditional trace control specifications set by the user. The user controls every step in the data recording process: placement of probes, specification of threshold values, sampling and clocking conditions, and the interaction of control logic and trace control. The combination of features and capabilities

in this logic analyzer provides data capture with unprecedented versatility and precision for rapid isolation of essential information.

When the recording process is completed, the contents of trace memory M are transferred to display memory A. Memory A holds the last recording made. Memory B, equivalent in size, can hold a previously stored reference recording for comparison. Information stored in either memory A or B can be reviewed in various formats using either the Data, Graph, or Timing displays. The Data display, also called the "state display", best shows the detailed relationships of all relevent signals for each sample. The Graph display gives a visual picture of relative sample magnitudes over time, and the Timing display shows timing relationships of individual signals or groups of signals graphically. Many functional keys are provided for reviewing these displays. The user can isolate portions of the displays for special treatment, expand the displays, search and compare, and examine the actual data underlying any portion of a graphic display.

Input sampling is performed using either external, internal, or mixed clocking. Twelve separate external clocks (six sample clocks and six latch enables) can be combined, using menu-specified Boolean expressions, to obtain comprehensive samples for powerful software monitoring. The choice of a number of different internal sampling rates allows precise selection of the desired timing resolution needed for determining either signal pulse widths and skew measurements, or the window size (absolute time interval) captured by each recording.

Mixed clocking allows both external and internal sampling to be done simultaneously. Separate clocks may be defined for each of three sections of 16 data inputs (C, B, and A), or a single master clock may be used to sample all three sections at the same time.

The primary user interface to the instrument is a CRT display and a set of control keys. Each of the major setups for controlling trace

parameters, data formatting, input sampling, and communications is actuated by pressing one of the six SPECIFY keys, such as **CLOCK SELECT** or **TRACE CONTROL.** When a key is pressed, the currently selected specifications for that module are displayed on one or more CRT screen pages. This allows rapid review and modification of each module.

Changes to a screen menu are made by positioning a flashing cursor over the pertinent field and then entering the new specification. Specifications are easily entered. Most are selected from a group of possible entries using your choice of either the CHOICE keys (scrolling possible selections with **NEXT** and **PREV**) or the QUICK key method of entering a single digit. Other choices are made by pressing one of the direct entry keys in the GENERAL key area, such as **SAMPLE** or **GLITCH.**

In addition to front panel operation of the K101-D, it is also possible to operate the unit remotely, using communications lines. There are two fully programmable communications ports: the IEEE-488/1978 and the RS-232-C I/O interfaces. Key codes and data transfer formats allow the unit to be controlled from many common computers and terminals. These interfaces allow generation of hard copy, data logging, storage of common trace specifications, and automatic capture of intermittent system failures.

A third interface, an RS-449 port, is also included to give the K101-D the ability to communicate with intelligent peripherals and probing accessories. At present it is used to communicate with optional microprocessor execution disassembly modules. A fourth interface provides a standard video signal (RS-170 compatible) for connection to either a video monitor or printer.

Complimentary, ancillary measurement capabilities are built into the K101-D and include a real-time time-of-day (TOD) clock, a digital voltmeter (DVM) with 3-1/2 digit readout, and an external frequency

counter. These tools facilitate analysis of recordings, increase the convenience of use, and minimize reliance on other measurement systems.

Confidence in the unit's operation is ensured by three separate diagnostic tests: a comprehensive Power Up test, a Probe Test that provides a functional check on each probe (ten inputs at a time), and, when maximum confidence is desired, an exhaustive series of specialized tests that can be chosen using the Self-Test specification screen. These tests virtually ensure proper operation. If a problem does occur, the tests are designed to quickly find and isolate it. Down time is minimized and suspicious recordings can be easily checked by verifying proper operation.

The Probe Test uses a built-in pattern generator that makes it possible to learn a great deal about the K101-D by sending a known pattern to the probes, and then setting up various specification conditions and recording and analyzing the results. Section 10 of this manual presents a comprehensive discussion of how to use the Probe Test to learn about operating the logic analyzer.

3.3 SPECIFICATIONS

3.3.1 SIGNAL INPUTS

a. Number: Total of 60; 48 sample inputs and 12 clock inputs.

b. Input assignments: All inputs are assigned to one of three sections, labeled C, B, or A. Each section contains a group of 20 inputs: 16 sample inputs and 4 clock inputs split between two probe inputs. Each probe provides 10 inputs: 8 sample inputs and 2 clock inputs.

c. Input impedance: 1 megohm, 15 pF, over a range of $\pm$10 V.

d. Thresholds: Assignable for each group of 10 inputs; TTL (+1.40 V), ECL (-1.30 V), VAR A and VAR B (±9.99 V in 10 mV steps with 20 mV accuracy). Thresholds referenced to probe tip.

e. Polarity: Assignable positive or negative for each sample input.

f. Maximum voltage: ±50 V continuous, ±100 V transient.

g. Input modes: Selectable in groups of 8 or 16.

1. Sample: Sample mode is the most basic input mode. Inputs selected for the Sample mode are checked at, and only at, each active clock edge to determine their current logic levels. Clock edge is specified by the sample clock expression used for the pertinent sample input section. In Sample mode any glitches that occur between sample clocks are ignored.

2. Glitch: Glitch mode helps detect possible troublesome noise spikes. Any even number of threshold crossings between valid sample clocks is considered by the K101-D to be a glitch. This input mode is handled in the same way as Sample mode, except that the selected inputs are also monitored between every clock sample to determine if a glitch occurs.

3. Latch: Latch mode is a special case of Sample mode. It allows you to either hold or pass data to half or all the sample registers of each section (C, B, or A) based on the status of separately assignable, latch enable clock expressions. Latch mode lets you capture data at one time and then merge that data with other data sampled at

a later time, based on two separate clock expressions. The signals that indicate valid data can often be completely different in type and timing from those that indicate the right time to sample the data.

When the expression used for enabling the Latch mode is true, the associated inputs are sampled just as though Sample mode has been specified. When the expression is false, the states present at the moment the expression went false are held constant causing all samples of those inputs to be the same during that period.

4. Demultiplex: Demultiplex mode lets you capture data present at two different times on the same bus lines for simultaneous evaluation by the conditional trace control as one sample. Typically, one uses this mode to capture both address and data on a shared bus. In Demultiplex mode, the data inputs to the lower byte group of the selected section (C, B, or A) are buffered and then sent to both groups of that section. The lower byte group (0-7) is automatically placed in Sample mode and the upper byte group (8-F) in Latch mode. The enable clock expression defined for that section determines when and how the upper byte is sampled, just as in regular Latch mode. The sample clock expression for the section defines when the lower byte is sampled and also when the contents of the upper byte latch are examined. Both bytes are presented to the trace control simultaneously as one valid sample. The term "alignment" is sometimes used to refer to this simultaneous evaluation, capture, and display of two events which are separate in time.

3.3.2 CLOCKING SELECTION

In external and mixed clock modes, the K101-D allows external AND/OR clocking of sample and enable clocks for each data input section. A master sample clock strobes information from the sample registers into the unit's main memory M. Complex external clocking is keyboard selectable using menu-specified sets of Boolean expressions. Clocking combinations allow monitoring of multi-phased and multiplexed systems, as well as simultaneous time/data measurements.

3.3.2.1 **Sample Clocks**

a. Inputs: Total of six (two on the upper group (F-8) of each section). DC to 50 MHz external operation. Minimum pulse width for valid clock: 10 ns.

b. Operation: Sample clock active on rising edge. Clock is TRUE when all AND clocks are TRUE or when any OR clock is TRUE.

c. AND clocks: Up to three (CJ, BJ, AJ). User-specified logic level.

d. OR clocks: Up to three (CK, BK, AK). User-specified logic level.

3.3.2.2 **Enable Clocks**

a. Inputs: Total of six (two on the lower group (7-0) of each section). DC to 50 MHz external operation. Minimum pulse width for valid clock: 8 ns.

b. Operation: Resultant enable clock used when samples from a section (C, B, or A) are taken in Latch mode. When enable clock is TRUE, information passes freely through input latches

as in the Sample mode. When enable clock goes FALSE, data are held in the input latches until enable returns TRUE. Enable clock is TRUE when all three AND clocks are TRUE, or when any OR clock is TRUE.

c. AND enables: Up to three (CR, BR, AR). User-specified logic level.

d. OR enables: Up to three (CS, BS, AS). User-specified logic level.

3.3.2.3 **Clock Modes**

a. Internal extended: Provides 10 ns (100 MHz) data sampling and transfer to main memory M for one or all input sections. Control logic and other input sections (if 100 MHz sampling is not desired) are clocked using the slower internal clock (20 ns to 160 ms).

b. Internal: 20 ns to 160 ms. Selectable in a 1 through 16 sequence. All sample registers and control logic clocked simultaneously by internal clock.

c. External single-phased: DC to 50 MHz. All sample registers and control logic are clocked by the master clock.

d. External multi-phased: User may specify a separate sample clock for each section and for the master clock. All three sections transfer data into main memory M using the master clock.

e. Mixed single-phased: Master clock must be external. Sample clocks may be internal or external. External sample clocks must be same as the master clock. Internally clocked sections transfer data to main memory M using the internal clock.

f. Mixed multi-phased: Master clock must be external. Sample clocks may be internal or external. External sample clocks are specifiable separate from master clock but data are still transferred into main memory M using the master clock. Internally clocked sections transfer data to main memory M using the internal clock.

3.3.2.4 **Clock Setup and Hold Time Specifications**

Setup time is defined as the amount of time the information to be sampled must be stable prior to the active sample clock edge. Hold time is the amount of time the information must be stable after the active sample clock edge.

Hold time is usually a negative value. This means that the information may change exactly at, or even before, the clock edge, yet still be sampled as if it were stable all the way up to the clock edge.

These times result from the inherent propagation delay of the instrument's clocking circuitry and the difference between the delays of the various clock inputs. Conforming to these specifications will avoid any potential race condition problems and guarantee that your clocking equations will perform as expected.

a. **Individual Inputs.** The specifications for the individual clock inputs are given in Table 3-1. These times may also be thought of as a clock's minimum pulse width: the time between a nonactive and active edge.

Table 3-1. Clock Input Specifications

Clock	Setup Time (nsec)		Hold Time (nsec)	
	Max.	Typical	Max.	Typical
CK	8	5	0	0
CJ	12	9	0	-4
BK	8	6	0	-1
BJ	12	10	0	-5
AK	8	7	0	-2
AJ	12	11	0	-6

b. **Combined Inputs.** When two or more inputs are combined into a Boolean expression, additional specifications come into play. For two or three J inputs "ANDed" together, or for two or three K inputs "ORed" together, the required time interval between a particular edge on one input and a particular edge on another input is as shown in Table 3-2. The intervals T_1, T_2, and T_3 are graphically depicted in Figures 3-1 through 3-3. These are the minimum time intervals needed between the edges of your clock inputs for the resultant to be desired "ANDed" or "ORed" expression. The interval of 0 for T_1 means

Table 3-2. Setup Times for a Combination of Two or Three Clock Inputs

Interval	Max. Setup Time (nsec)	
	ORed	ANDed
T_1	0	0
T_2	4	12
T_3	12	4

Figure 3-1. T_1: Time From Active Edge on One Input to Active Edge on Another Input.

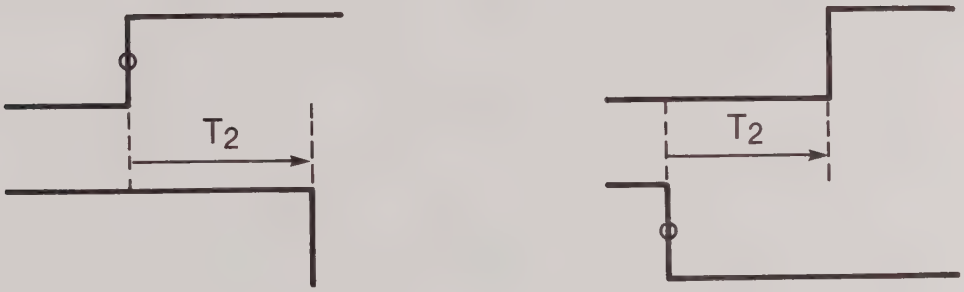


Figure 3-2. T_2: Time From Active Edge on One Input to Nonactive Edge on Another Input.

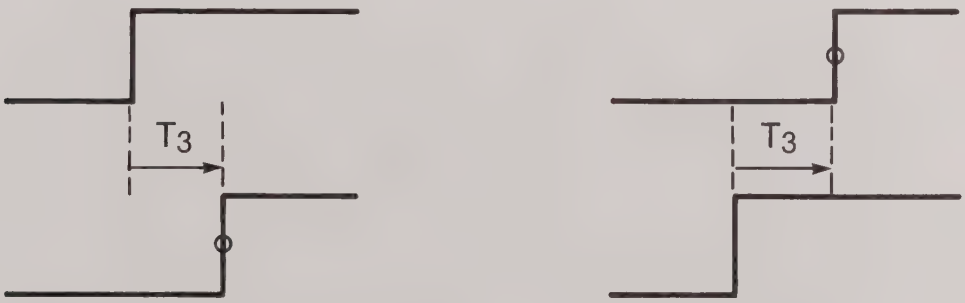


Figure 3-3. T_3: Time From Nonactive Edge on One Input to Active Edge on Another Input.

that T_1 can be any value and the resultant clock will toggle correctly, even if the two active edges occur simultaneously. If T_3 is less than its maximum specified time, then a desired resultant clock toggle (active sample edge) may not occur. If T_2 is less than its maximum specified time, then an unwanted resultant clock toggle (active sample edge) may occur. The previous specifications for individual clock input pulse widths still apply. When you use both J and K terms in an expression, add an additional 4 ns to T_2 and to T_3 for the "ORing" of the two sub-expressions.

Figures 3-4 through 3-12 illustrate the time intervals for all the possible AND, OR and active edge combinations of two similar clock inputs.

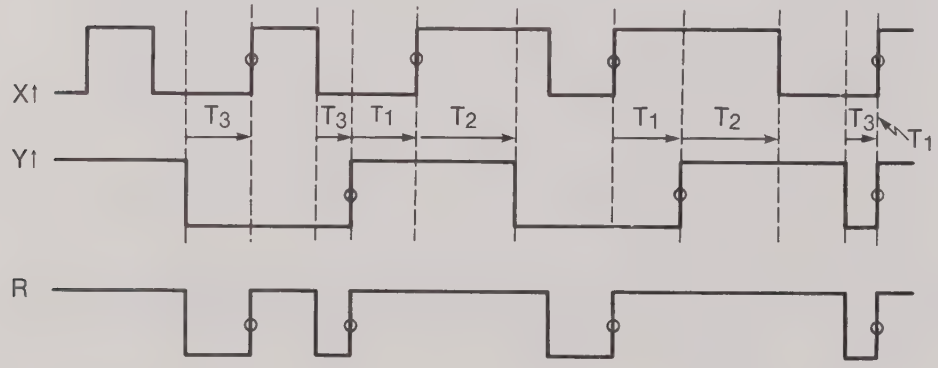


Figure 3-4. XK↑ + YK↑.

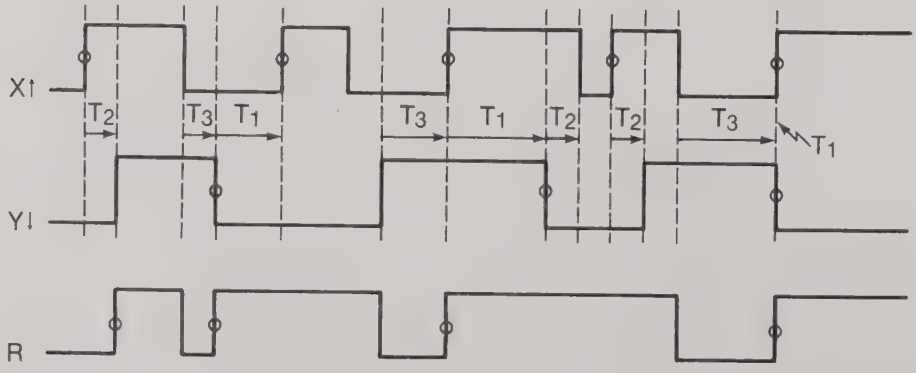


Figure 3-5. XK↑ + YK↓.

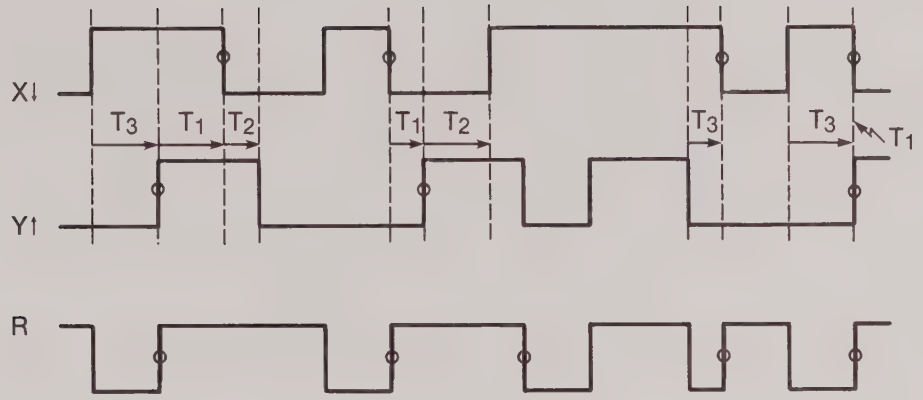


Figure 3-6. XK↓ + YK↑.

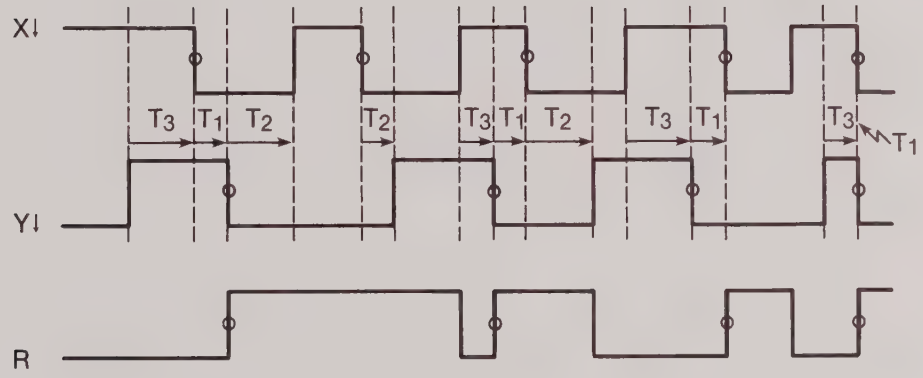


Figure 3-7. XK↓ + YK↓.

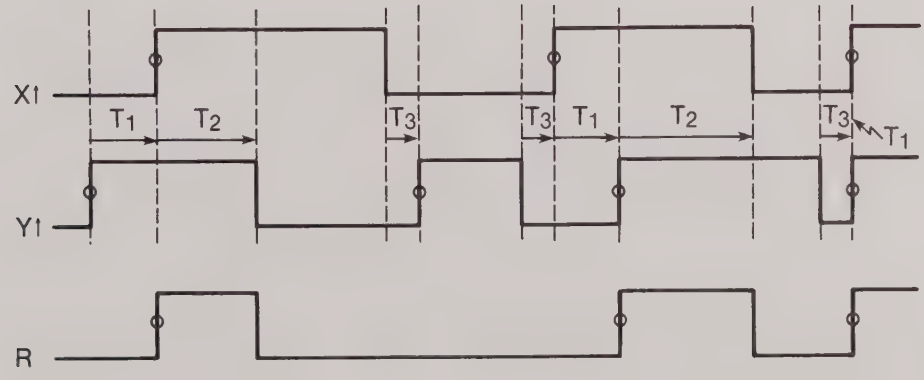


Figure 3-8. XJ↑ · YJ↑.

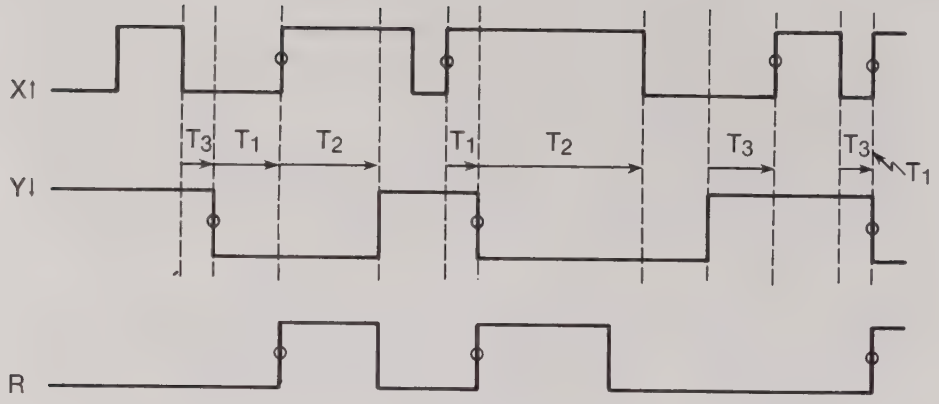


Figure 3-9. XJ↑ · YJ↓.

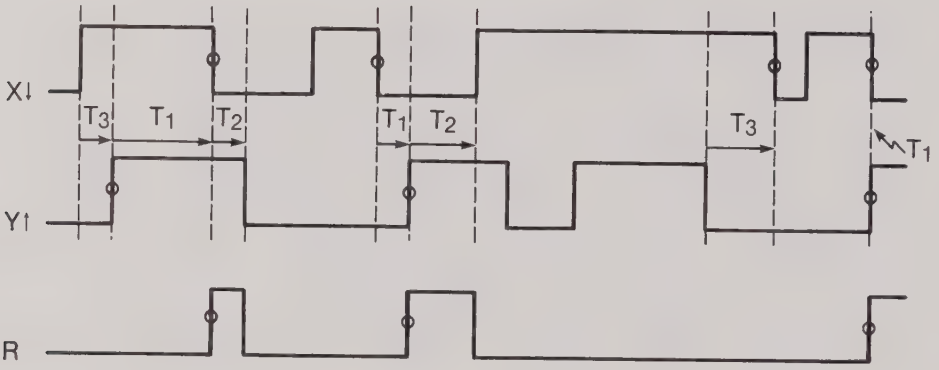


Figure 3-10. XJ↓ · YJ↑.

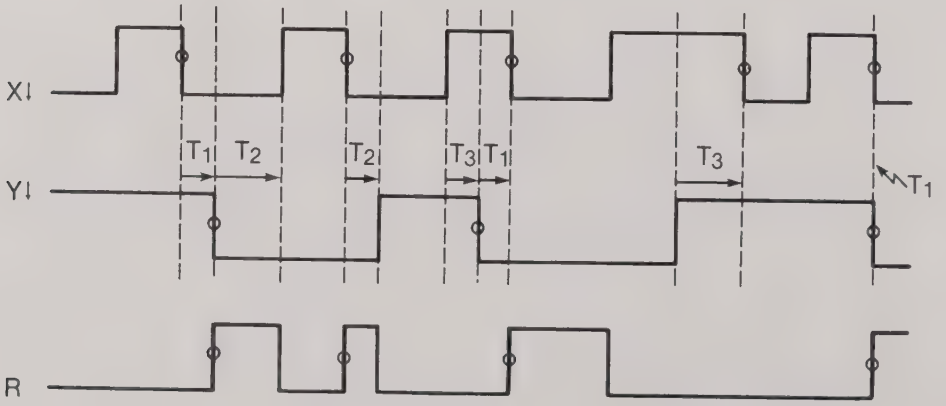


Figure 3-11. XJ↓ · YJ↓.

c. **Multiphase Clocking.** When using different master and section sample clock expressions, the active edge of a section sample clock must occur either 15 ns before the master clock active edge or 4 ns after it. This relationship must be true in order for the master clock to take a valid sample of a section's sample register contents. In other words, the master clock setup time is 15 ns, and its hold time is 4 ns (see Figure 3-12).

Although sampling should occur as specified, avoid specifying a section sample clock expression that is identical to the master expression. If possible, use a single-phase mode interval. this will prevent any potential master/sample setup or hold time problems.

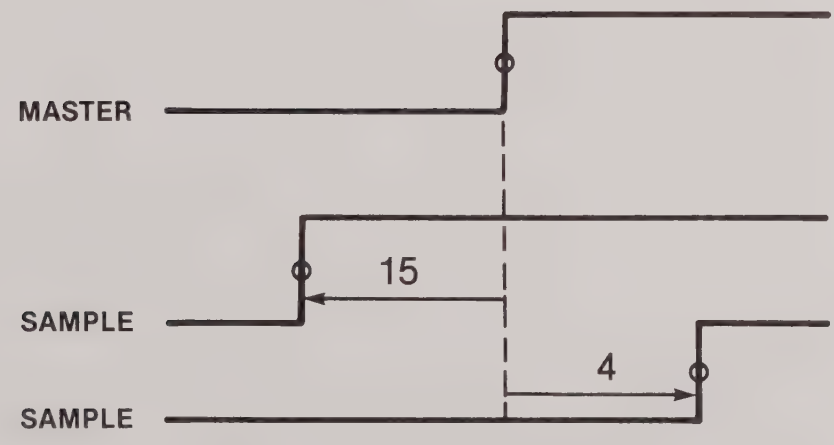


Figure 3-12. Master and Sample Clock Skew Requirements.

3.3.3 TRACE MEMORY

The K101-D contains high-speed main memory M, display memory A, and reference memory B.

a. Size: Memories M, A, and B are each 52-bits wide (48 bits for data inputs plus 4 bits for trace-level tracking) by 515-bits long (512-bits long plus 3 bits for pipeline data). In other words, these memories consist of 515 words of 52 bits each. Three words of memory M are used for pipeline data; 512 words are available for saving conditionally traced events.

b. Operation: Memory M accepts and transfers new information held at the end of each recording to memory A for display. Memory B is used as a reference and may be loaded from memory A, the keyboard, or the GPIB or RS-232-C interfaces.

c. Search: The unit accepts an up to 48-bit pattern through the Data Format display. The search pattern is independent of the original criteria which caused each 48-bit record to be saved. Either memory A or B can be searched.

On the display, each entry matching the search criteria is identified with an asterisk (*). The display also shows the memory addresses of the first and last occurrences and the total count. Pressing the **NEXT** key moves the cursor to each occurrence in sequence.

d. Compare: Memory A is compared to memory B. Differences are indicated by inequality (≠) signs on the data displays. The **NEXT** key moves the cursor to each occurrence, as with Search mode.

e. Edit mode: The user may enter or edit data in memory B using keyboard entry. This can be a useful tool for analysis in conjunction with the COMPARE function.

3.3.4 DATA FORMATS

The user defines data display characters. Multiple menu screens allow the specification of how all 48 signal inputs are to be shown. Each input signal, when captured, is either a one or zero. Signals can be shown as such (by choosing binary) or grouped with other signals and displayed as numeric values or characters. The user can specify either fixed formats or mixed formats. Fixed formats define all signals to be grouped as binary, octal, or hexadecimal characters. In mixed formats, these three radices and ASCII and EDCDIC can be used. Fixed formats are grouped in order by input signal; mixed formats are individually specified. Mixed formats allow an individual signal to be shown in more than one group.

Optional execution disassembly accessories are available for several specific microprocessors. These disassemblers format machine code into assembler operation codes and addresses, identify and display all memory and port activity, and highlight nonexecuted instructions when applied to prefetch-type microprocessors.

3.3.5 TRACE CONTROL

The trace control screens provide conditional trace control for capturing events, using up to 16 separately specifiable levels. The trace logic can move freely from one level of specification to another during a recording, so that information capture can be made dependent on an exact sequence of events or possibilites. This allows rapid review of long or disjointed execution intervals by providing the means for the precise definition of the information to be captured. With trace control you can investigate virtually all cause and effect relationships

and also benefit by very efficient use of memory space. Each level offers individual DELAY commands and conditional STOP, JUMP, ADVANCE, and TRACE commands. The priority of operations is STOP before JUMP, and JUMP before ADVANCE. TRACE is independent.

a. DELAY: Entered as decimal (1 to 65,535) or hexadecimal (1 to FFFF), for each of 16 trace levels. The sample count for DELAY is specifiable using either occurrences of the master clock or of the level's advance pattern. Whenever the trace logic enters a level, the sample count for the level is reinitialized.

b. STOP: Causes the tracing and recording process to stop. There are nine conditions: (1) Stop If Data = S, (2) Stop Always, (3) Stop Never, and (4-9) Stop If Data = S and Sample Count >, <, =, $\geq$, $\leq$, or <> ($\neq$) Delay. "S" may be any noncontradictory data pattern possible based on the currently specified data format. All variations of each specified character can be entered, including a "Don't Care" state. STOP has priority over JUMP and ADVANCE commands. A specified current trace will be made before the tracing process stops.

c. JUMP: Causes tracing to jump to a user-defined level (0-F) if specified conditional command comes true. This allows a change of conditions for tracing or can be used to reinitialize the sample count by jumping back to the current level. There are nine conditions: (1) Jump If Data = J, (2) Jump Always, (3) Jump Never, and (4-9) Jump If Data = J and Sample Count >, <, =, $\geq$, $\leq$, or < > ($\neq$) Delay. "J" may be any noncontradictory data pattern possible based on the currently specified data format. All variations of each specified character can be entered, including a "Don't Care" state. JUMP has priority over ADVANCE command. A specified current trace sample can still be taken as trace control jumps to the new level.

d. ADVANCE: Causes tracing to advance to next level of tracing (1-F) if the specified conditional command comes true. This allows a change of conditions for tracing. There are nine conditions: (1) Advance If Data = A, (2) Advance Always, (3) Advance Never, and (4-9) Advance If Data = A and Sample Count >, <, =, ≥, ≤, or < > (≠) Delay. "A" may be any noncontradictory data pattern possible based on the currently specified data format. All variations of each specified character can be entered, including a "Don't Care" state. A specified current trace sample can still be taken as trace control advances to the next level.

e. TRACE: Evaluates each valid sample to the specified trace conditions. There are nine conditions: (1) Trace If Data = T, (2) Trace Always, (3) Trace Never, and (4-9) Trace If Data = T and Sample Count >, <, =, ≥, ≤, or < > (≠) Delay. "T" may be any noncontradictory data pattern possible based on the currently specified data format. All variations of each specified character may be entered, including a "Don't Care" state. TRACE is independent of the STOP, JUMP, or ADVANCE operations. If the trace condition is met, the event will be put into memory. If the stop, jump, or advance condition is met, that operation will occur separately.

The combination of these conditions allows following various possible execution paths. For example, a trace control screen for level 3 might specify to advance (to level 4) under a particular condition and to jump to level 6 under another. By using such building blocks, a complex chain of interacting events can be followed and traced. Trace is independent of the other controls. For example, a set of eight level screens might be used to follow expected program flow without tracing, and four or five other level screens could be used to trace if the program got into unexpected areas.

3.3.6 ARM MODES

3.3.6.1 **Selections**

Selectable as Manual, Auto, Auto Stop, or Auto Stop Within Limits.

a. Manual: The user presses the **ARM** key, and the unit makes one recording and transfers the new data to memory A. If a stop condition is satisfied, the recording is made according to the trace conditions specified. It stops when the trace conditions reach a STOP operation.

b. Auto: The user presses the **ARM** key, and the unit begins the recording process. When the recording process reaches a STOP, the unit rearms itself and begins again. Each time it transfers new data to memory A. Pressing the **STOP** key or reaching the pass counter limit halts new acquisitions. The pass counter range is 1 to 9,999 cycles.

c. Auto Stop: The unit arms itself and acquires new data in memory A, which is compared with memory B. Conditions that can be specified to stop the unit from rearming and recording further are as follows: A=B, A≠B, or the pass counter reaching specified limit.

d. Auto Stop Within Limits: The comparison of memories A and B is limited to data between the unit's dual cursors inclusively, as specified in memory A. Also, only displayed data channels are compared. Conditions that can be specified to stop the unit from rearming and recording further are as follows: A=B Within Limits, A≠B Within Limits, or the pass counter reaching a specified limit.

3.3.6.2 **Acquisition Command Keys**

a. Arm: Initializes the control logic for all currently specified recording parameters and begins new recording, using the current Arm mode. If unit is already armed, pressing **ARM** still initializes the control logic and starts the recording process again.

b. Advance: Forces trace logic to unconditionally advance to next trace level. Recording process continues at next level just as though that level had been entered normally.

c. Memory M to A: Moves current contents of trace memory M to display memory A, and stops the recording process. The current contents of memory M will not include material from previous recordings since the memory is automatically flushed at the beginning of each arm cycle.

d. Stop: Stops the recording process and leaves contents of memory A intact.

3.3.7 DISPLAYS

The K101-D has a built-in, seven-inch diagonal raster scan CRT for display of all menus and data. There are three main types of displays: menu screens for specifying sampling and tracing of information, data display screens for analyzing recorded data, and a screen for entering interface specifications.

3.3.7.1 **Recording Specification Screens**

a. Input Modes: The user selects input modes in eight signal-input groupings (Sample, Glitch, Latch, and Demux). Threshold values and the arm condition are also selected on this display.

b. Logic Polarity: (+) or (-), assignable by user to each data input. Affects data display, graph display, trace control patterns, and the binary cursor readout on the timing display.

c. Clock Select: The user specifies clock mode and clock inputs using one of six menus.

d. Data Format: The user defines data display radices (octal, hex, decimal, binary, ASCII, or EBCDIC) for up to 48 inputs. Inputs may be in any sequence and may be repeated (that is, the same inputs may be shown in different character groupings as convenient).

e. Trace Control: The user defines trace control parameters for up to 16 levels, 0 through F.

3.3.7.2 **Recording Analysis Displays**

a. Data: Presents data up to 48 columns wide as determined by the currently specified Data Format display. When less than 24 columns are specified, the format is repeated to provide more data on the display; 24, 48, 72, or 96 samples can be displayed.

b. Timing: Shows simultaneous display of up to 24 timing waveforms. A total of up to 60 waveforms may be displayed by paging (six signals per page for ten pages). A user-selected label of up to seven characters can be entered as desired for each waveform. The user can rearrange the channel sequence of each page for convenient display. Vertical expansions of the display by 6, 12, and 24 can be specified. Horizontal expansions by 3, 6, and 12 can be specified. The display indicates the sample count between the Control Cursor and the

Reference Cursor. There is a binary logic readout of the Control cursor or the Reference Cursor position, whichever was used last.

c. Graph: Shows a dot graph of sample magnitude versus memory location (x, y). The user selects data inputs and the range of values to be graphed. The Reference Cursor and the Control Cursor delimit the vertical display. The horizontal expansion is the same as with Timing mode. Graph mode is useful for a quick overview of program execution.

3.3.7.3 **Interface Specification Screen**

The user can select GPIB (IEEE-488) or RS-232-C interface parameters. This screen also allows entry of time-of-day clock, date, or error beep status (enabled/disabled). The current software revision level is displayed.

3.3.8 AUXILIARY MEASUREMENTS

3.3.8.1 **Digital Voltmeter (DVM)**

Front panel IN and GND provide ±20 V range.

Resolution:	20 mV
Accuracy:	±0.5%
Input impedance:	20 kilohms

3.3.8.2 **Clock Status/Frequency**

Automatic measurement of external clock frequency.

Range:	100 Hz to 50 MHz
Accuracy:	0.1%

3.3.8.3 **Time of Day**

A 24-hour, time-of-day (TOD) clock is displayed in all modes. The end-of-acquisition time is captured for each recording. The time-of-day is retained by battery when power is off.

3.3.8.4 **Total Trace Time**

The total time that trace was enabled for each recording appears at bottom of the Timing Display. This allows precise measurement of time between any two events.

Resolution:	0.5 μ sec
Range:	00.00 μ sec to 1638.35 sec (27.3 min)

Note

Count resets to zero on overflows.

3.3.8.5 **Trace Level Tracking**

This allows the user to determine trace level reached during recording and to determine the level used to record each sample when reviewing recording.

a. Trace level: Shows current or last level reached during recording. Appears at bottom-right of all displays as "Level = n" (n is 0 through F).

b. Cursor level: Shows which level was used to record each sample. Appears just to left of trace level field as "CL = n" (n is 0 through F).

3.3.9 INTERFACES/REAR PANEL CONNECTORS

a. GPIB (IEEE-488/1978): Provides complete programmability via GPIB. Data and setup information are transferrable to and from either A or B memories. Using the GPIB interface, the K101-D can be made part of a system, produce hard copy or be operated remotely.

b. RS-232-C: A serial interface with capabilities similar to those of the GPIB.

c. RS-449: Allows unit to communicate with intelligent accessories. It is currently used for the optional RTE-816 microprocessor execution disassembly modules.

d. Trace output: TTL active high only while unit armed and current trace level is enabled.

e. Clock output: ECL active low signal corresponding to current internal master clock rate.

f. GET: Group execute trigger signal. Available via GPIB.

g. Video output: 1 V p-p into 75 ohm, RS-170-compatible levels. Used with compatible monitor or printer.

3.3.10 CONFIDENCE TESTS

a. Power Up: During power up, the K101-D performs checks of ROM, MPU, and CMOS RAMs, power supplies, and keyboard. Gives the user confidence that the instrument is operating properly.

b. Self Test: Allows user to select from a series of additional test routines for measurement validation or to serve as a

troubleshooting aid. The full set of self-test exercise routines is equivalent to in-house tests that are run to validate a unit before shipping it.

c. Probe Test: Allows user to test each probe (ten inputs at a time) with a built-in, ring-counter-type pattern generator. More than a simple test of probe functioning, the use of the pattern generator and various specification screens allows the internal operation of complex conditions for display, and therefore provides further validation of functions.

3.3.11 ACCESSORIES SUPPLIED

a. Probes: Set of six input probes with ten inputs each. Probes include flying leads and spring hook tips.

b. Manual: One operating and service manual supplied with each K101-D.

3.3.12 MISCELLANEOUS

a. Size: 21.8 cm high x 44.6 cm wide x 59.0 cm deep with bail (8.6" x 17.5" x 20.7").

b. Weight: 20 kg with probes (44 lb).

c. Power, internally selectable:

Nominal 115 VAC, 90-132 V RMS; 400 watt, 7 amp fuse.

Nominal 230 VAC, 200-268 V RMS; 400 watt, 4 amp fuse.

d. Temperature: 0 to 50°C operating range.

e. Battery back-up: Provides power for two setup saves plus TOD clock.

f. Accessory power: +5 V and -5.2 V, 300 mA total. Located at two rear panel LEMO connectors.

Section 4

USER CONTROLS AND DISPLAYS

4.1 OVERVIEW AND STRATEGY

You should be familiar with the features of the K101-D before you try to use the equipment for a specific application. This section describes the controls and default displays of the K101-D. It also includes suggestions that should assist you in becoming familiar with the instrument. Subsequent sections (5 through 8) discuss how to use the K101-D in actual applications. The familiarization process described in this section involves turning on the K101-D, using the controls, and observing the displays that will be shown on the screen of the CRT. Take the time to read the descriptions in this section before you try to connect the analyzer to a system.

The K101-D is both forgiving and robust: there is rarely any problem if you press the wrong key. After you power up, try using hunt-and-peck exploration to see what happens. When you are exploring the K101-D, don't worry about applying what you learn. That will come in later sections of this manual. For now, just explore. Get a general idea of how entries are made and how the various screens and entries relate to each other. The goal is for you to become familiar with the K101-D controls.

Section 10 (Probe Test) includes additional procedures that will assist you in operating the equipment. The K101-D incorporates two levels of self-test. When the K101-D is turned on (powered up), a short self-test is run automatically. A more extensive self-test routine can be initiated by the user. (The user-run routine will be indicated with initial caps: Self-Test.) This Self-Test program, which is described in Section 10, is the equivalent of the factory preshipment quality assurance test. This test will give you the same level of confidence in

the K101-D as if factory quality assurance or customer support personnel had checked out the instrument.

4.2 BRIEF DESCRIPTION OF KEYBOARD AND FRONT PANEL INPUTS

The K101-D front panel is shown in Figure 4-1. The key features of the panel are described in the following subsections.

4.2.1 PROBE CONNECTORS

Six connectors for probes are located across the bottom of the front panel. The connectors are grouped in sections of two probes each and labelled SECTION C INPUTS, SECTION B INPUTS, and SECTION A INPUTS. Each section can receive 16 sample inputs and 4 external clock inputs, for a total of 48 sample inputs and 12 external clock inputs.

4.2.2 CRT DISPLAY SCREEN

The screen is used to set up recording specifications and to display the results. The keyboard is used to specify and control the displays.

4.2.3 POWER, DVM, AND PROBE TEST

The POWER switch turns power on and off. The DVM sockets are used to access the digital voltmeter function when desired. The PROBE TEST socket provides pattern generation for the Probe Test.

4.2.4 KEYBOARD

There are 56 keys, most having multiple function (see Figure 4-2). They are used to specify and control the recording process and to display the results.

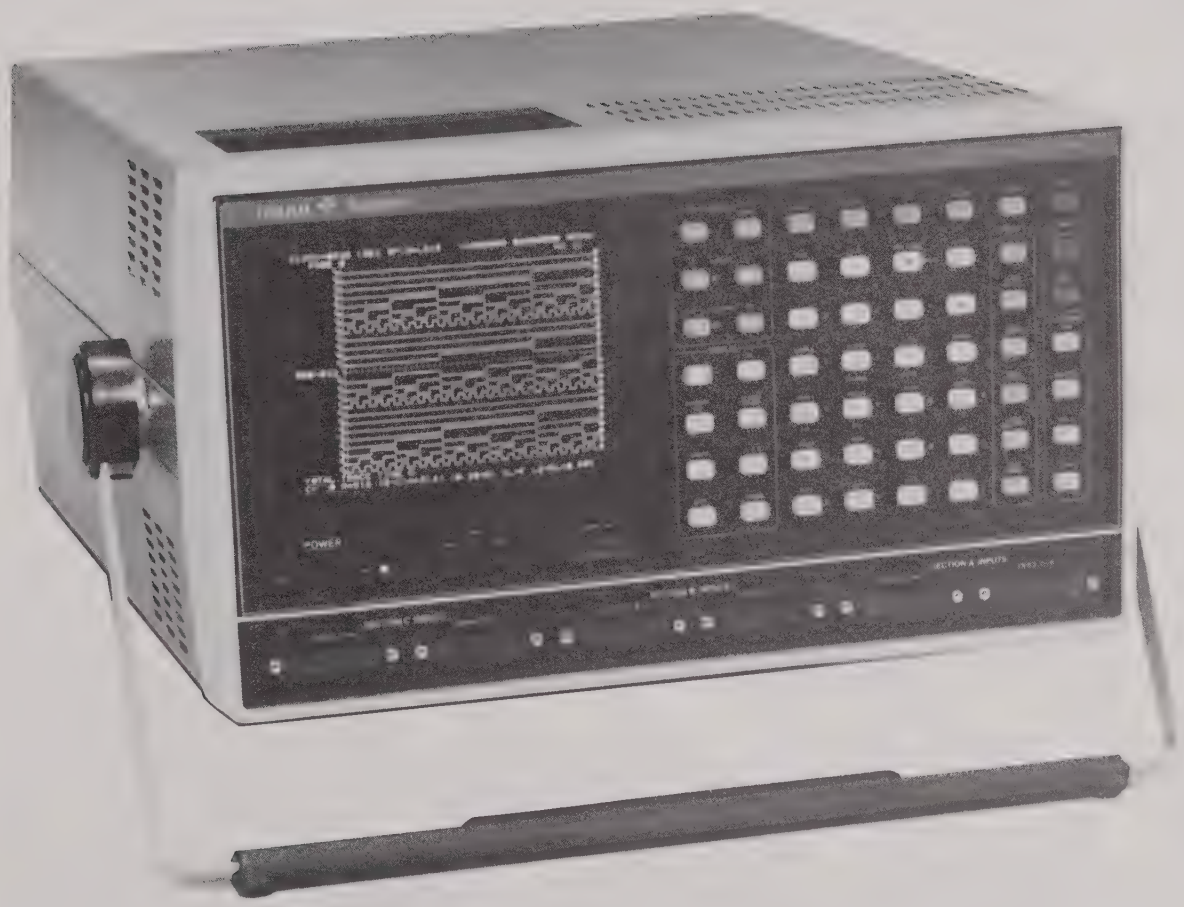


Figure 4-1. K101-D Front Panel.

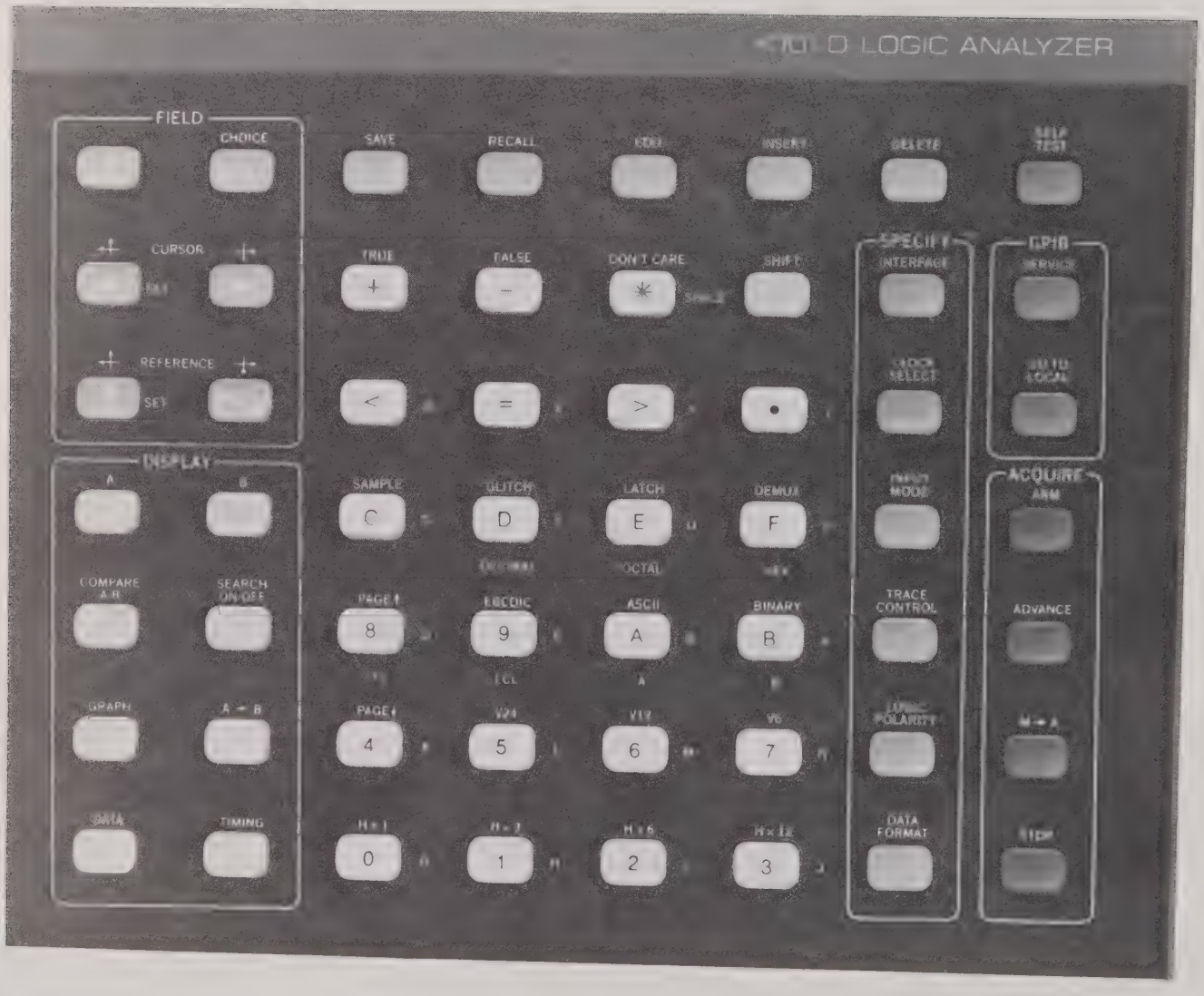


Figure 4-2. K101-D Keyboard.

4.2.5 POWER CHECK

The K101-D can be used with either 115 VAC or 230 VAC. Input voltage is set by a switch inside the unit. All units are factory set for 115 VAC line input.

Before powering up the unit, it may be necessary to change the input voltage selection switch. If a line voltage change is required, proceed as follows:

a. Remove the top cover.

b. Locate the input voltage selection switch in the rear quarter area, left-hand side of the instrument (as viewed from the front).

c. Move the input voltage switch to the desired setting (115 VAC or 230 VAC).

d. Replace the top cover.

e. Change the fuse (115 VAC, 7 amp fuse; 230 VAC, 4 amp fuse).

4.3 **POWER UP**

When you power up the K101-D, a beep will be heard and a short self-test program will start. The screen will be blank while the test is running. At the conclusion of the test, a second beep will be heard and a "RDY" indication will appear at the bottom right of the screen.

If the power up self-test indicates an error condition, refer to Section 10, which explains the meaning of self-test messages and the appropriate action to take.

4.4 USING THE KEYBOARD

This paragraph presents a general description of keyboard functions (refer to Figure 4-2). Keyboard details are presented in paragraph 4.5.

The displays are discussed in paragraph 4.6. You will find that the screen displays change when you use different keys. If you make an incorrect entry, the logic analyzer will beep. You can make use of this to try various entries, see the changes in prompt messages and possibilities, and test possible responses.

As shown in Figure 4-2, the keyboard of the K101-D can be divided into the following groups: FIELD, DISPLAY, SPECIFY, GPIB, ACQUIRE, and GENERAL.

Five of the groups listed are outlined and labelled on the keyboard. The GENERAL area is not labelled as such on the keyboard.

4.4.1 FIELD KEYS

The FIELD group contains arrow keys for moving cursor and selection keys for specifying choices. In the setup screens, arrow keys move the cursor from one entry field to the next, and the selection keys can then be used to specify a choice of possible entries for a field. In the display screens, used for showing recording results, arrow keys are used to position two cursors that are used in working with displays, the Control Cursor and Reference Cursor.

4.4.2 SPECIFY KEYS

The SPECIFY keys, as well as the ACQUIRE and DISPLAY keys discussed below, are used to set up recording conditions, control the recording process, and analyze the results. The six SPECIFY keys have associated setup screens. Entering values in these screens specifies the entire

sampling process. Specifications include the probe polarity and threshold values, the clocking and inputting conditions for sampling probe inputs, how the recording process will be controlled, and the data display format.

4.4.3 ACQUIRE KEYS

The ACQUIRE keys control the recording process. One key starts the process and other keys can stop the recording or intervene and force the tracing process to move to the next level.

4.4.4 DISPLAY KEYS

These keys are used for displaying and analyzing data in the display memory and the reference memory. Data can be displayed in graphic form, as state data, or as timing diagrams. Either memory can be searched, or the two can be compared and the results displayed. One of these keys controls the transfer of display memory to reference memory.

4.4.5 GPIB KEYS

These keys perform certain optional control and communications functions. They start and end both GPIB communications and RS-232 communications.

4.4.6 GENERAL KEYS

At the top of the GENERAL key area is a line of action keys, colored blue. These keys are used to save and restore the contents of setup screens, to edit display and reference data, and to run the Self-Test.

The white keys have multiple functions, all used for data entry.

Data entry keys include numbers **0-9** and letters **A-F**, which are used for setting many values. The ASCII keys, shown as yellow letters, are

available when using the (yellow) **SHIFT** key. They are used in certain data formatting and can be used for labelling channels in the timing display.

Numeric keys can also be used as "quick keys." Specification choices can be made by number as well as by using the CHOICE keys in the FIELD area.

In addition to the face designation, these keys have other direct entry functions that are dependent on the context. The other direct entry designations, when present, are shown above and below the key.

For many of the setup screens, choices are entered directly by pressing one of these keys. For example, when specifying the input mode, pressing the **SAMPLE** key selects the Sample mode. In a different context, pressing this key would enter a "C."

4.5 KEYBOARD DETAILED DESCRIPTION

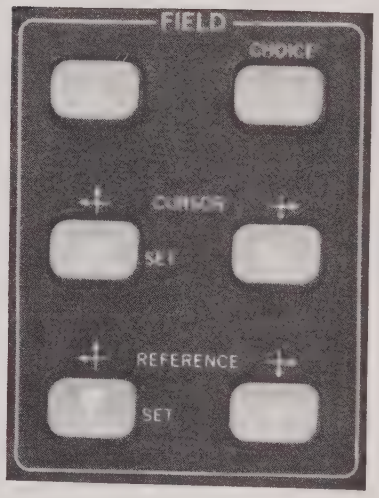
The keys are described by area. Since different areas can interact, cross references are given within the descriptions as necessary.

In general, when looking at a choice of entries for a given field, there is no harm in trying a likely key. If the choice is illegal, the K101-D will beep and you can try another entry.

4.5.1 FIELD KEY AREA

The FIELD area contains keys for moving about in the fields of the setup screens and for positioning the cursors in the display screens. For the setup screens, many entry fields can be programmed by using the CHOICE keys (**NEXT** and **PREV**) to step through the available choices.

4.5.1.1 **Arrow Keys**



The four keys with an arrow on the face move the cursor up, down, right, and left, into data entry fields of the screens. When the cursor is positioned in an entry field, the field blinks to show it can be modified as appropriate. Depending on the field, the modification may be made by directly entering data or by using either the CHOICE keys or the "quick key" method, explained below. These keys may also be used to position the nonblinking reverse video cursor and to edit timing, data, or graph displays.

The cursor used to select fields is sometimes called the Parameter Cursor to distinguish it from two other cursors that will be discussed later, the Control Cursor and the Reference Cursor.

4.5.1.2 **CHOICE Keys**

The **NEXT** and **PREV** keys are called the CHOICE keys, and are used to select among alternate, predefined specifications. For example, in setting trace conditions, there are nine predefined conditions for tracing: "Trace Always," "Trace Never," "Trace if T = XXX....," and so on. Placing the cursor in the trace condition field accesses the first condition. Pressing **NEXT** accesses the next. Continuing to press **NEXT** accesses the next eight in order.

Pressing **PREV** accesses the previous entry. **NEXT** and **PREV** wrap around: the **NEXT** key moves the cursor from trace condition eight to trace condition zero. Similarly, the **PREV** key will move from the first trace condition choice to the last.

4.5.1.3 **QUICK Keys**

The QUICK keys, which are alternatives to the use of the CHOICE keys, are in the GENERAL area. They are the numeric keys (**0-9**) used in conjunction with the FIELD keys. When the cursor is positioned in a specification field where a CHOICE key can be used, a numeric key can also be used to give direct access to a choice by number of entry. For example, when the cursor is positioned to make a trace selection, pressing **7** will immediately access the seventh trace condition entry.

4.5.1.4 **Control Cursor and Reference Cursor Arrow Keys**

Four keys are shown with arrows above them. They are used in a fashion similar to the FIELD keys, but instead of moving about in entry fields, they are used to move about in the graphic, timing, or data display screens. (Data display is also called "state" display.) The two keys labelled CURSOR control the control cursor; the two labelled REFERENCE control the reference cursor. The cursors can be sequentially scrolled through the memory locations or sent immediately to a specific location.

The Control Cursor can be used to specify an area for detailed attention. The Control Cursor and Reference Cursor can be used in combination to define a particular area of the displays for special attention. For each pair of keys, one has arrows indicating up and left, and the other down and right. The action depends on whether the timing display, graphic display, or the data display is showing. Left and right pertain to timing and graphic displays, and up and down to data displays.

The effect of these cursors depends on whether the logic analyzer is displaying in graphic, timing, or data mode. In data mode, the cursors move vertically among the recorded entries. When a compare or search operation has been completed, the Control Cursor moves from one tagged

entry to another. The control and reference cursors together can be used to specify a group of entries for special use in automatic compare and control operations.

In graphic or timing mode, the cursors are dotted vertical lines that move horizontally. The state data associated with the display at the location of the Control Cursor are also displayed on the screen. The two cursors together can be used to specify a group of entries for special use.

The location of the two cursors is shown at the bottom of the screen, indicated by C for Control and R for Reference. The screen display for timing or graphic display adjusts so that if the display is expanded vertically or horizontally, the Control Cursor is always in the display area; the Reference Cursor may not be.

4.5.2 SPECIFY KEY AREA

The six SPECIFY keys have associated setup screens. On the display screen, the menu title is shown at the top of the screen under the GPIB information. These menus are explained below, in the following order: Interface, Clock Select, Input Mode, Trace Control, Logic Polarity, and Data Format.

4.5.2.1 **Interface**

The Interface screen allows the user complete manipulation of the GPIB and RS232 interface parameters. The time and date for the real time clock can also be set, using data entry keys from the GENERAL area. The CHOICE keys or the QUICK keys are used to choose from the groups of entries shown below, and direct entries for the others. GPIB entry possibilities are presented in Table 4-1.

Table 4-1. GPIB Entry Possibilities

Mode:	End Chars:	By direct entry:
Listen Only	CR	Date specification
Address = nn	CR + EOI	Time specification
Talk Only	CR/LF	Command = any valid instrument command
	CR/LF + EOI	

"Address = nn" value is entered directly.
Command used only with Talk Only mode.

RS232 Entry Possibilities:

Baud rate =	110	600	2400
	150	1200	4800
	300	1800	9600
Stop bits =	1		
	2		
Parity =	ODD		
	EVEN		
	NONE		
Word length =	7 bits		
	8 bits		
Protocol =	NAK/ACK		
	CTS/RTS		
Command =	Any valid instrument record		

Note: This screen also allows suppression or activation of the error beep, and indicates what level or revision of software is in the instrument.

4.5.2.2 **Clock Select**

The Clock Select menu is used to set up the correct clocking arrangement for a particular case. The CHOICE or QUICK keys can be used to step through the groups of entries, and data keys for variable entries. Clock entry possibilities, which change according to the basic specification, are summarized in Table 4-2.

Table 4-2. Clock Entry Possibilities

a. Clock Mode Menus:

Internal	Mixed Single-phased
External Single-phased	Mixed Multi-phased
External Multi-phased	Internal Extended

b. Internal Clock Period: 10 ns to 160 ms

c. Clocks

Possible clocks depend on mode. Categories are Master, Sample, and Enable. There are six possible entries for each, with each clock entry specified as active high, active low, or not used.

Master and Sample

$(CJ \cdot BJ \cdot AJ) + (CK + BK + AK)$ $\cdot$ = AND + = OR

Enable

$(CR \cdot BR \cdot AR) + (CS + BS + AS)$

4.5.2.3 **Input Mode**

The Input Mode screen selects the threshold values for signals, the Input mode for accepting data, and the "Arming" mode, which specifies how the recording process will proceed. Input Mode entry possibilities are presented in Table 4-3.

Table 4-3. Input Mode Entry Possibilities

Input modes:	Sample*
	Glitch*
	Latch*
	Demux* (Xf - X8 only; X = A, B, OR C)
Threshold:	TTL*
	ECL*
	VAR A ±9.99 V
	VAR B ±9.99 V

Threshold values are assignable by probe. VAR A and B are specified by direct entry of the **A** or **B** keys. Their numeric values are specified by direct entry.

Arming:	Manual
	Auto
	Auto stop if A=B
	Auto stop if A≠B
	Auto stop if A=B within limits
	Auto stop if A≠B within limits
Pass count limit:	0 - 9999 (direct entry)

The arming specifications are made by CHOICE keys or QUICK keys. Arming limits are set by Control and Reference Cursor locations.

---

*These keys are direct entry keys in the GENERAL area.

4.5.2.4 **Trace Control**

Sixteen separate conditional trace control levels are available, each with its own menu screen numbered 0 through F. Each level has four conditional commands: STOP, JUMP, ADVANCE, and TRACE. The execution of each command within a control level can be made conditional to a uniquely defined data pattern (of up to 48 bits) and a delay count. The bit pattern corresponds to the probe signals, as conditioned by input modes, clocking, and threshold setting.

Rather than simply finding a single specific area in a program for recording, the K101-D can use the trace control specifications to actually follow the program flow through the system under test. The instrument can trace through complex data paths, recording many precisely defined portions of the program flow along the way.

The data pattern at the top of the screen is set using the Data Format menu. Trace Control menu data entry possibilities are presented in Table 4-4.

4.5.2.5 **Logic Polarity**

The Logic Polarity menu allows the user to specify negative or positive convention logic on any of the 48 sample inputs from the probes. The Logic Polarity entry possibilities are

Polarity Positive (+) or Negative (-)

Entries can be set by either the CHOICE keys or **+ (TRUE)** and **- (FALSE)** keys in the GENERAL area.

Table 4-4. Trace Control Entry Possibilities

Level:	16 levels, 0 to F, entered directly
Delay:	Specified either in decimal or hex. Counted as either occurrence of master clock cycles or of that level's specified advance pattern.

DECIMAL and **HEX** are direct entry keys. Delay is entered using the numeric/hexadecimal keys. The maximum delay is hex FFFF, equivalent to 65,535.

Clocks A Patterns:	CHOICE key or QUICK key
End Level Conditions:	0 to F, entered directly

Conditions are set for STOP, JUMP, ADVANCE, and/or TRACE. Conditions are chosen using the CHOICE or QUICK keys. Some choices involve matching a pattern. The pattern is keyed to the data display at the top of the screen, which is specified by the Data Format menu, also in the SPECIFY area. The pattern to match is specified to fit the designated format, using direct entry keys and the **DON`T CARE** key.

Stop conditions:	Stop if data = S Stop always Stop never Stop if data = S and sample count > delay Stop if data = S and sample count < delay Stop if data = S and sample count = delay Stop if data = S and sample count ≥ delay Stop if data = S and sample count ≤ delay Stop if data = S and sample count <> delay
Stop pattern:	S = XXXX XXXX XXXX XXXX
Jump conditions:	Jump to L* if data = J Jump to L always Jump to L never Jump to L if data = J and sample count > delay Jump to L if data = J and sample count < delay Jump to L if data = J and sample count = delay Jump to L if data = J and sample count ≥ delay Jump to L if data = J and sample count ≤ delay Jump to L if data = J and sample count <> delay

*Note: L is level 0 to F

Table 4-4. Trace Control Entry Possibilities (Cont'd)

Jump pattern:	J = XXXX XXXX XXXX XXXX
Advance conditions:	Advance if data = A Advance always Advance never Advance if data = A and sample count > delay Advance if data = A and sample count < delay Advance if data = A and sample count = delay Advance if data = A and sample count ≥ delay Advance if data = A and sample count ≤ delay Advance if data = A and sample count <> delay
Advance pattern:	A = XXXX XXXX XXXX XXXX
Trace conditions:	Trace if data = T Trace always Trace never Trace if data = T and sample count > delay Trace if data = T and sample count < delay Trace if data = T and sample count = delay Trace if data = T and sample count ≥ delay Trace if data = T and sample count ≤ delay Trace if data = T and sample count <> delay
Trace pattern:	T = XXXX XXXX XXXX XXXX

4.5.2.6 **Data Format**

The Data Format menu is used to arrange the input signals of the logic analyzer for display. The formats specified here are used for reference in the Trace Control menu.

During recording, individual input signals are evaluated as being zero or one according to the criteria set up in other specify menus. The formats set in this menu specify how those signals are to be grouped in the state data when displaying recorded information.

The data format does not control data capture. If signals are eligible for capture (connected), they are recorded. Display definition can be changed after capture in order to see the recording in a different manner.

The Data Format menu can also be used to specify a pattern for use with the **SEARCH ON/OFF** key (one of the DISPLAY keys). Data Format entry possibilities are

Hex	Mixed user
Octal	Mixed CF-A0 sequence
Binary	Device Mnemonics (if available)

These formats are specified by direct entry (GENERAL) keys. The first three formats, and last, are fixed formats. Input signals are grouped in order from CF to A0. Four signals form each hexadecimal character, three for octal, and one for binary.

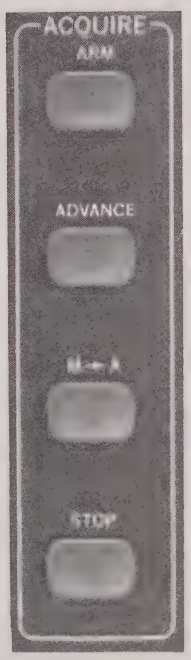
The two mixed formats allow combining any of five formats (hex, octal, binary, ASCII and EBCDIC). Mixed user provides fields for specifying the input signals.

For the mixed user format, when an entry is made, the corresponding area below it is open for specification of the input signal, CF to A0. These entries are made by direct entry of the keys **0-9** and **A-F**. Signals can be grouped or ignored as desired. The same signal can be used in more than one display.

Search patterns are entered in the same manner. The mode is selected in the same way, because the search screen changes its pattern at the same time as the main screen. When the cursor is moved into the search menus, the pattern is entered in the manner described for the main screen. Also, **DON'T CARE** may be specified as an input.

Disassembler mnemonics are available only when the K101-D is used in conjunction with an RTE-816 real-time execution disassembler. These are available for various microprocessors. The signals from the specific RTE microprocessor are automatically formatted in the most useful grouping for that microprocessor and translated into its assembler mnemonics. The RTE, after loading, also automatically specifies the required logic polarity, threshold values, input mode, and clocking for its microprocessor.

4.5.3 ACQUIRE KEYS



These keys control the actual recording process. The conditions for recording are set up using the Input Mode screen in the SPECIFY area. The choices are shown under "Arming."

4.5.3.1 **ARM**

The **ARM** key initiates the recording process, whether recording is in Manual or Automatic mode.

4.5.3.2 **ADVANCE**

The **ADVANCE** key can be used to force the trace control level to advance during a recording. Usually, this would only be done if the trace did not advance because of the trace condition logic. This function is useful when the assumptions made in the trace level advance specification do not work, and allows the attempt to capture data at other levels.

4.5.3.3 **M->A**

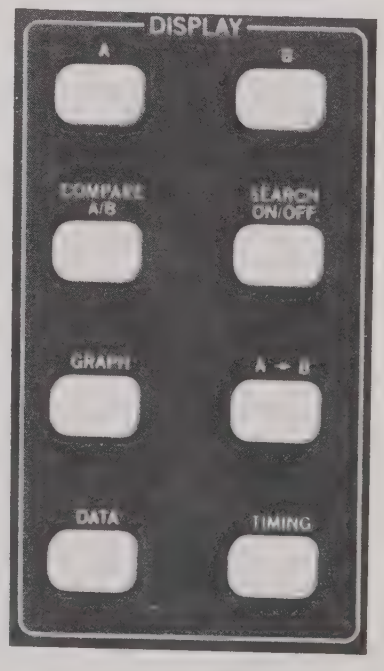
The **M->A** key stops the recording process and transfers the contents of high speed memory to display memory, including the setup information for the screens.

4.5.3.4 **STOP**

The **STOP** key stops a recording in progress, without transferring the contents of high speed memory. It allows the recording process to be aborted without changing a prior recording.

4.5.4 DISPLAY KEYS

The DISPLAY key menus are used after the recording has been made to review and analyze the recording. They select the Data, Timing, or Graph displays for viewing, and provide functions for manipulating the display and reference memories.



4.5.4.1 **A**

The **A** key specifies that the contents of the display memory are to be viewed.

4.5.4.2 **B**

The **B** key specifies that the contents of the reference memory are to be viewed.

4.5.4.3 **COMPARE A/B**

The **COMPARE A/B** key allows the user to compare the contents of A and B memory. It is a toggle key, and sets compare on or off.

Example: Comparison results appear at the bottom of the CRT, such as:

Total ≠ = 20 First ≠ = Ø Last ≠ = 450
All unequal samples are marked with ≠

Pressing **NEXT** moves the Control Cursor from the first unequal entry to each successive unequal entry.

4.5.4.4 **SEARCH ON/OFF**

The **SEARCH ON/OFF** key is another toggle key. Before setting search on, the user must first enter the search pattern. This is done with the Data Format menu in the SPECIFY area. Pressing **NEXT** moves the Control Cursor from one entry to the next.

Example: Comparison results appear at the bottom of the CRT, such as:

Total * = 1 First * = 350 Last * = 350

4.5.4.5 **GRAPH**

The **GRAPH** key sets Graph mode, and causes the K101-D to plot the magnitude of specified inputs versus time or memory locations on the horizontal axis. Either A or B memory can be plotted, according to whether the **A** or **B** key was pressed.

a. For horizontal expansion: press the appropriate keys (**H x 1, H x 3, H x 6, H x 12**).

b. For vertical expansion: press **EDIT**, then enter the upper and lower data limits. Then press **GRAPH**.

The horizontal expansion keys are direct entry keys in the GENERAL area.

4.5.4.6 **A->B**

The **A->B** key simply transfers the contents of A memory to B memory. It is one of three ways to put contents in reference memory B. The other two are direct keying in Edit mode or by communications.

4.5.4.7 **DATA**

The **DATA** key allows the user to view the recorded data as state data, in the format chosen with the Data Format menu (either in the A or B memory).

4.5.4.8 **TIMING**

The **TIMING** key displays an actual timing diagram of the recorded data from either A or B memory.

a. Each timing waveform may be labelled or rearranged by pressing the **EDIT** key, moving the waveform cursor, and using any of the ASCII characters and numbers in the GENERAL area, or may be removed with the **DELETE** key.

b. Vertical expansion: **V24, V12, V6.**

c. Horizontal expansion: **H x 1, H x 3, H x 6, H x 12.**

d. Since only 24 lines of timing can be displayed at one time, the **PAGE UP** or **PAGE DOWN** keys can be used to view the other channels.

Note

The **EDIT** key, the vertical and horizontal expansion keys, and the ASCII keys are all in the GENERAL key area.

4.5.5 GENERAL KEYS

The GENERAL keys are shown in Figure 4-3. The top row of blue keys are used for memory and data manipulation. The white keys have multiple functions as discussed later in this section.

4.5.5.1 **Blue GENERAL Keys**

The blue GENERAL keys are used to save and restore the contents of setup screens, to edit display and reference data, and to run the Self-Test.

The **SAVE** and **RECALL** keys are used for storing and retrieving user-selected menu setups.

Pressing **SAVE** stores the contents of all the setup screens; pressing **RECALL** restores the saved contents for the screens.

Pressing **SHIFT** and then pressing **RECALL** restores all screens (except Interface) to their default setups -- that is, the standard setups provided by the factory. **SHIFT, RECALL** does not change stored information, which may still be recalled.

When the K101-D is turned off, it saves all screen information and restores it when turned on. (There is an exception: If the Timing display sequence has been changed, the changed order is not saved. Timing labels are saved and restored, but the original sequence (CF-A0) will replace the changed sequence.)

The **EDIT** key is used to edit the contents of reference memory B for display or comparison. The EDIT function can be used to create idealized graphic, timing, or data displays, or to remove irrelevant information. In the Data display, **INSERT** and **DELETE** keys are used to insert and delete entry lines. The data entry keys are used for

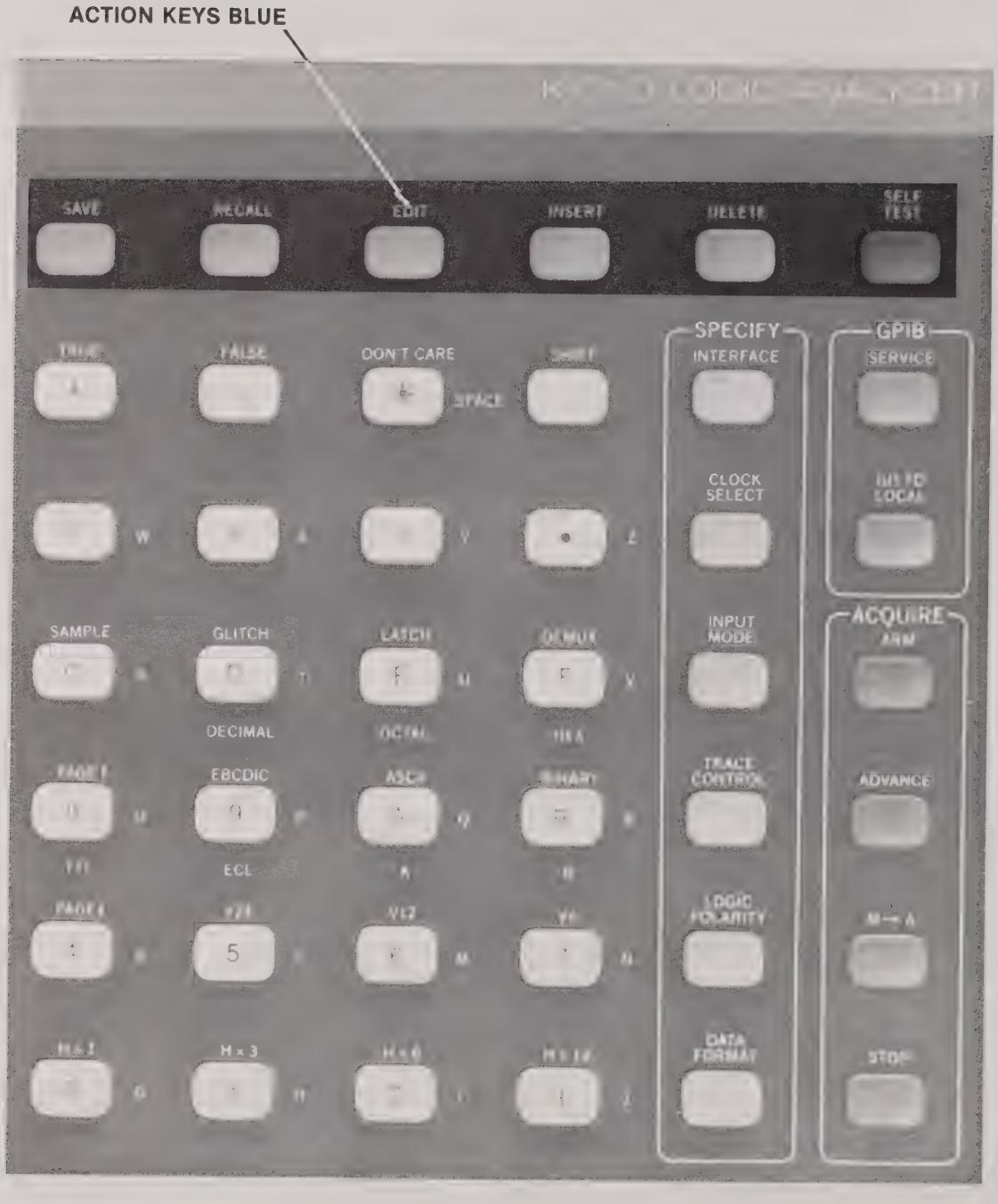


Figure 4-3. GENERAL Area Keys.

character-by-character replacement and for entering inserted lines. In the Timing display, **DELETE** is used to remove entries.

EDIT is also used to adjust the Graph display, as described above under the DISPLAY keys. It is used to provide labels for the timing diagrams, also described in the DISPLAY keys section (under "Timing").

The **SELF TEST** key resets the K101-D and performs a menu-oriented diagnostic check. Press **SHIFT**, then **SELF TEST** to access an extensive series of tests to check system confidence. The Self-Test is explained in Section 10.

4.5.5.2 **Data Entry Keys**

The white, multiple-function data entry keys are presented graphically in Figures 4-4 through 4-14.

The numeric keys (Figure 4-4) are the numbers **0-9**. These keys are used with many different functions. Some of the subsequent figures in this section reference the numeric keys shown in Figure 4-4. The hexadecimal keys include these numbers and the letters **A-F** (see Figure 4-5). The designations of these keys are on the face of the key. Wherever a numeric or hexadecimal entry is needed, the information shown in Figures 4-4 and 4-5 applies.

Numeric keys can also be used as QUICK keys (see Figure 4-4). Specification choices can be made by number as well as by using the CHOICE keys in the FIELD area.

The ASCII keys, shown as yellow letters, are available when using the (yellow) **SHIFT** key (see Figure 4-6). The ASCII keys are used with

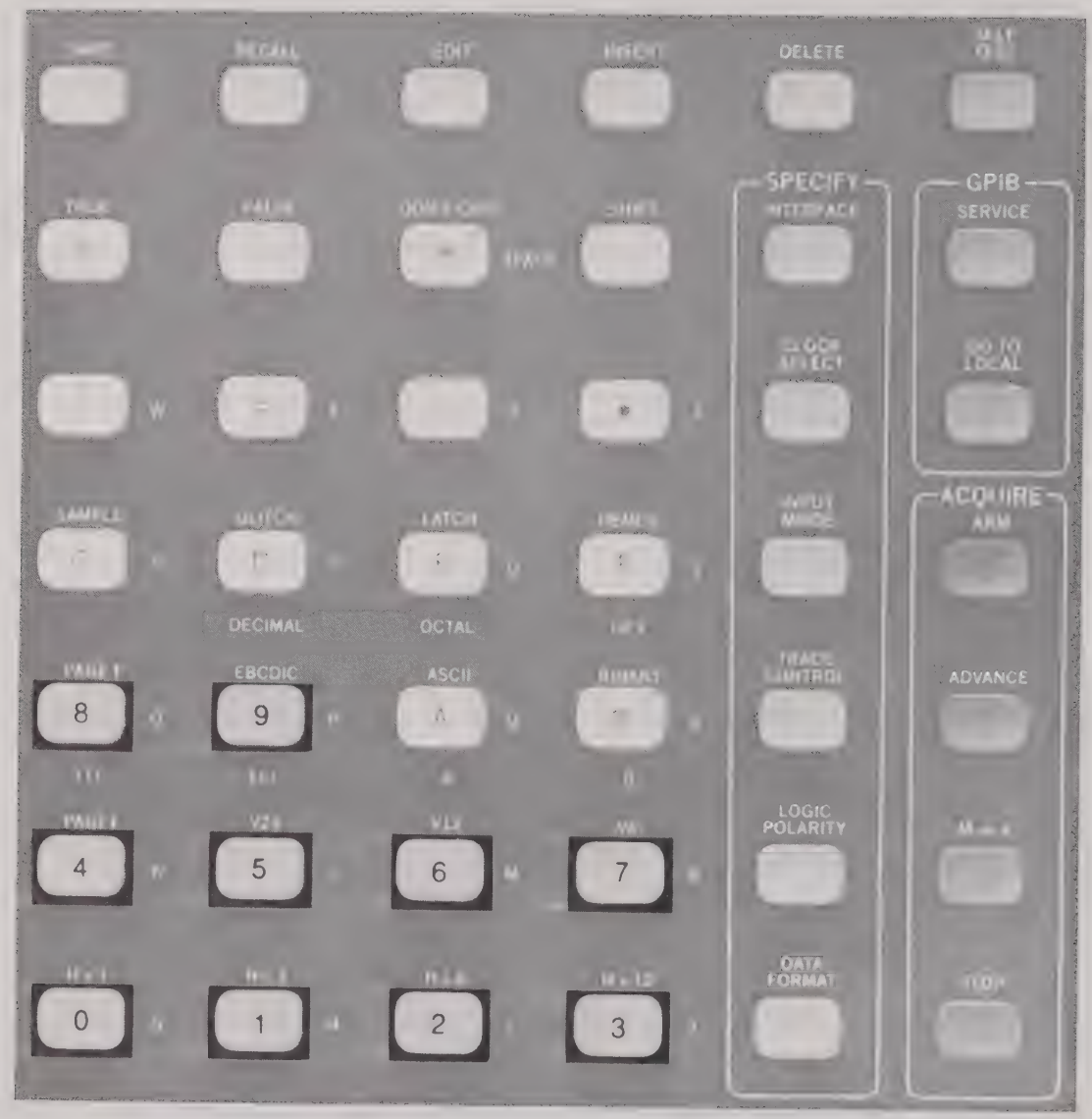


Figure 4-4. Numeric Data and QUICK Keys.

Figure 4-5. Hexadecimal Keys.

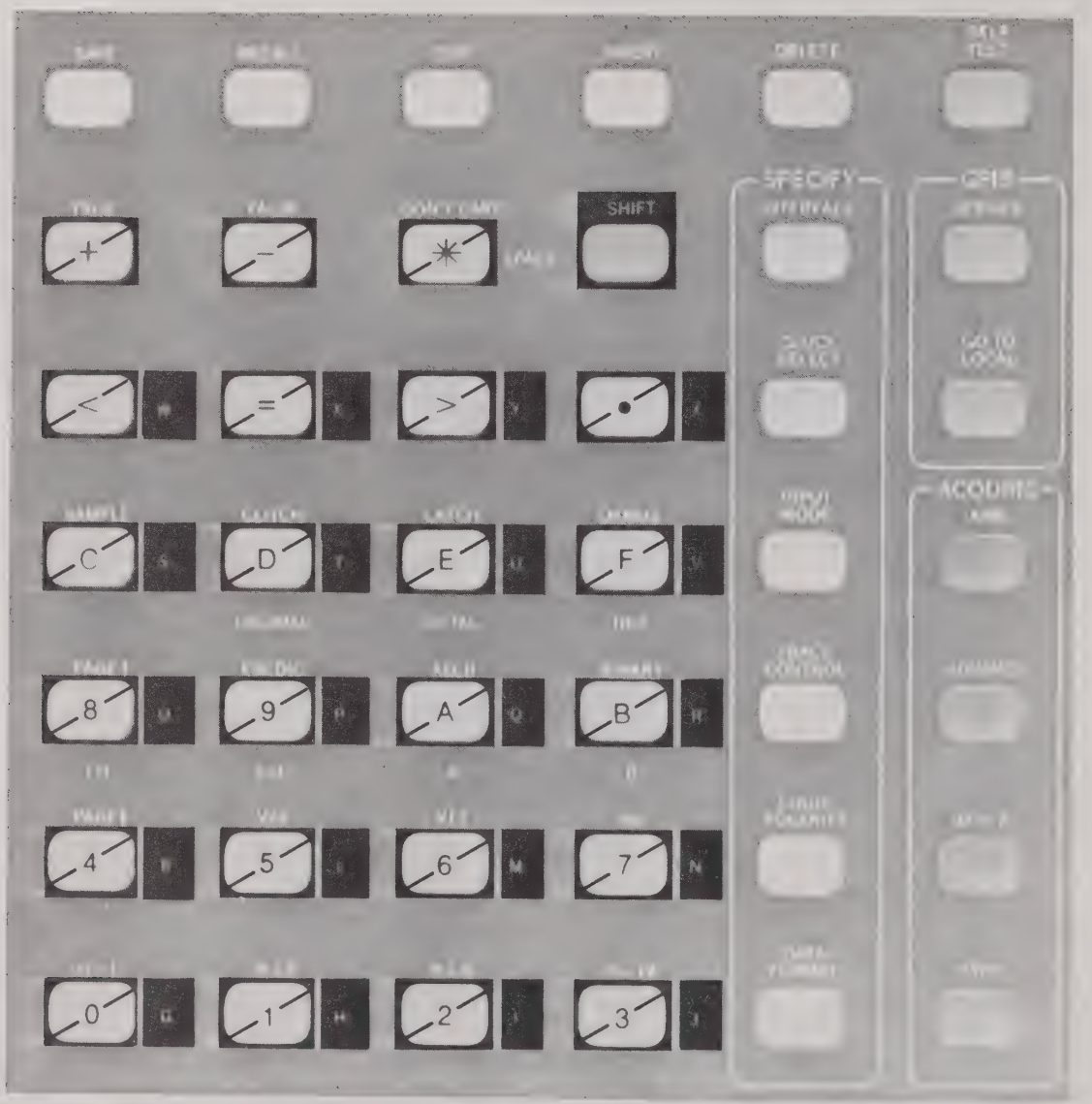


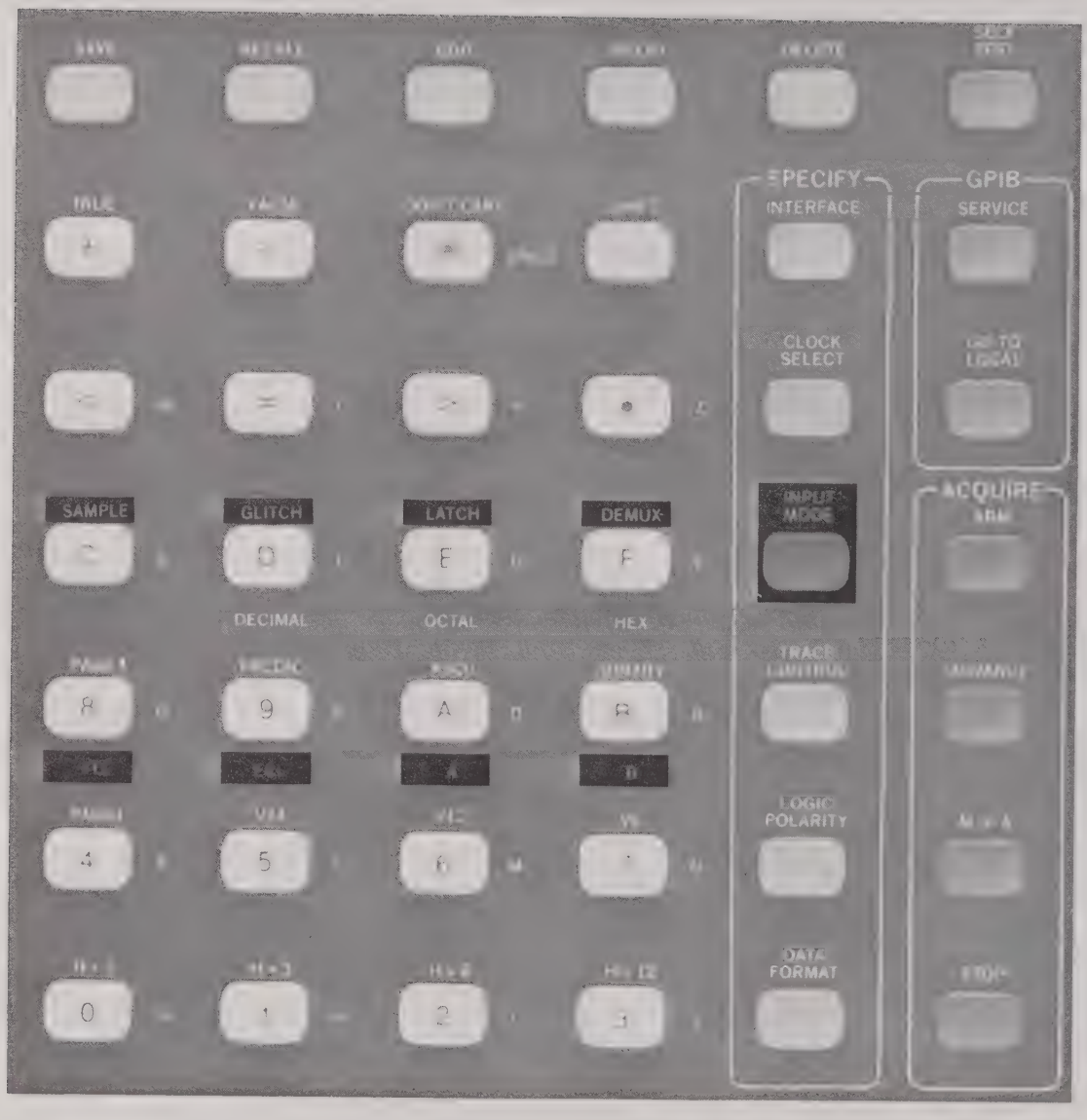
Figure 4-6. ASCII Keys.

and without the **SHIFT** key as shown in Figure 4-6. These keys can be used for labelling channels in the timing display. Table 4-5 is an index to the various key groups and corresponding figures.

Table 4-5. Key Groups

Key Group	Figure
INPUT MODE	4-7
TRACE CONTROL	4-8
LOGIC POLARITY	4-9
DATA FORMAT	4-10
EDIT	4-11
DATA ENTRY	4-12
GRAPH	4-13
TIMING ENTRY	4-14

The **PAGE UP** and **PAGE DOWN** keys scroll displays vertically. The horizontal expansion keys are used with the Graph display and the Timing display. They are **H x 1, H x 3, H x 6,** and **H x 12.** The vertical expansion keys are used with the Timing display. They are **V24, V12,** and **V6.**



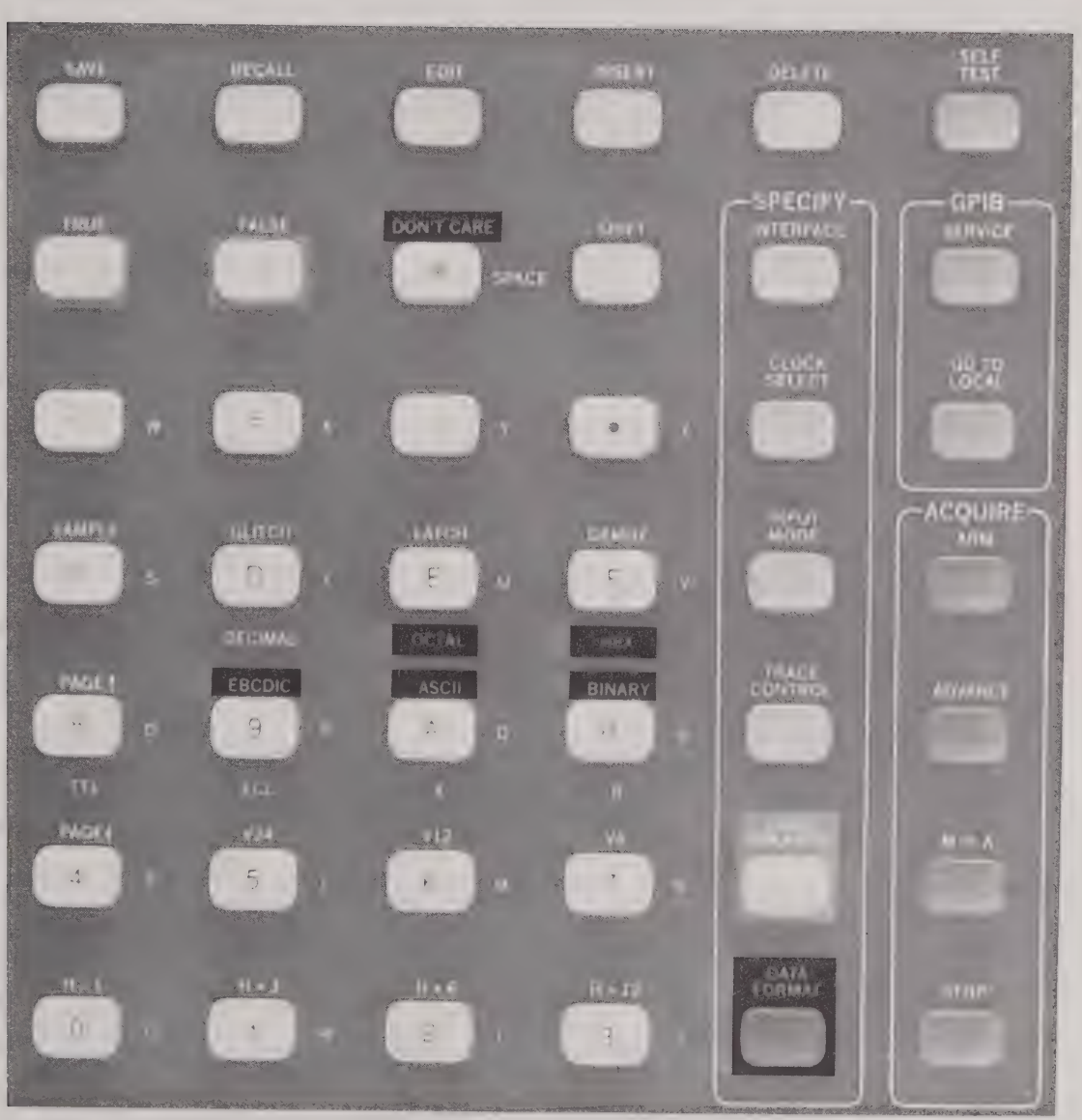
USED WITH NUMERIC CHOICE AND QUICK KEYS

Figure 4-7. Input Mode Keys.

USED WITH HEXIDECIMAL NUMERIC CHOICE KEYS AND QUICK KEYS

Figure 4-8. Trace Control Keys.

Figure 4-9. Logic Polarity Keys.



USED WITH QUICK KEYS AND CHOICE KEYS.

Figure 4-10. Data Format Keys.

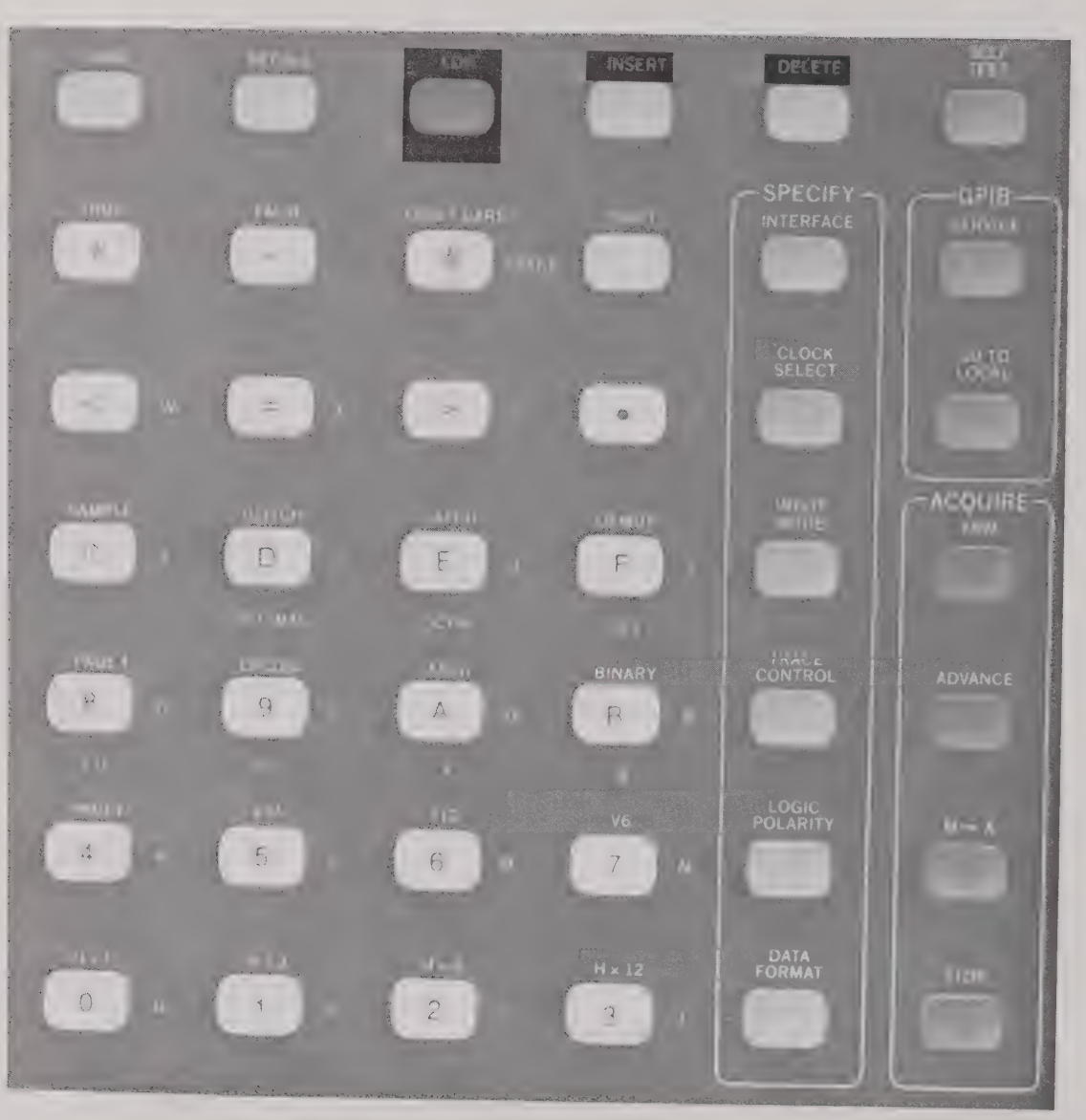


Figure 4-11. Edit Keys.

Figure 4-12. Data Entry Keys.

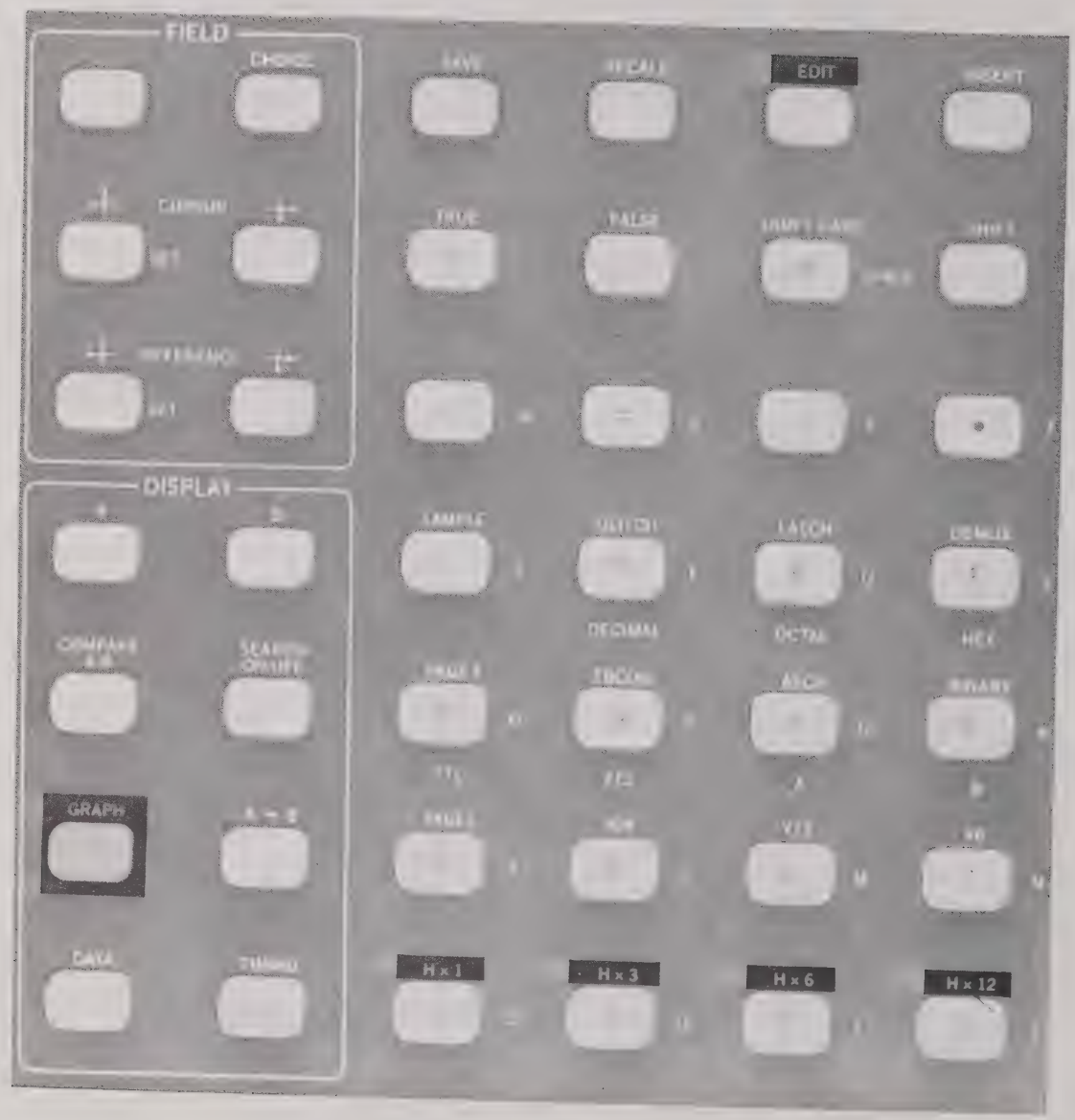


Figure 4-13. Graph Keys.

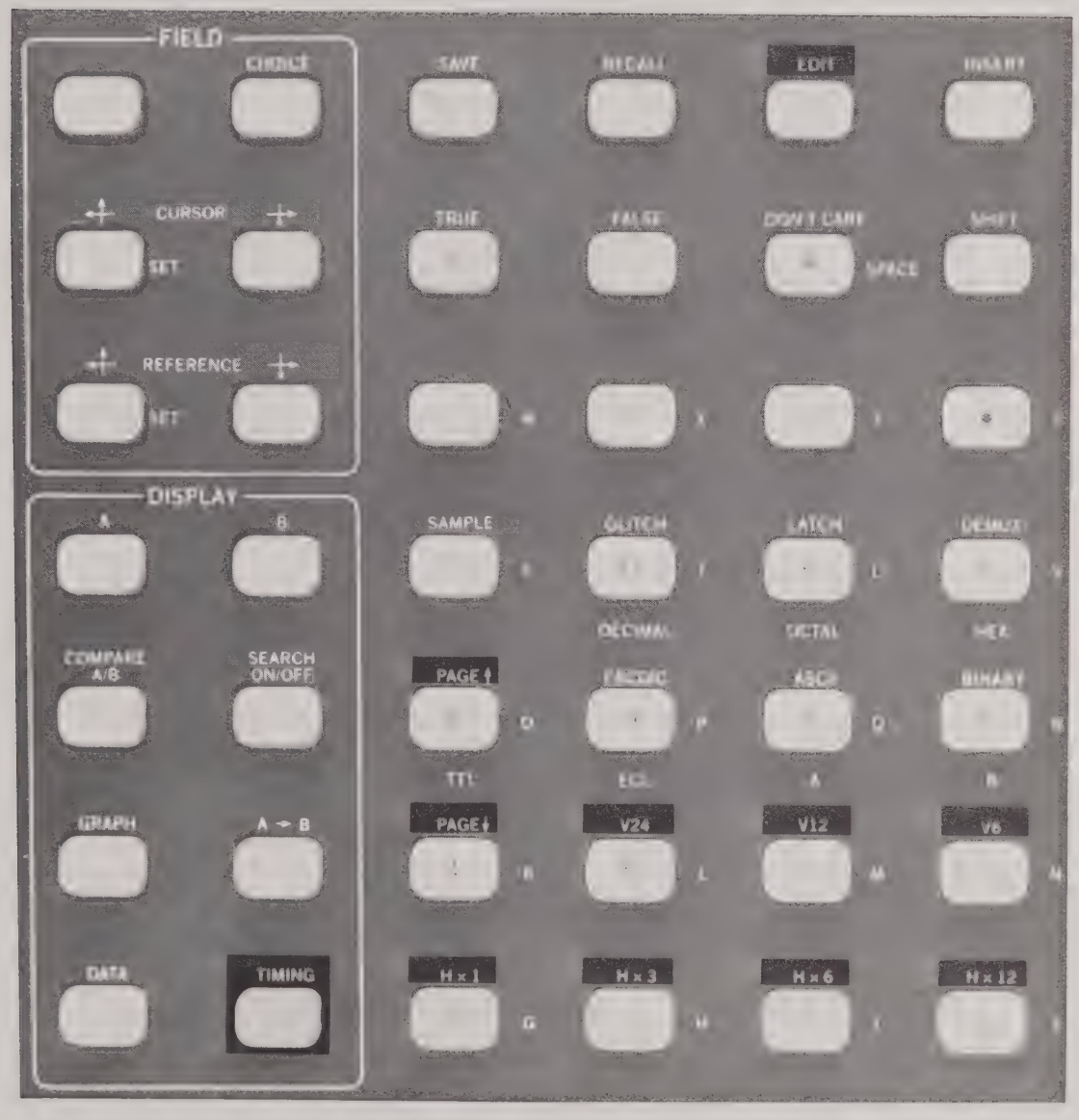


Figure 4-14. Timing Entry Keys.

4.5.6 GPIB KEYS

These keys control start and stop communication functions for either GPIB or RS-232 protocol. The interface conditions are set using the Interface screen in the SPECIFY area.

The GPIB status is shown at the top of each K101-D display.

The **SERVICE** key puts a service request (transfer request) onto the GPIB bus (SRQ). **SHIFT, SERVICE** generates a transfer request for the RS-232 interface.

The **GO TO LOCAL** key returns the K101-D to front panel control.

4.6 DISPLAYS

4.6.1 OVERVIEW

Four types of displays are incorporated in the K101-D as shown in Figure 4-15. On the left side of Figure 4-15 are operational displays; on the right side, self-test displays. The actions required to load the different sets are also shown in Figure 4-15.

The operational displays are used in sets. A set consists of the following:

a. Clock Select	Figure 4-16	(see Paragraph 4.5.2.2)
b. Input Mode	Figure 4-17	(see Paragraph 4.5.2.3)
c. Trace Control	Figure 4-18	(see Paragraph 4.5.2.4)
d. Logic Polarity	Figure 4-19	(see Paragraph 4.5.2.5)
e. Data Format	Figure 4-20	(see Paragraph 4.5.2.6)
f. Graph	Figure 4-21	(see Paragraph 4.5.4.5)
g. Timing	Figure 4-22	(see Paragraph 4.5.4.8)
h. Data	Figure 4-23	(see Paragraph 4.5.4.7)
i. Interface	Figure 4-24	(see Paragraph 4.5.2.1)

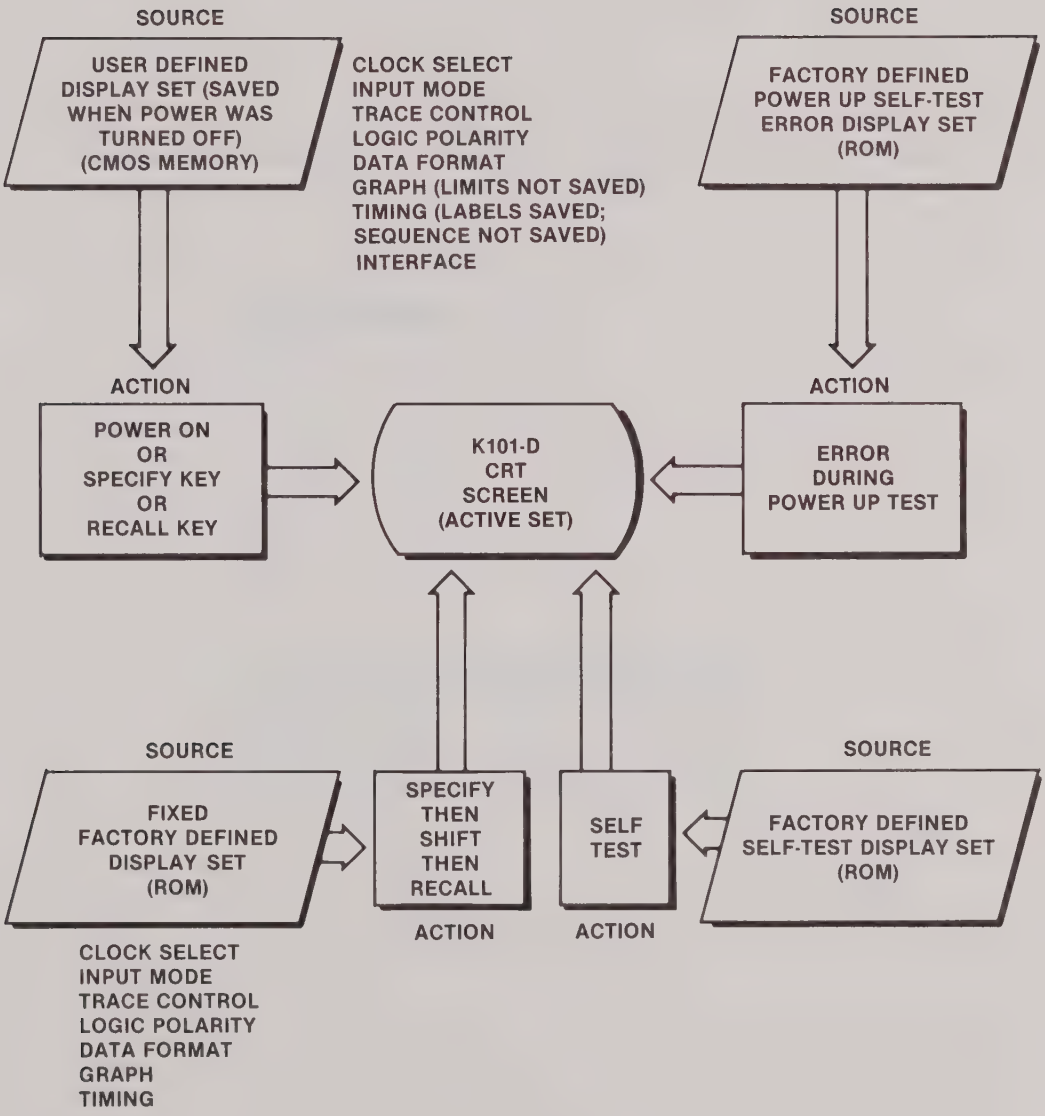


Figure 4-15. Types of Displays on the K101-D.

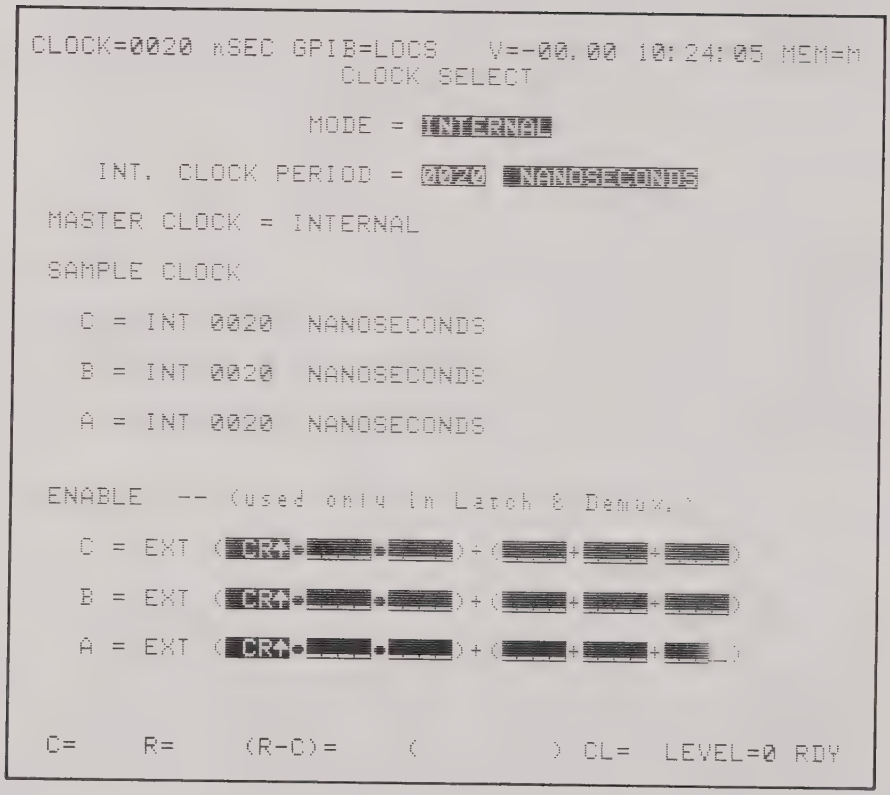

CLOCK=0020 nSEC GPIB=LOCS V=-00.00 10:24:05 MEM=M
CLOCK SELECT
MODE = INTERNAL
INT. CLOCK PERIOD = 0020 NANOSECONDS
MASTER CLOCK = INTERNAL
SAMPLE CLOCK
C = INT 0020 NANOSECONDS
B = INT 0020 NANOSECONDS
A = INT 0020 NANOSECONDS
ENABLE -- (used only in Latch & Demux.)
C = EXT
B = EXT
A = EXT
C= R= (R-C)= ( ) CL= LEVEL=0 RDY

Figure 4-16. Clock Select Default Display.

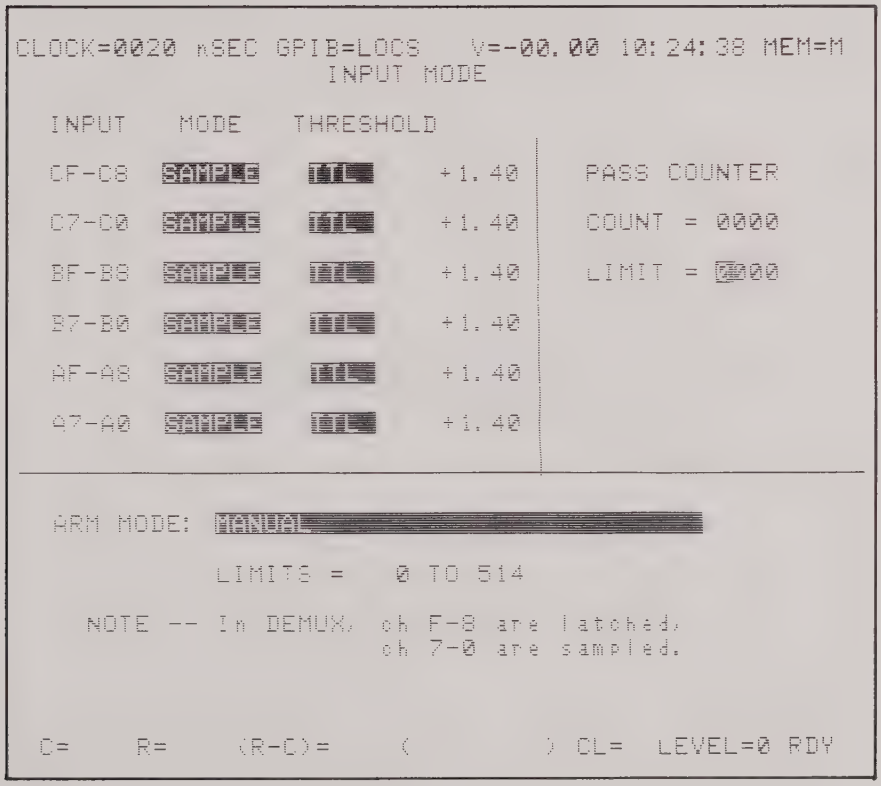

CLOCK=0020 nSEC GPIB=LOCS V=-00.00 10:24:38 MEM=M
INPUT MODE
INPUT MODE THRESHOLD
CF-C8 SAMPLE TTL +1.40
C7-C0 SAMPLE TTL +1.40
BF-B8 SAMPLE TTL +1.40
B7-B0 SAMPLE TTL +1.40
AF-A8 SAMPLE TTL +1.40
A7-A0 SAMPLE TTL +1.40
PASS COUNTER
COUNT = 0000
LIMIT = 0000
ARM MODE: MANUAL
LIMITS = 0 TO 514
NOTE -- In DEMUX, ch F-8 are latched,
ch 7-0 are sampled.
C= R= (R-C)= ( ) CL= LEVEL=0 RDY

Figure 4-17. Input Mode Default Display.

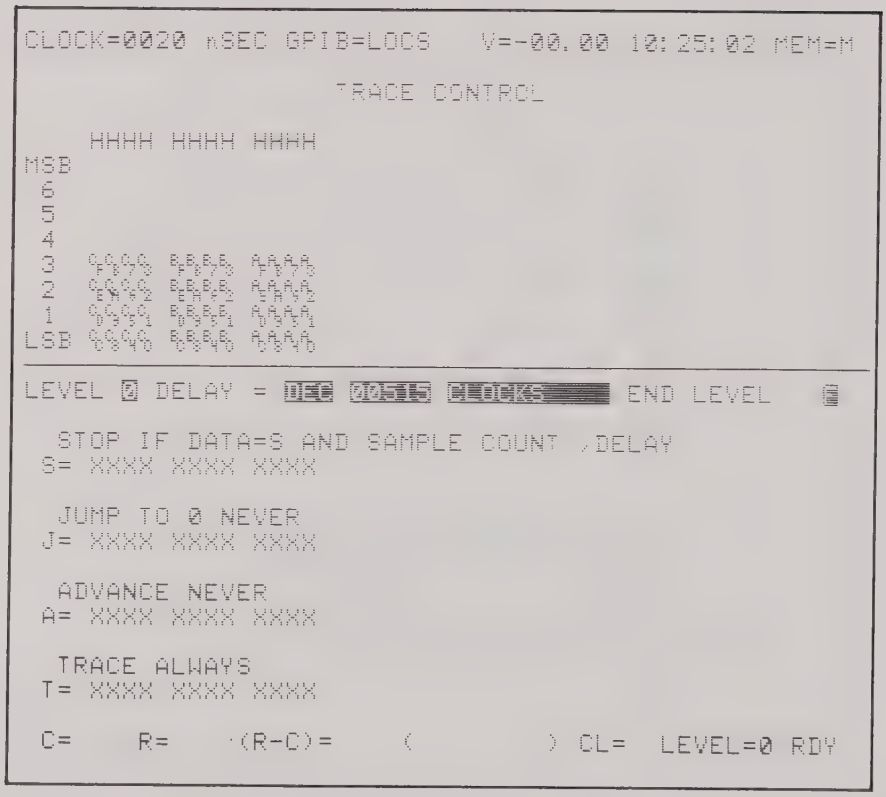


Figure 4-18. Trace Control Default Display.

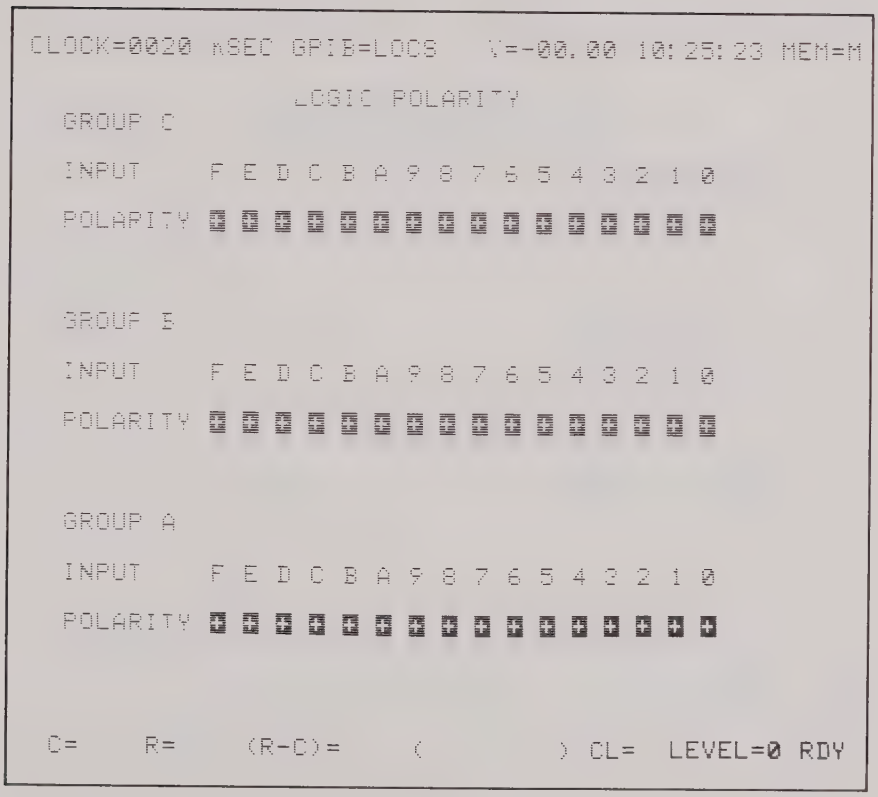

CLOCK=0020 nSEC GPIB=LOCS V=-00.00 10:25:23 MEM=M
LOGIC POLARITY
GROUP C
INPUT F E D C B A 9 8 7 6 5 4 3 2 1 0
POLARITY
GROUP B
INPUT F E D C B A 9 8 7 6 5 4 3 2 1 0
POLARITY
GROUP A
INPUT F E D C B A 9 8 7 6 5 4 3 2 1 0
POLARITY
C= R= (R-C)= ( ) CL= LEVEL=0 RDY

Figure 4-19. Logic Polarity Default Display.

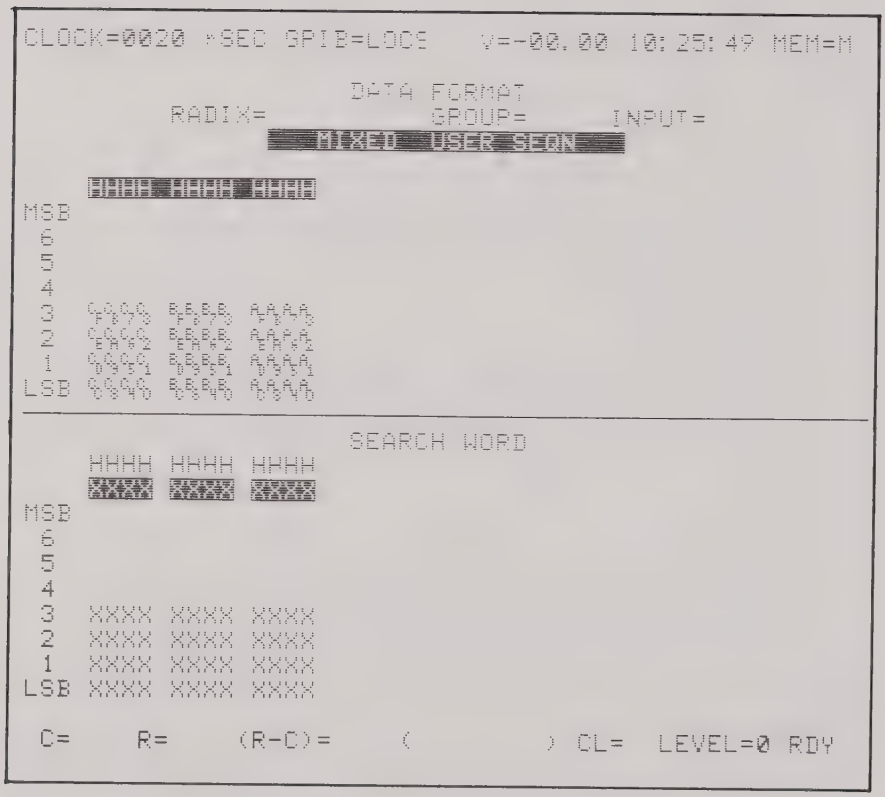


Figure 4-20. Data Format Default Display.

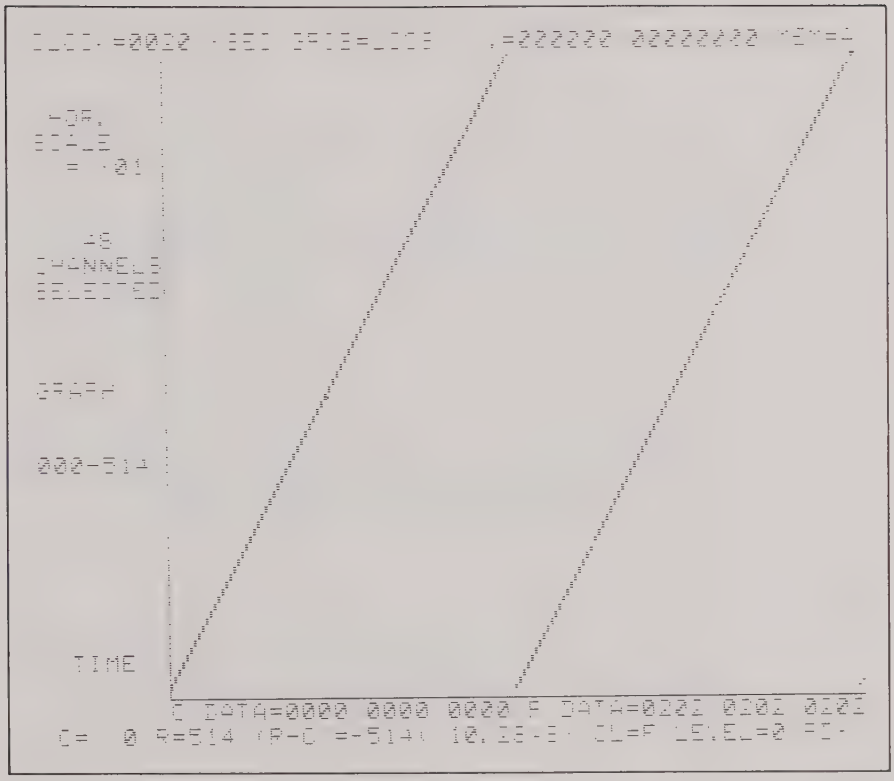


Figure 4-21. Graph Default Display.

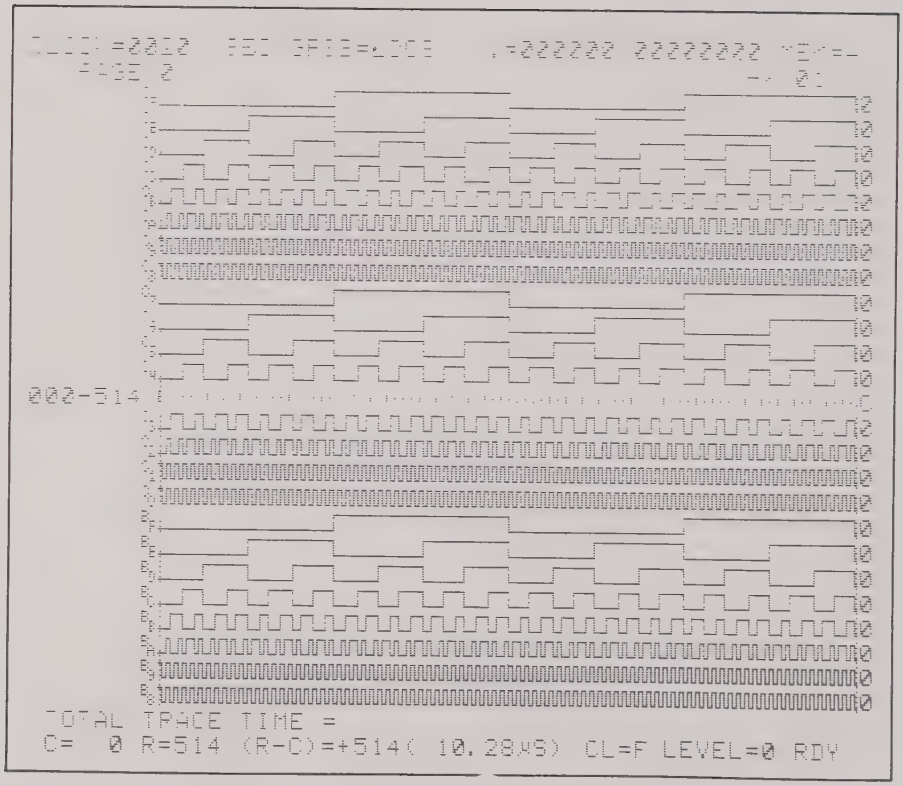


Figure 4-22. Timing Default Display.

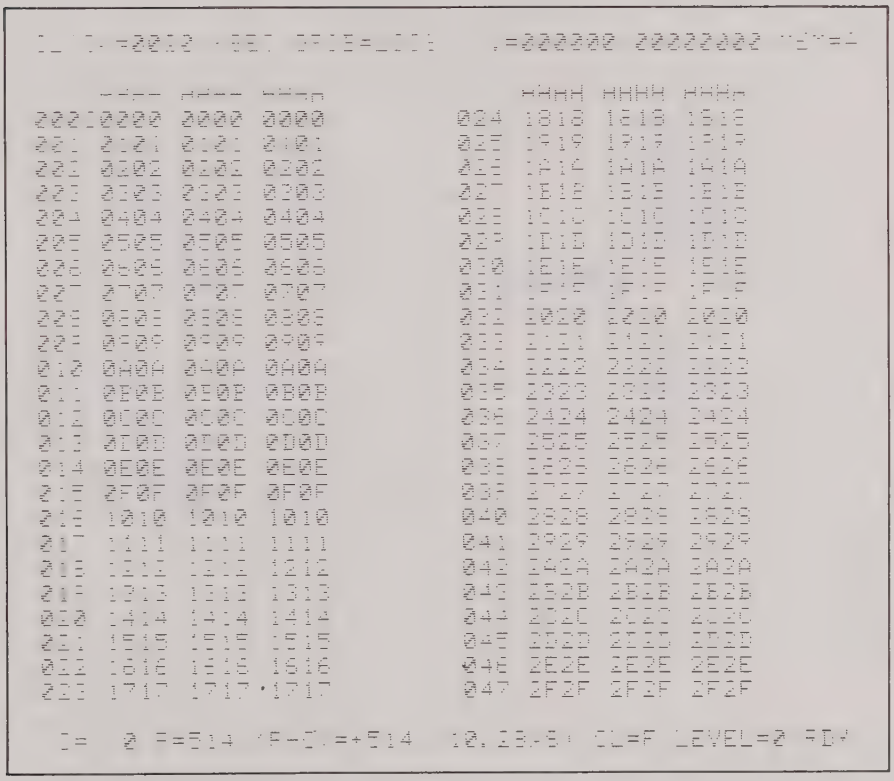


Figure 4-23. Data Default Display.

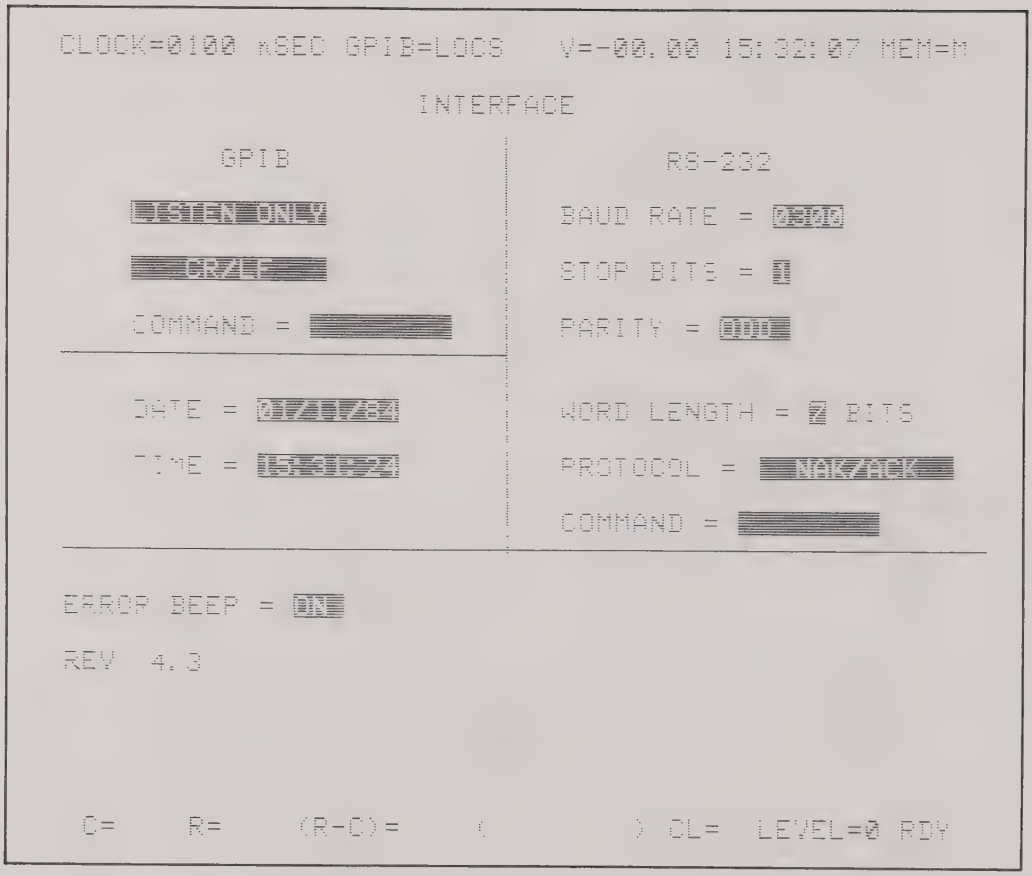


Figure 4-24. Interface Default Display.

The first eight displays relate to setup, recording, and analysis. The last one, Interface, is used for communication options. These displays are discussed in detail in other parts of the manual as indicated above.

The operational display set can be individually defined by the user or it can be simply the base set of factory-defined displays stored in ROM. (See Figures 4-16 through 4-23 for the factory-defined set.)

The user-defined displays are built up from the factory-defined (default displays) set.

Note

The operational displays are loaded, saved, or recalled as sets.

For convenience of discussion, the operational display of memory that is shown on the screen at any instant of time is referred to as part of the Active Display set. If AC power is lost for any reason, the Active Display set will be saved in battery-backed CMOS memory by the K101-D. When power is restored (or the unit is turned on) all of the previously active recording parameters are recalled. The Clock Select display of the Active Display set will show on the screen after the power up self-test is successfully completed.

If there is an error during the power up test, the screen will show one of the factory-defined error messages.

After successful power up, the operator can select any one of the displays of the Active Display set for review or modification.

Alternately the operator could replace the Active Display set with the basic factory-defined Operational Display set. This is achieved by pressing one of the SPECIFY keys, then **SHIFT** and **RECALL**.

CAUTION

Do not press **SHIFT/RECALL** if you want to save the setup for the Active Display set. Press **SHIFT/SAVE** to store the set before you load the factory-defined set.

Any Active Display set can be modified directly from the keyboard. Two setups of Clock Select, Input Mode, Trace Control, Logic Polarity, and Data Format can be stored in memory. One Interface setup can be stored. The Graph format, Timing format, and Data format are derived from the same saved information. Timing format labels, used for describing signals, are saved, but other Timing format changes are not saved.

The fourth type of display set is the Self-Test Display set. These displays are described in detail in Section 10.

4.6.2 DEFAULT DISPLAYS

The displays presented in Figures 4-16 through 4-24 are examples of the factory-defined default displays. There are multiple pages of the various displays as follows:

Display	No. of Pages	Display	No. of Pages
Clock Select	6	Graph	1
Input Mode	1	Timing	10
Trace Control	16	Data	varies
Logic Polarity	1	Interface	1
Data Format	6		

When the K101-D is powered up a self-test program is run. The power up program loads memory A and B with test data. The default Graph, Timing, and Data displays show the test information. Identical information is stored in both memories.

a. Turn the power switch OFF then ON. The unit will beep, the screen will stay blank for a few moments, then a Clock Select display will be shown on the screen. RDY will show in the right-hand bottom corner.

b. Press TIMING, A, B.

This is the timing information (Figure 4-22) loaded into memory A and B during the power up process. Both displays should be the same.

c. Press COMPARE A/B to compare the two (see Figure 4-25).

There should be no inequalities.

d. Press GRAPH, A, B, to see the graphs (see Figure 4-21).

4.6.3 STATUS INFORMATION

A status line is included at the top and bottom of every display.

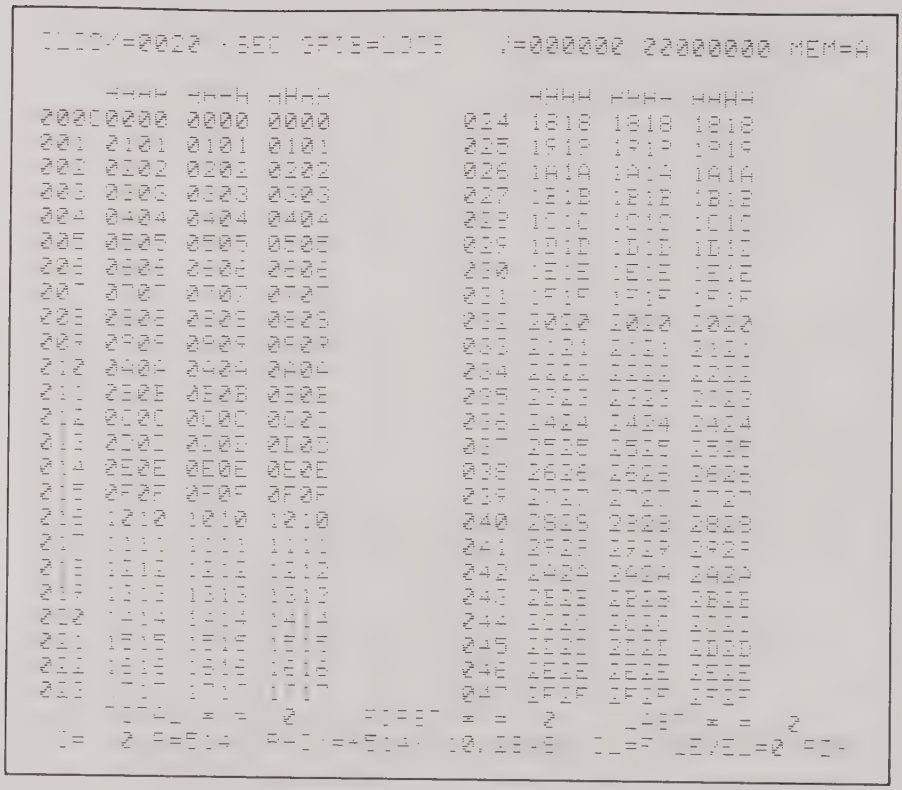


Figure 4-25. Compare A/B Display.

4.6.4 DISPLAY FORMATTING AND MEASUREMENT FEATURES

The most recent recorded data are stored in memory A. Reference data are stored in memory B. Four different perspectives are available: time domain, data domain, graph, and mnemonics. The instrument setups used to make each recording are stored with the recording and some are shown on the status lines of the display. The setups can be reviewed at any time by pressing the desired SPECIFY key, then DISPLAY **A** or B.

4.6.4.1 **Time Domain**

The Timing display shows the logic state of each input as logic high or logic low. The total time (in seconds) that the TRACE command was enabled during a recording (i.e., TRACE if Data = T or TRACE always) is shown in the bottom left corner of the display (TOTAL TRACE TIME); the time is accurate to 20 ns.

The Timing display is divided into ten pages with six lines per page. Figure 4-26 shows a typical 6-line timing page. The number of pages displayed on the screen is a function of the vertical expansion mode that is selected. One, two, or four pages can be shown. Figure 4-22 shows a 24-line presentation. The two PAGE keys can be used to view all the pages. The page number is shown in the upper left corner of the display. The vertical expansion choices are shown on the keyboard as **V24**, **V12**, and **V6**. Expansion takes place below the uppermost input.

The 60 lines of timing information are divided between the instrument sample inputs (48 max.) and user-defined groupings (12 max.). The user-defined inputs are marked with an asterisk (see Figure 4-27).

Horizontal resolution can be expanded by a factor of 3, 6, or 12 (see Figure 4-28). Expansion is indexed to the Control Cursor and occurs to the right of the Control Cursor. When the Control Cursor is moved in an expanded display, the cursor remains fixed and the display shifts.

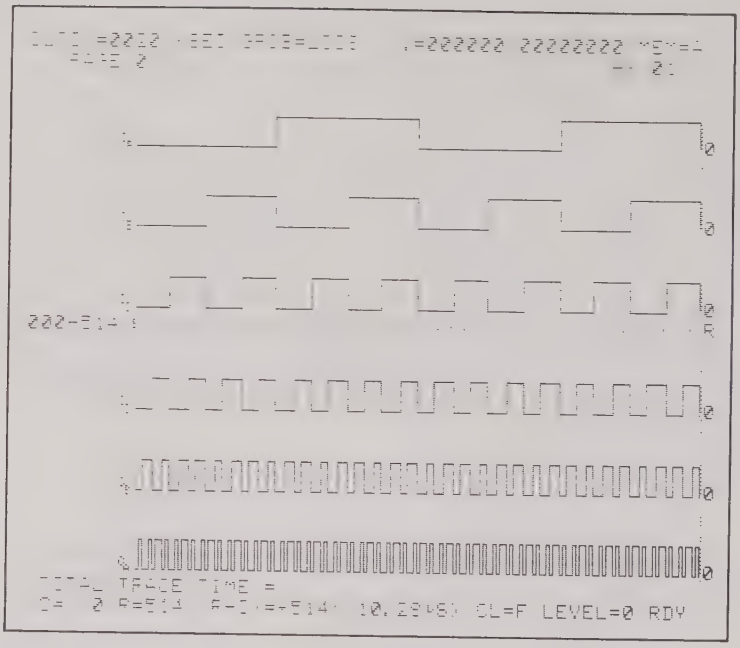


Figure 4-26. Typical Timing Page -- Six lines.

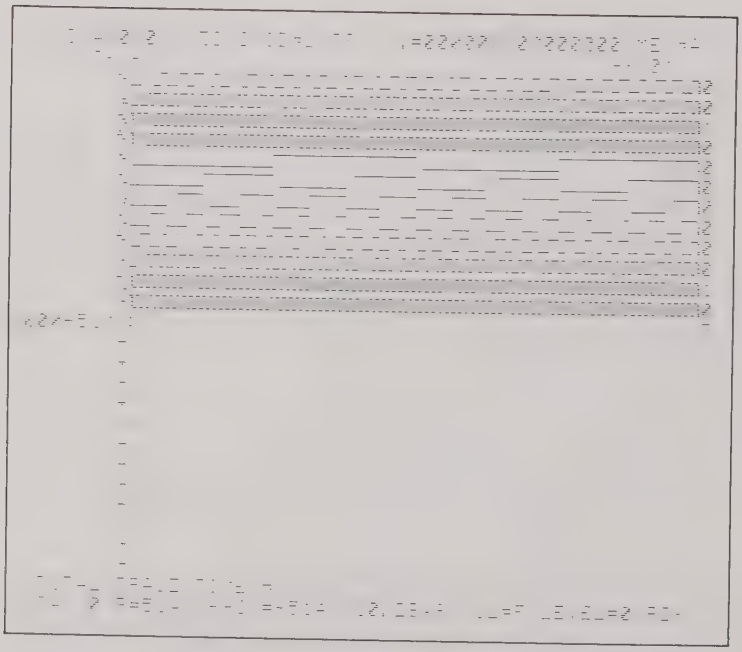


Figure 4-27. User Defined Timing Input.

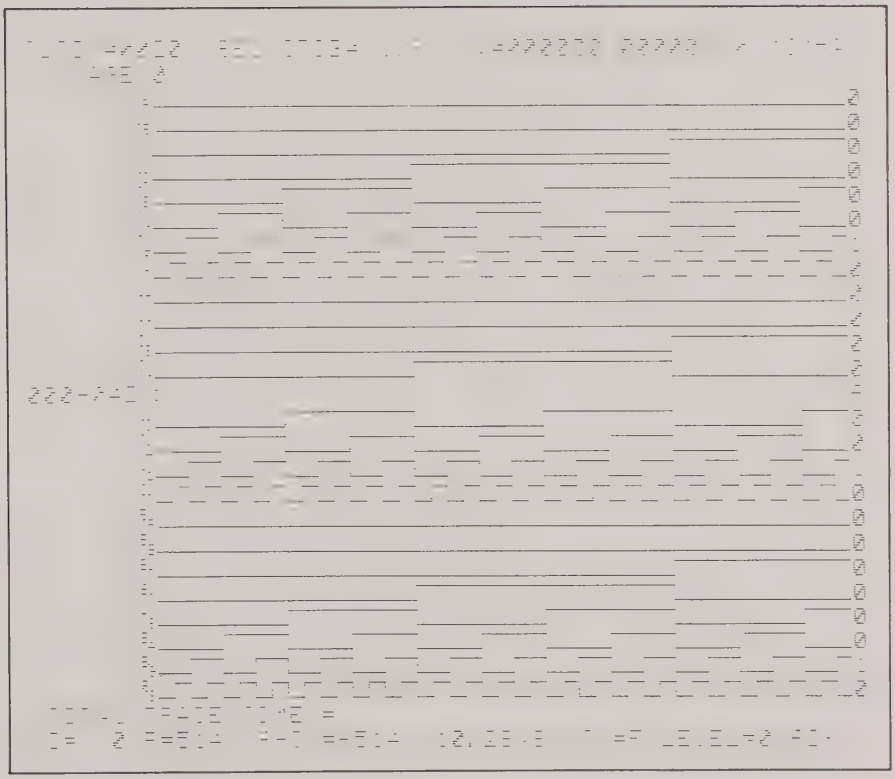


Figure 4-28. Horizontal Expansion.

The HX1 mode uses visual data compression (3 to 1). When the cursor is moved, the location data must change three locations before the cursor on the screen moves. (Cursor location and read out data are always accurate.)

The Timing display can be edited to label, delete, and rearrange individual inputs for your viewing convenience. The location of a one-character, reverse video field indicates which input will change and where a label will appear. To enter the edit mode, press **EDIT**. The video field will appear at the topmost input. Use FIELD keys to position it over the input you wish to alter. To restore it or to put in a different input, press the alphanumeric keys for the specific section input desired. (An input does not have to be deleted before being changed.) The inputs are not removed from memory; they are removed only from the display. The rearranged order of inputs will not be saved when power is turned off. **DELETE** can be used to delete an input.

To give an input a label, move the video field to the left of the desired input. Up to seven alphanumeric characters may be used. The label for each input will be saved along with that input. Therefore, the label will follow when an input is repositioned, and all labels will be saved when power is turned off. Press any of the DISPLAY or SPECIFY keys to escape the Edit mode or press **EDIT** again.

4.6.4.2 **Data Domain**

The binary logic (1 or 0) state of each input at each sample point is displayed as a numeric radix or alphanumeric code.

Press

,

,

to display the data.

In the data domain, each page or column of information consists of 24 words. The entire display can be shifted up or down 24 words at a time by pressing the PAGE keys. A minimum of one page, or 24 words, and a maximum of seven pages, or 168 words, can be on screen at a time. The number of words and columns displayed depends on the width of the data format chosen.

As in the time domain display, each of the two cursors indicates a particular memory location and its associated value. Besides the status line, the location of each cursor displayed is indicated by a C and R between the memory location number and the data value at that location (see Figure 4-29). In the FIELD key area, each press of the CURSOR keys (for the Control Cursor) and the REFERENCE keys (for the Reference Cursor) will move the cursor one location up or down. Holding a key down will cause the cursor to rapidly advance. A cursor can be directly moved to a location by pressing the **SHIFT SET**, the desired location, and the **DATA** key (in the DISPLAY area). When the Control Cursor reaches the top or bottom of the first-displayed, 24-word column, the display automatically shifts 24 words so that the Control Cursor always stays on the screen in the first column (see Figure 4-29). This is not true for the Reference Cursor; it may be off screen. However, its memory location is always given in the bottom status line. Press and hold to move the cursor through several columns.

The entire contents of memory A and its associated setups can be copied into memory B simply by pressing

.

The entire sampled contents of memory A can be compared to the entire contents of memory B on a bit-by-bit basis. A line at the bottom of the display gives the total number of mismatches (indicated by a ≠ sign) and

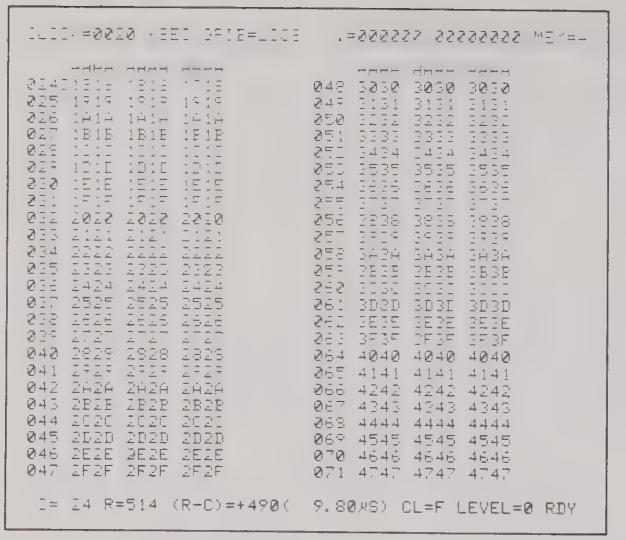
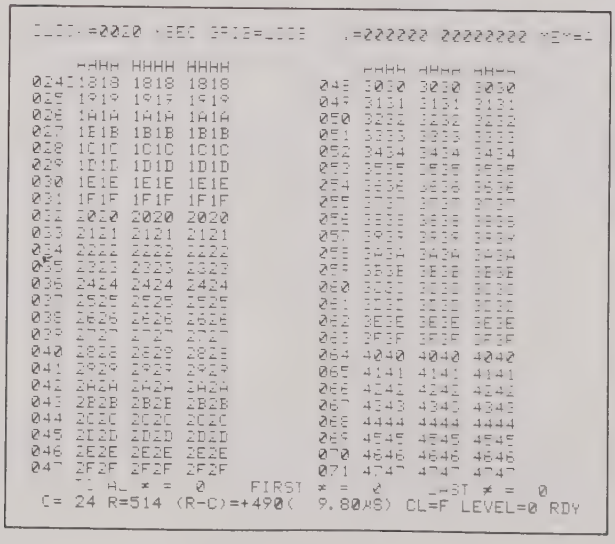


Figure 4-29. Data Display Cursor Location.



Note: Comparing memories A and B shows that there are no differences between them.

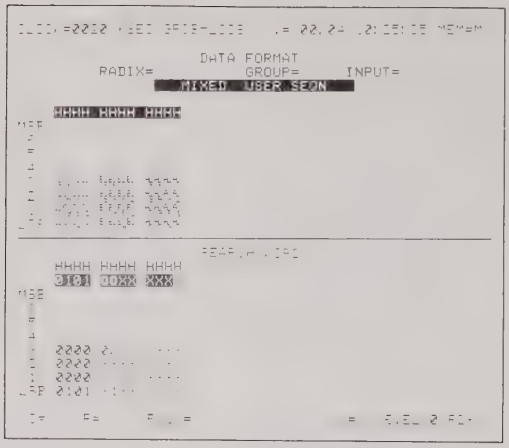
Figure 4-30. Equal Compare of Memories A and B.

the location of the first and last mismatch (see Figure 4-30). Each individual mismatch is marked by a ≠ sign between its location and data value. If a single bit in a displayed memory A word is unequal to its counterpart bit in memory B, a ≠ sign is displayed. Only the sample inputs of those characters displayed are compared. If an input is not displayed by the current data format, then it is not included in the comparison.

Memory A or B can be searched for all occurrences of any word you wish to locate. Enter the desired word in the bottom half of the Data Format screen. The word can be specified by character or bit. If a character value is entered, the K101-D automatically assigns the individual bit values. If individual bit values are assigned, but not all bits of a character are specified, then a "semi-care" is put in the character field (see Figure 4-31).

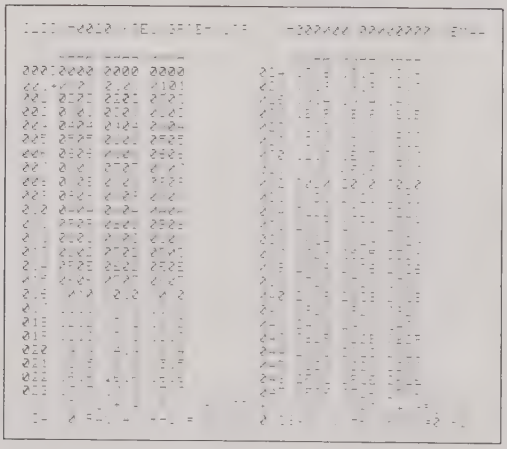
To implement the search, after entering the desired word, press DATA and then SEARCH ON/OFF .

A line at the bottom of the display gives the total number of specified words found (indicated by an *) and the location of the first and last word found. Each individual word found is marked by an * between its location and data value (see Figure 4-32). The display automatically brings up the first word found. Pressing CHOICE NEXT will automatically shift the display to the next sequential word found and places the Control Cursor at its location. Press CHOICE NEXT . Press SEARCH ON/OFF again to turn it off.



Note: The first four characters (inputs CF-C0) of the search word were specified as hex characters in the character field. Inputs BF and B8 were specified individually in the bit fields thereby creating a "semi-care" in the character field.

Figure 4-31. Search Pattern with "Semi-Care."



Note: The first of three words to meet the search word specifications was found at memory location 1.

Figure 4-32. Search Result Status.

Memory B can be edited or filled from the front panel keyboard (or through the communication interface). Display memory B by pressing **DATA, B, EDIT.** A reverse video field appears which can be moved around by the appropriate FIELD keys to the location and character to be edited. To enter a specific data value, press the appropriate alphanumeric key.

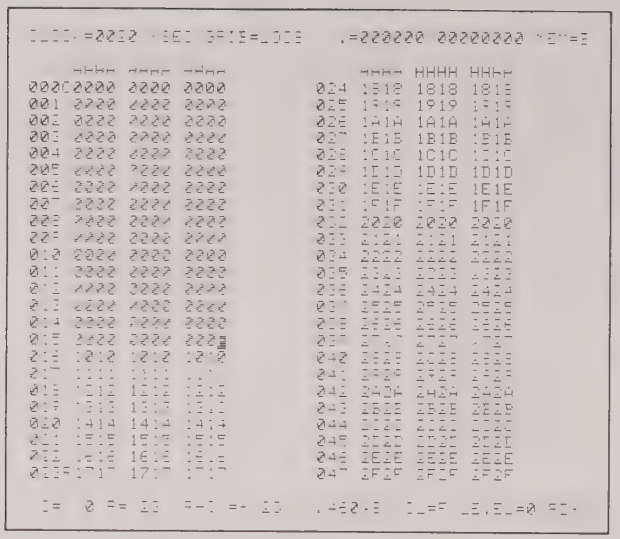
Press ▽ SET , ▷ four times, then C S , D T DECIMAL , E U OCTAL , F V HEX .

Holding a single key down will cause the video field to automatically advance rapidly and write over each character with that key value changing the actual memory B contents.

Press △ , then press and hold 0 G Hx1 through location 15 (see Figure 4-33). Press A→B to restore the contents of memory B by transferring memory A into memory B.

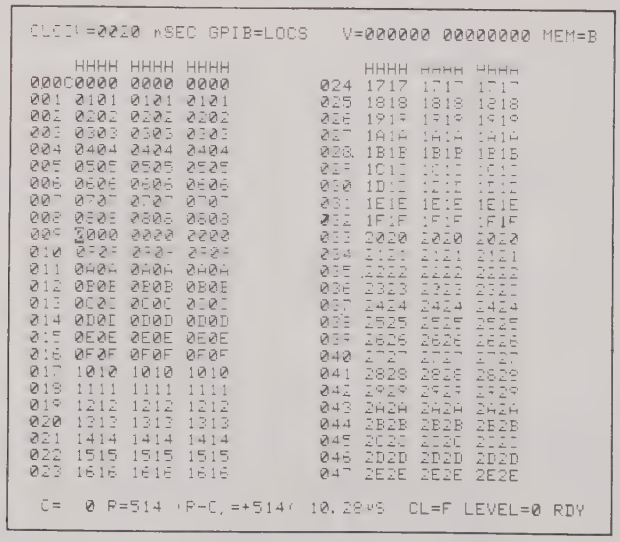
Entire words can be inserted and deleted from memory. Move the video field to any character of the word you wish to insert or delete.

Press EDIT , then ▽ SET nine times. Pressing INSERT will insert a word of all zeros at that location and shift all subsequent words down one location (see Figure 4-34). New information can now be entered. The last word in memory will be lost.



Note: Through editing, the first 16 words of memory B have been replaced with all zeros.

Figure 4-33. Editing Memory B.



Note: A word of all zeros has been inserted at location 009, shifting all other words down one location.

Figure 4-34. Inserting a Word in Memory B.

Pressing DELETE will remove that word from memory and shift all words up one location (see Figure 4-35). Pressing it again will remove the new word at that location. The last memory location is loaded with zeros.

The captured information can be reformatted into a format different from the one initially displayed. The memory contents are not changed by changing the displayed data format nor is the time domain display affected. Changing the data format changes the way the memory A and B contents are displayed in the data domain, the format of the trace control word recognizers, and the inputs that will be selected for graphing. A character column is deleted by positioning the field cursor over the character radix and pressing **DELETE**. All columns to the right of the field cursor location can be deleted at one time by pressing **SHIFT, DELETE**. A column can be inserted at the cursor location by pressing **INSERT**.

4.6.4.3 **Graph**

Each recorded sample is displayed as a single point on a graph (see Figure 4-21). The internal memory location of each sample is plotted on the horizontal axis, and the magnitude or numeric value of the inputs that comprise each sample is plotted on the vertical axis. A graph gives a macro view of all recorded samples and system activity.

Press SHIFT , RECALL , GRAPH , A .

Generating the graph takes a few seconds to complete because each point is plotted on a pixel basis. While the graph points are being calculated, a BUSY PLOTTING message appears on screen (see Figure 4-36).

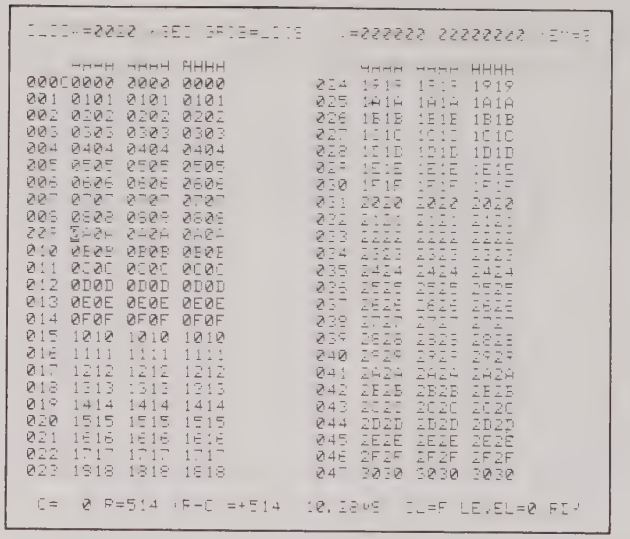


Figure 4-36. Message Displayed During Graph Point Calculations.

Similar to the time domain display, the two movable cursors (the Control Cursor and Reference Cursor) highlight the sample point at a particular memory location. A hexadecimal readout of the value or magnitude of the sample point is displayed just above the bottom status line. As in all displays, the locations and separation of the cursors are indicated in the bottom status line.

All 514 samples are graphed in HX1, the regular unexpanded mode, which gives an overview of the entire recording. The graphic scale can be horizontally expanded by a factor of 3, 6, or 12 to allow better visual resolution. Expansion takes place to the right of the Control Cursor, which then remains at the leftmost edge of the display. Moving the Control Cursor in an expanded display causes the entire display to shift, but not the cursor.

The first 14 columns of the current data format determine the input channels that will be plotted. The number of inputs in each character column can vary from one to eight depending on the radix or code specified for that column. The number of input "channels selected" to be graphed is the sum of the number of inputs that comprise the first 14 columns. (Each space, or blank column, counts as one character of zero inputs.) Therefore, all 48 inputs of the K101-D can be plotted when the data format is 12 hex characters (see Figure 4-37). If there are more than 14 columns in the current data format, the analyzer will plot only the value of the first 14.

The display can be vertically expanded between any two points to give better visual resolution by editing the upper and lower numeric limits.

Press [DATA FORMAT] , [PAGE 4 K] , [▽ SET] , [▷] twice, [SHIFT] , [DELETE] , [GRAPH] to reformat and display the graph (see Figures 4-38 and 4-39).

Move the Control Cursor [▷] to location 127, and move the Reference Cursor [▽] SET to location 159. This gives you the upper and lower data values of the visual area you wish to expand (see Figure 4-40). Press [EDIT], [EBCDIC 9 ECL] P, [DEMUX F HEX] V, [V6 7] N, [DEMUX F HEX] V to enter the new upper and lower boundary values for the vertical axis. Press [EDIT] again to automatically replot the graph with the new limits. Out-of-range values will be shown as a line at the very top or bottom of the display. Press [Hx12 3] J to see better detail.

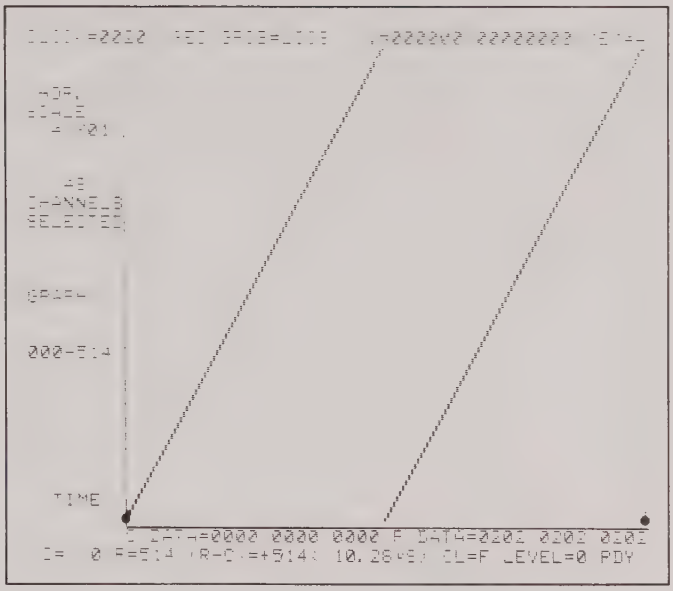


Figure 4-37. Two Full Cycles of Six 8-bit Binary Counters.

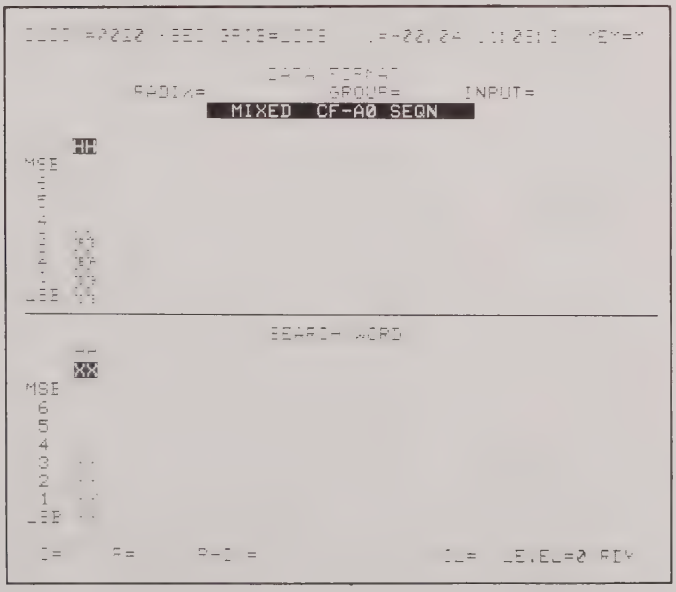


Figure 4-38. The Data Format Used For Figures 4-39 and 4-40.

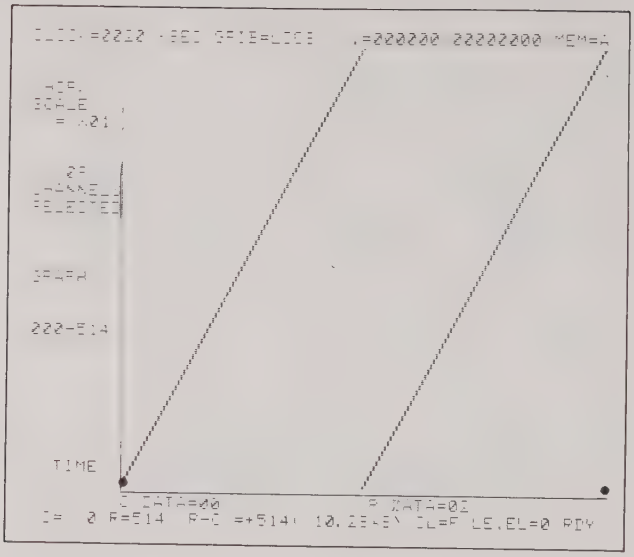
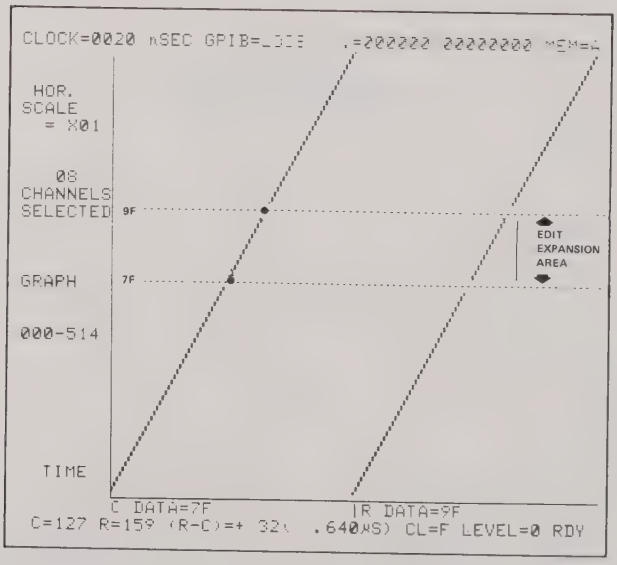


Figure 4-39. Graph of Two Full 8-bit Binary Counter Cycles.



Note: The Control and Reference Cursors are moved to find the numeric values of the area it is desired to expand.

Figure 4-40. Expanding the Display.

Section 5

SPECIFYING RECORDING PARAMETERS

5.1 OVERVIEW AND STRATEGY

In discussing the principles of logic analysis, we have presented these themes: collection, reduction, and organization. This section considers the strategy and approach for data collection and reduction -- that is, the isolation of meaningful data for collection. Of course, organization of the data is implied in how we select what to look for.

The key concept is selection. The system under test can generate millions of events surrounding a half-dozen events of interest.

This section focuses on what you can do with the specification possibilities. Section 3 gives detailed reference material on the Specify menus. Section 4 presents information on keying your selections. Those sections answered "what" and "how"; this section explores "which choice" and "why."

5.1.1 DATA FLOW

For background, consider again the flow of data into the K101-D. Your recording parameter specifications influence many points in the data flow, so we will start with a brief overview of the whole process before delving into details.

Events in the system are monitored according to where the probes are attached. Individual signals to the system are characterized as zeros and ones, depending on their voltage level at the moment of sampling and on two settings for each input signal: threshold level and polarity. Individual signals are retained, discarded, or set aside for later use according to your input mode and clock selections.

The trace control logic examines the current samples and evaluates them for control of the recording process and for determination of tracing. Samples that are selected for tracing are clocked into memory M, initially at location 511. As the recording process continues, samples are shuttled forward in memory. If no END OF ACQUISITION signal occurs before a sample is clocked past memory location 000, then that sample and each sample thereafter is discarded and replaced by the subsequent sample.

5.1.2 ENDING THE RECORDING CYCLE

Several conditions generate an END OF ACQUISITION signal, which ends the recording cycle. The signal may come from the trace control logic, caused by either the fulfillment of a stop condition or by the presence of an end level. Manual entry of a STOP or M->A command also generates this signal.

5.1.3 ORGANIZATION OF SECTION 5

This section is organized in two parts: (1) a brief discussion of probe connection, and (2) a detailed discussion of the specification choices for conditioning the input signals from the probes and using the signals to control and trace events within the system under test.

5.2 **PROBE CONNECTION**

To begin specification, you must decide where to connect the probes based on your understanding of the system under test and the capabilities of the logic analyzer. Some information on probe connection is given below, to help in selecting connection points and connection order and in making the physical connections.

5.2.1 INPUT SIGNALS AND DATA FORMAT

You can connect more probes than you specify in the data format. If a trace event is recorded, all signals present at that moment are recorded.

The extra recorded signals are not displayed unless you change the data format to specify them. Also, you can display a probe signal more than once by grouping recorded signals in more than one format as convenient.

5.2.2 ORDER OF CONNECTION

The order and grouping of input signals (probe connections) affect later specifications of these signals. Certain specifications are assigned by probe, that is, assigned to a block of eight sample input signals and two clock signals. Among these are the input mode and threshold values. Data formats can be automatically assigned in sequence from CF to A0. If you wish to use a different sequence, you must enter it. This information is detailed later in this section.

5.2.3 PHYSICAL CONNECTION

When connecting the probes to the front panel, insert with the label up and key slot to the left. This is the correct orientation for the signal input designations.

When you connect probes to the target system, keep a written record of their location. Gould provides a form suitable for this, "Input Connection Guide," part number DWS45.183. For an example, see Figure 5-1.

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ____ OF ____ DATE _____

K101-D			TARGET SYSTEM								
			SECTION C			SECTION B			SECTION A		
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J									
CLK	GRY	K									
DATA	VIO	F									
DATA	BLU	E									
DATA	GRN	D									
DATA	YEL	C									
DATA	ORG	B									
DATA	RED	A									
DATA	BRN	9									
DATA	BLK	8									
GND	LT. BRN	GND									
CLK	WHT	R									
CLK	GRY	S									
DATA	VIO	7									
DATA	BLU	6									
DATA	GRN	5									
DATA	YEL	4									
DATA	ORG	3									
DATA	RED	2									
DATA	BRN	1									
DATA	BLK	0									
GND	LT. BRN	GND									

DWS45-5982

Figure 5-1. Input Connection Guide.

5.3 SPECIFICATION CATEGORIES

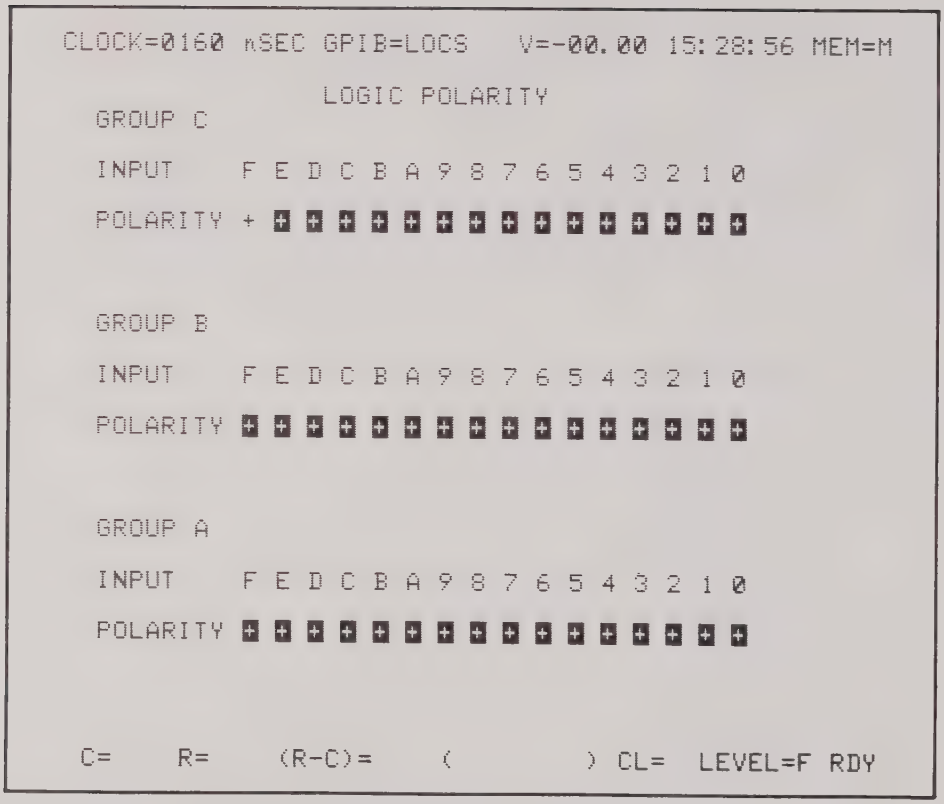
You use screens to specify recording parameters. Information on the SPECIFY key screens and methods of entering specifications are presented in Sections 3 and 4. In the following material we discuss the meanings and uses of the various specification catagories. In general, we do not repeat the full reference material from the prior sections, but only sketch in the important points. If you need help entering your choices, consult Section 4 (User Controls and Displays). Here, we discuss the following categories of the specification process, in the order shown:

a. Logic Polarity
b. Input Mode Screen
    1. Input Mode
    2. Threshold
    3. Arming Modes
c. Clock Select
d. Data Format
e. Trace Control
f. Interface

In actual use, screens may be specified in any order convenient, except that the Data Format screen must be specified before the Trace Control screen. Arming modes and the Interface screen are mentioned here to provide thorough information on the specification process, but are explained elsewhere in this manual.

5.4 LOGIC POLARITY

The Logic Polarity screen allows you to select polarity for all 48 data inputs. The choices are positive or negative; The K101-D assumes positive polarity unless changed. With positive polarity, a signal above threshold is considered as a one and a signal below threshold is considered as a zero. Negative polarity is the reverse: a signal above


CLOCK=0160 nSEC GPIB=LOCS V=-00.00 15:28:56 MEM=M
LOGIC POLARITY
GROUP C
INPUT F E D C B A 9 8 7 6 5 4 3 2 1 0
POLARITY + + + + + + + + + + + + + + + +
GROUP B
INPUT F E D C B A 9 8 7 6 5 4 3 2 1 0
POLARITY + + + + + + + + + + + + + + + +
GROUP A
INPUT F E D C B A 9 8 7 6 5 4 3 2 1 0
POLARITY + + + + + + + + + + + + + + + +
C= R= (R-C)= ( ) CL= LEVEL=F RDY

Note: The logic polarity of each data input can be specified individually. Trace capture data and graphic displays are influenced by the states chosen.

Figure 5-2. Logic Polarity Assignment.

the threshold is considered a zero and below, a one. As Figure 5-2 shows, all inputs are assigned horizontally to their respective section (C, B, or A) and within that section are labelled left to right as F through 0.

The logic polarities specified affect the data patterns seen by the trace control levels as well as the sense of the recorded data. New polarity specifications should cause a new and different recording to be captured, so long as the affected inputs are used for pattern recognition in a relevant trace control level.

When you change polarities, only those recordings made after changing the Polarity screen show the new specifications. This feature eliminates confusion over what conditions were used to make a recording and prevents erroneous interpretation of existing recordings.

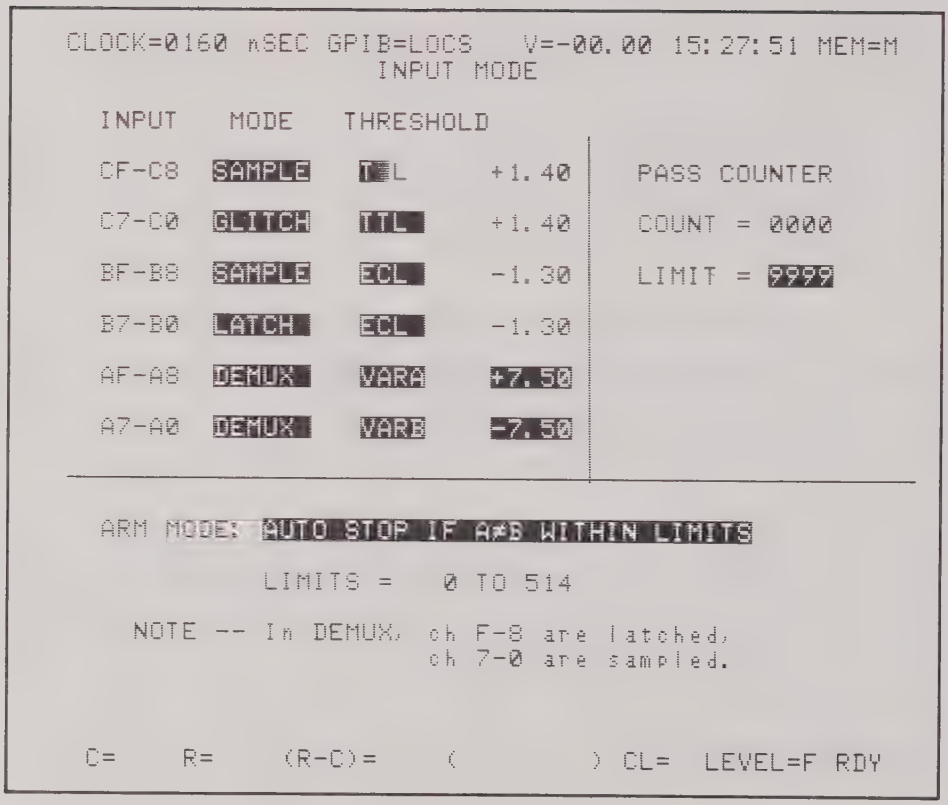
In either the Data or Graph mode, new data are displayed with the selected polarities. In the Timing mode only the binary cursor readout is adjusted; the Timing display always shows the signals as though they were all recorded using positive logic.

5.5 **INPUT MODE SCREEN**

The Input Mode screen (see Figure 5-3) allows you to specify three different types of parameters: input modes, threshold levels, and the arm mode. Each of these categories has several choices available and is discussed separately.

5.5.1 INPUT MODE SELECTION

The K101-D provides flexible input conditioning, with four input mode choices: Sample, Glitch, Latch, and Demux, specified by direct entry keys. The flexibility of input mode specification allows detection of a


CLOCK=0160 nSEC GPIB=LOCS V=-00.00 15:27:51 MEM=M
INPUT MODE
INPUT MODE THRESHOLD
CF-C8 SAMPLE TTL +1.40
C7-C0 GLITCH TTL +1.40
BF-B8 SAMPLE ECL -1.30
B7-B0 LATCH ECL -1.30
AF-A8 DEMUX VARA +7.50
A7-A0 DEMUX VARB -7.50
PASS COUNTER
COUNT = 0000
LIMIT = 9999
ARM MODE: AUTO STOP IF A≠B WITHIN LIMITS
LIMITS = 0 TO 514
NOTE -- In DEMUX, ch F-8 are latched,
ch 7-0 are sampled.
C= R= (R-C)= ( ) CL= LEVEL=F RDY

Note: The Input Mode screen lets you select pertinent sampling parameters for each recording and the maximum number of recordings that may be attempted for each arm cycle.

Figure 5-3. The Input Mode Screen Parameters.

variety of system conditions such as the logic states present at the sample clock expressions or noise spikes occurring between valid sample clocks. Proper choice of input sampling not only captures the right information, it can also reduce loading of the system under test and simplify signal connections.

Input mode assignment is largely independent of other trace specifications. In general, any input mode can be used with any clock mode. However, in all Clock Select screens, the enable clock expressions for each section (C, B, or A) are used when, and only when, either Latch or Demux mode is selected for all or part of that section.

The following descriptions of the four input modes and how they relate to each other will help you decide which mode, or combination of modes, is appropriate for a particular application.

5.5.1.1 **Sample Mode**

Sample mode is the unit's most basic input mode. Inputs selected for the Sample mode are checked at, and only at, each active clock edge to determine their current logic levels. The clock edge is specified by the sample clock expression used for the pertinent input section. In Sample mode, any threshold transitions that occur between sample clocks are ignored.

The total operation of Sample mode during a recording cycle involves both the section's sample clock and the master sample clock. The logic levels present when a section's sample clock comes valid are held in temporary sample registers until that section's next valid sample clock; they are then displaced by the next sample (see Figure 5-4). When the master sample clock comes true, the current contents of all of the temporary sample registers are presented to the trace control for evaluation. If the master sample matches the requirements of the trace control, the trace is enabled for that sample and clocked into the

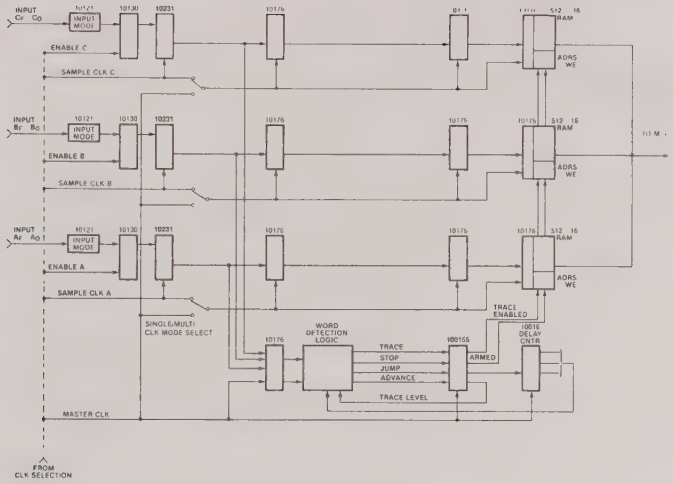
instrument's high-speed memory. The master sample is discarded if it does not match the trace control requirements.

5.5.1.2 **Glitch Mode**

Glitch mode helps detect glitches (possible troublesome noise spikes or asynchronous threshold crossings between valid sample clocks) in your system that would not otherwise be captured. This input mode is handled in the same way as Sample mode, except that the selected inputs are also monitored between every clock sample to determine if a glitch has occurred (see Figure 5-5).

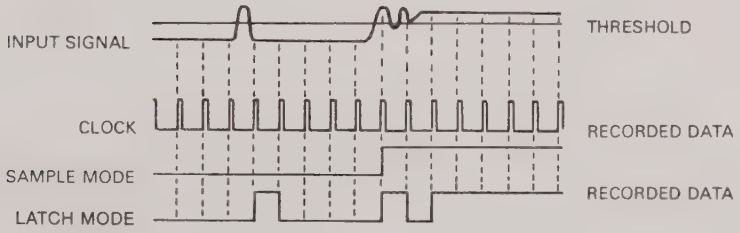
If a glitch does occur between samples, it is held in the temporary sample register instead of the level present at the next occurrence of the sample clock. Therefore, a glitch is displaced when displayed; it shows as if it were the following sample. After the next sample clock, the sample register is reset. If no glitch occurs (that is, if no additional threshold crossings occur between the following sample clocks), the data held in the sample register will be the same as if the unit were in Sample mode.

Glitch capture is independent of the chosen sample rate; a glitch is captured and stored as the next sample whether the unit is being clocked at a slow external rate or sampling at 100 MHz. Absolute glitch capture capability, however, is a function of the sensitivity of the particular instrument and its probes, the threshold level selected, and the total energy of the glitch above (or below) that threshold. A typical response curve is shown in Figure 5-6. Your unit may be a bit more or less sensitive, but should be similar. As noted in the section on specifications, to guarantee that the K101-D will capture a noise spike as a glitch, the spike must exceed the specified threshold level by at least 25% and have a pulse width at the threshold level of at least 5 ns. A glitch need not be sharp and intense; a lower, longer pulse that has sufficient energy may be captured.



Note: Block diagram of K101-D front-end sampling circuitry. The two pipeline registers serve as a delay to allow time for each sample to be evaluated by the trace control for possible storage.

Figure 5-4. Temporary Sample Registers.



Note: Finding noise spikes between sample clocks is easy with the K101-D's Glitch mode. Any glitches between samples are stored as the next sample instead of the state present at that sample clock.

Figure 5-5. Glitch Mode Used for Noise Spikes.

5.5.1.3 **Latch Mode**

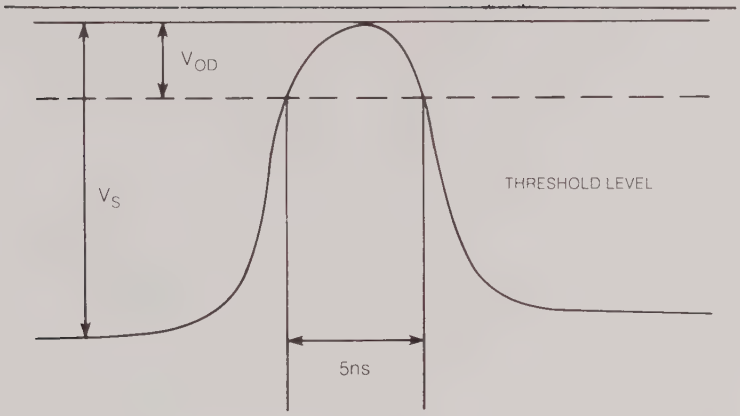
Latch mode is a special case of Sample mode. It allows you to either hold or to pass data to half or all the sample registers of each section (C, B, or A), based on the statuses of separately assignable latch enable clock expressions. Latch mode lets you capture data at one time and sample it at a later time, based on two separate clock expressions; the signals indicating valid data can be completely different in type and timing from the signals indicating the right time to sample that data.

When you select Latch mode, a latch enable clock expression is made active for the chosen inputs. Whenever that specified enable clock expression is true, data pass directly to the corresponding sample clock registers, just as if the inputs were still in Sample mode. When the enable expression goes false, the latch register inputs are disabled. The data present in the latch register at that time are held constant until the enable expression comes true again. Basically, Latch mode is Sample mode under latch control.

The sample clock actually looks at the current contents of the latch register, rather than directly at the data inputs. If the inputs are selected for Latch mode and the latch is enabled at that time, the data transferred to the sample register are the same as if those inputs had been selected for Sample mode. If the Latch is disabled, the data transferred to the sample register are the last data that were present in the latch register when the enable clock expression went false (see Figure 5-7).

5.5.1.4 **Demultiplex Mode**

Demultiplex mode lets you capture data present at two different times on the same bus lines for the later, simultaneous evaluation by the trace control. Typically one uses this mode to capture both address and data



Note: In this typical pattern of a narrow noise spike, V_{OD} is about 25% of V_S. To be captured, a glitch must exceed the threshold level by at least 25% and have a pulse width of at least 5 ns.

Figure 5-6. Typical Glitch Pattern.

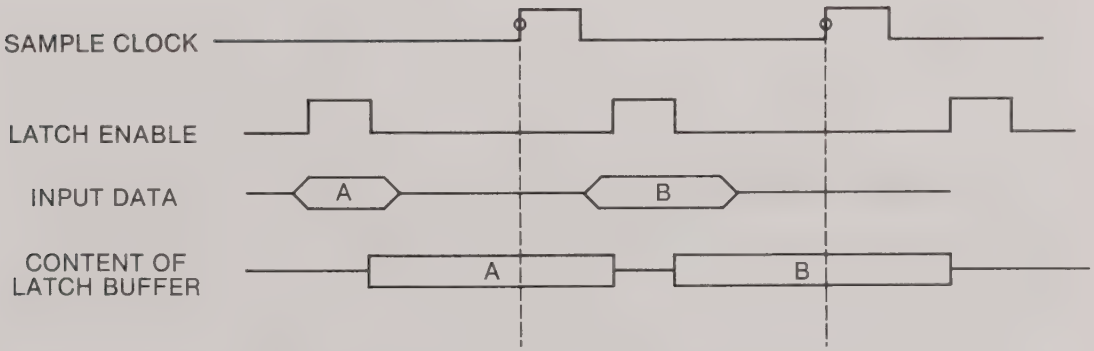


Figure 5-7. Latch Register Holds Event For Sampling (Latch Mode).

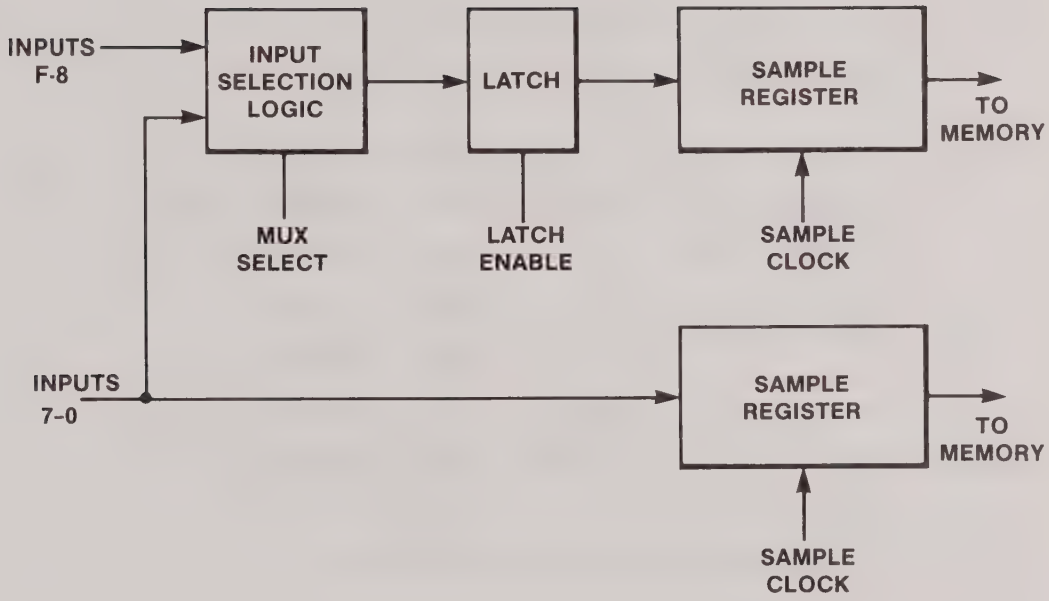
on a shared bus. The data inputs to the lower byte group of the selected section (C, B, or A) are buffered and then sent to both groups of that section (see Figure 5-8). The lower byte group (0 through 7) is automatically placed in Sample mode and the upper byte group (8 through F) in Latch mode. The enable clock expression defined for that section determines when and how the upper byte is sampled, just as in regular Latch mode. The sample clock expression for the section defines when the lower byte is sampled and also when the contents of the upper byte latch are examined. Both bytes are presented to the trace control simultaneously as one valid sample. The term "alignment" is sometimes used to refer to this simultaneous evaluation, capture, and display of two events separate in time.

The Demultiplex mode eliminates the need for double probing, allows more precise trace control, and results in a much more efficient use of memory when investigating multiplexed systems. Loading of your system is kept to same low level (1 megohm, 10 pF) as in normal sampling because only one probe connection is used.

5.5.1.5 **Input Mode Summary**

Sample mode is the most basic input mode. Inputs are sampled only at each active clock edge. Glitch mode is a special case of Sample mode which detects noise spikes or asynchronous threshold crossings between valid sample clocks. Latch mode allows you to capture data at one time and sample the data later, based on clock expressions that may be entirely separate. Finally, Demultiplex mode is a specialized combination of Sample and Latch mode that allows the simultaneous evaluation of two events that occur at different times on the same bus lines.

As this brief summary shows, each mode has its special functions and uses; select modes according to your particular needs. As an example,



Note: The Demultiplex mode allows you to probe multiplexed signals with a single probe. This avoids unnecessary circuit loading and the inconvenience of attaching double probes. The data inputs to the lower byte group of the section in Demultiplex mode are buffered and then simultaneously monitored in both Sample and Latch modes. When the section's sample clock comes true, the data present at that time are sent to the lower byte group of trace memory M and the contents of the latch are sent to the upper byte group.

Figure 5-8. Diagram of Demultiplex Logic.

in a session to verify that a system is operating correctly, you might proceed as follows:

a. Set up the probes and use Sample mode to check basic system functioning and to verify that the probes are properly set.

b. Specify Glitch mode for various areas of investigation to look for problems.

c. Finally, specify Latch mode to check certain groups of signals against each other to verify that they are occurring in proper relationship.

5.5.2 THRESHOLD LEVEL SELECTION

Threshold levels are set from the Input Mode screen. The threshold selection fields are located just to the right of their respective Input mode selection fields (see Figure 5-9). The selection applies to all eight input signals in a probe.

There are four possible threshold settings: fixed TTL (+1.40 V), fixed ECL (-1.30 V), and two variable thresholds, A and B. The variable thresholds can be set to $\pm$9.99 V in 10 mV steps, with 2 mV accuracy. A value specified for a variable applies for all references to that variable. In other words, if two input signal groups use variable A, the most recent setting applies to both.

5.5.3 ARM MODE SELECTION

Arm mode is selected from the Input Mode screen (see Figure 5-9). This mode defines how new data acquisition cycles begin and the conditions required for them to be completed. The choices in this mode -- Manual, Auto, Auto Stop, and Auto Stop Within Limits -- control whether or not the recording process is automatically repeated. Manual mode, for

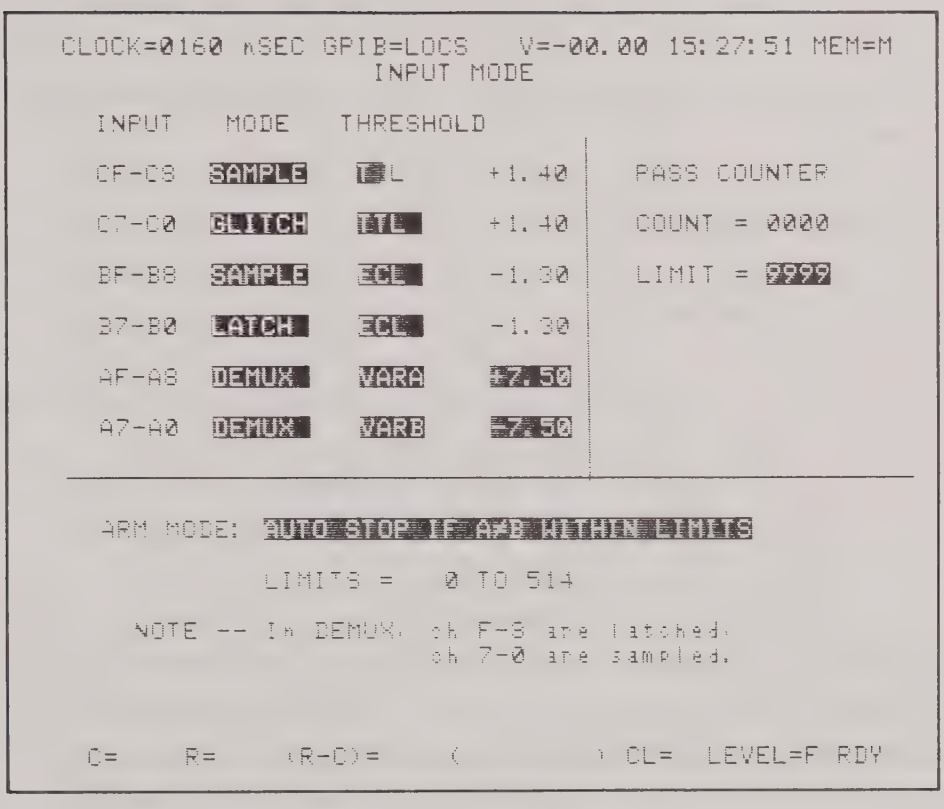

CLOCK=0160 nSEC GPIB=LOCS V=-00.00 15:27:51 MEM=M
INPUT MODE
INPUT MODE THRESHOLD
CF-C8 SAMPLE TTL +1.40
C7-C0 GLITCH TTL +1.40
BF-B8 SAMPLE ECL -1.30
B7-B0 LATCH ECL -1.30
AF-A8 DEMUX VARA +7.50
A7-A0 DEMUX VARB -7.50
PASS COUNTER
COUNT = 0000
LIMIT = 9999
ARM MODE: AUTO STOP IF A#B WITHIN LIMITS
LIMITS = 0 TO 514
NOTE -- In DEMUX: ch F-8 are latched.
ch 7-0 are sampled.
C= R= (R-C)= ( ) CL= LEVEL=F RDY

Figure 5-9. Setting Threshold Levels and Arm Modes.

example, does not repeat, and is usually chosen for the first trial of a recording process. The special and complementary capabilities of the arm modes are discussed in Section 6 (Making a Recording) along with information on the functions of the keys in the ACQUIRE area: **ARM**, **ADVANCE**, **M->A**, and **STOP**.

After an arm mode is chosen, the actual acquisition cycle is initiated by pressing the **ARM** key. When a recording is completed, it is transferred to display memory A, along with the time at which the acquisition was completed.

5.6 CLOCK SELECT SCREENS

5.6.1 GENERAL DESCRIPTION

A prerequisite for efficient logic analysis of a particular test problem is the ability to look at digital data at just the right times. In order to capture relevant data, you must first understand the timing characteristics of your system and how those characteristics relate to the flow of data through the system. Next, you should be able to easily specify the precise clocking scheme needed to investigate that data flow in an efficient manner. To ensure that you have this capability for almost any parallel bus system, the K101-D provides wide variety of directly accessible synchronous and asynchronous clocking arrangements. With the K101-D's Clock Select menu, you can make comprehensive yet selective synchronous (data domain) recordings, precise and detailed asynchronous (time domain) recordings, and mix synchronous and asynchronous recordings during the same acquisition. Sophisticated synchronous external clocking options allow you to easily monitor complex multiplexed and multiphased systems requiring both AND and OR logic control signals for proper definition of valid data. Many asynchronous internal sampling rates offer precise timing resolution from 160 ms to 10 ns. Mixed data acquisitions are available for simultaneous collection of both data and time domain information.

The K101-D's Clock Select menu has six clocking modes, selectable in the following order:

a. Internal
b. External Single-Phase
c. External Multiphase
d. Mixed Single-Phase
e. Mixed Multiphase
f. Internal Extended

These six choices represent three basic modes: internal, external, and mixed, with two choices in each mode. The choices result from the ability to specify an internal or external clock source and to specify sample clock, master clock, or both. A short overview of internal, external, and mixed clocking is given below. A full discussion of these choices follows the explanation of enable clocking.

5.6.2 CLOCKING MODE OVERVIEW

a. Internal

All three sections of data inputs (C, B, and A) are sampled simultaneously by the master internal clock. The sample clock is set to "Same as Master," and the internal clock period can range from 20 nanoseconds to 160 milliseconds. Clocking into memory and the making of trace control decisions are done at the master internal rate.

Use: Timing analysis.

b. Internal Extended

Each section (C, B, or A) can be sampled and traced into memory at one of two rates: the master internal clock rate

("Same as Master") of 20 nanoseconds to 160 milliseconds, or a special internal rate of 10 nanoseconds. Trace control decisions are made at the master internal clock rate, and clocking into memory is done by section at the sample clock rate for the section.

Use: High-resolution timing analysis.

c. External Single-Phase

All sections (C, B, and A) are sampled simultaneously by the external master clock. The sample clock for all sections is "Same as Master." That clock controls both tracing decisions and clocking into memory.

Use: Basic synchronous state analysis.

d. External Multiphase

Each section (C, B, or A) may have a different external clock, which is different from the master external clock. For each section, the sample clock is either a unique external clock expression or the master external clock ("Same as Master"). Although each section can be sampled at its own rate, samples are actually clocked into memory at the master rate. This mode can serve as a reduction technique, because under certain conditions several samples could be taken from a section before a sample is actually clocked into memory. Trace control decisions are made at the master rate.

Use: Advanced synchronous state analysis. For example, this mode could be used with multiphased microprocessors or multiprocessor systems.

e. Mixed Single-Phase

Each section (C, B, or A) may be sampled at one of three choices: the internal clock period (20 nanoseconds to 160 milliseconds); a special internal selection (10 nanoseconds); or the master external rate ("Same as Master"). Internally clocked sections clock into memory at their specified rate, but externally clocked sections are sampled at their rate and clocked at the master rate. Under certain conditions several samples could be taken from a section before a sample is actually clocked into memory. The master rate is used for trace control determination.

Use: Combined timing and state analysis, useful when integrating hardware and software.

f. Mixed Multiphase

Each section (C, B, or A) may be sampled at one of four choices: the internal clock period (20 nanoseconds to 160 milliseconds); a special internal selection (10 nanoseconds); the master external rate ("Same as Master"); or a unique external rate specified by a clock expression. Internally clocked sections clock into memory at their rate, but externally clocked sections are sampled at their rate and clocked at the master rate. Under certain conditions several samples could be taken from a section before a sample is actually clocked into memory. Trace control decisions are made at the master rate.

Use: Debugging of hardware/software integration problems.

Many of the clock specifications are made using a Boolean expression of six terms: three terms "ORed" and three terms "ANDed," with the two

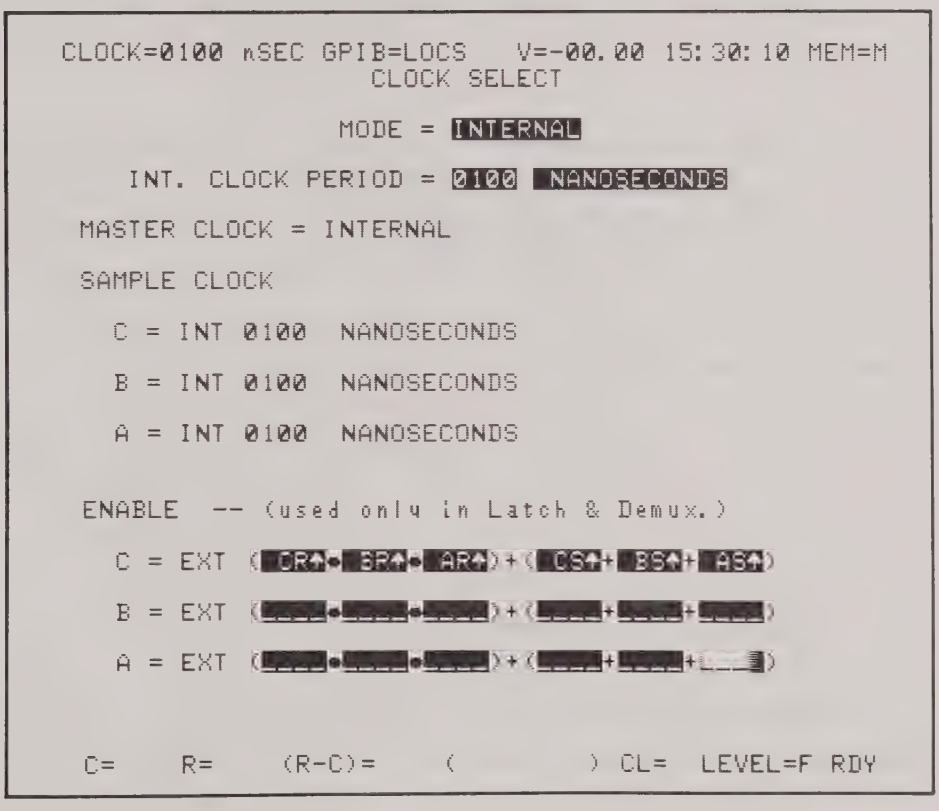
groups "ORed" together. Individual clock terms can be specified as rising or falling active edge (active low or active high), or left out. It may be helpful to think of the six-term Boolean expression as a four-term OR expression, in which one of the terms is made up of a single term or two or three terms "ANDed" together.

The enable clock fields function independently of the specific menu mode and are present in all modes. Before considering each mode separately, therefore, we will first discuss the function and use of the enable clock fields.

5.6.3 ENABLE CLOCKS

The enable clocks are formed by Boolean expressions of six separate latch enable clocks (see Figure 5-10). These clocks are level-sensitive and are used to gate or hold data in high-speed input latches for possible later examination by their respective section's Sample clock expression.

This capability is useful in several application areas such as collecting data from systems with a multiplexed bus, collecting data from systems requiring a negative hold time for the clocks relative to the data, and for filtering irrelevant data from timing acquisitions. When you are collecting data from a multiplexed bus, the enable fields let you define the control signal(s) for sampling and holding the data that first come valid on the bus; these data are then presented to the trace control simultaneously with the data that come valid later on the bus, as defined by that section's sample clock expression. When you are collecting data from a system requiring a negative hold time for the clocks relative to the data, the enable fields let you use some earlier signal (such as the system's primary clock) to capture the data while still valid and hold the data until the correct sample clock comes true (such as the system's READ and WRITE signals, which allow more efficient data capture).


CLOCK=0100 nSEC GPIB=LOCS V=-00.00 15:30:10 MEM=M
CLOCK SELECT
MODE = INTERNAL
INT. CLOCK PERIOD = 0100 NANOSECONDS
MASTER CLOCK = INTERNAL
SAMPLE CLOCK
C = INT 0100 NANOSECONDS
B = INT 0100 NANOSECONDS
A = INT 0100 NANOSECONDS
ENABLE -- (used only in Latch & Demux.)
C = EXT (CR↑•BR↑•AR↑)+(CS↑+BS↑+AS↑)
B = EXT (•••)+(•••)
A = EXT (•••)+(•••)
C= R= (R-C)= ( ) CL= LEVEL=F RDY

Note: The six enable clocks are shown on the lower third of this Clock Select screen, all selected for a rising edge or high state in section C.

Figure 5-10. Enable Clocks.

You can use certain control signals to accomplish very sophisticated filtering of data for timing analysis. These control signals indicate known invalid time periods on the system's bus (such as when the bus is floating or tristated). They prevent these irrelevant states from being presented to the trace control, which would result in the capture of incorrect data.

The current input mode selected for section is the sole determinant of whether that section's enable clock expression is pertinent for a given recording. If either Latch or Demux mode is selected for an input group, then the enable expression will be active and control the data latch for those inputs. If either Sample or Glitch mode is selected, then the enable expression for that group is irrelevant.

If either Latch or Demux mode is selected, then, when the expression used for an enable field is true, data pass transparently through the input latches. When the expression goes false, the data present at that time are held in the input latches indefinitely until the expression comes true again. The expression is true when either all three AND clocks are true or when any of the OR clocks is true. The three AND enable clocks are CR, BR, and AR. The three OR enable clocks are CS, BS, and AS. The same clocks are used to define the enable fields for all three sections and are presented in the same order. Totally different expressions are possible for each section, however, because each clock field can be selected as either active high or active low or can be excluded from the expression (see Figure 5-11).

5.6.4 INTERNAL MODE

Internal mode allows you to make asynchronous timing measurements with resolution from 160 ms to 20 ns. All three sections are sampled simultaneously at the master clock rate, which is entered into the internal clock period field (see Figure 5-12). This field is broken into two subfields. The first subfield is used to enter the numerical

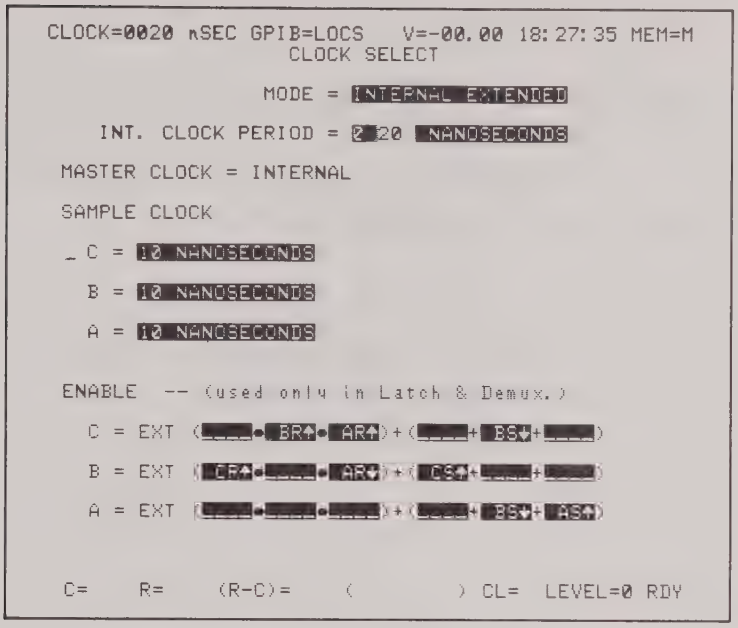

CLOCK=0020 nSEC GPIB=LOCS V=-00.00 18:27:35 MEM=M
CLOCK SELECT
MODE = INTERNAL EXTENDED
INT. CLOCK PERIOD = 020 NANOSECONDS
MASTER CLOCK = INTERNAL
SAMPLE CLOCK
C = 10 NANOSECONDS
B = 10 NANOSECONDS
A = 10 NANOSECONDS
ENABLE -- (used only in Latch & Demux.)
C = EXT (BR↑•AR↑)+(BS↓)
B = EXT (CR↑•AR↓)+(CS↓)
A = EXT (BS↓+AS↑)
C= R= (R-C)= ( ) CL= LEVEL=0 RDY

Figure 5-11. Examples of different Enable expressions specified for each section.

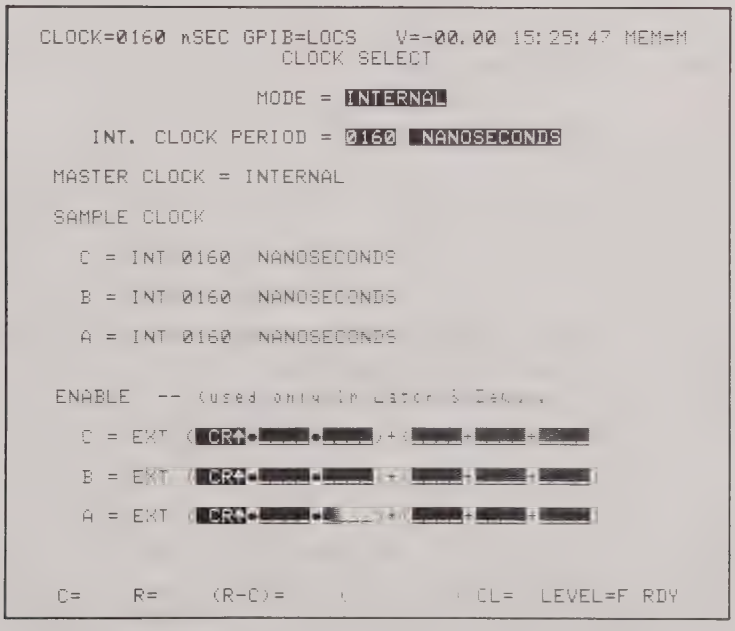

CLOCK=0160 nSEC GPIB=LOCS V=-00.00 15:25:47 MEM=M
CLOCK SELECT
MODE = INTERNAL
INT. CLOCK PERIOD = 0160 NANOSECONDS
MASTER CLOCK = INTERNAL
SAMPLE CLOCK
C = INT 0160 NANOSECONDS
B = INT 0160 NANOSECONDS
A = INT 0160 NANOSECONDS
ENABLE -- (used only in Latch & Demux.)
C = EXT (CR↑•
B = EXT (CR↑•
A = EXT (CR↑•
C= R= (R-C)= ( ) CL= LEVEL=F RDY

Figure 5-12. Internal Mode Clock Select Screen.

value of the sample rate and the second subfield is used to specify the units used for sampling. No other fields need to be entered in this mode, unless you are using the enable clock fields (which, as mentioned earlier, are specifiable from any mode).

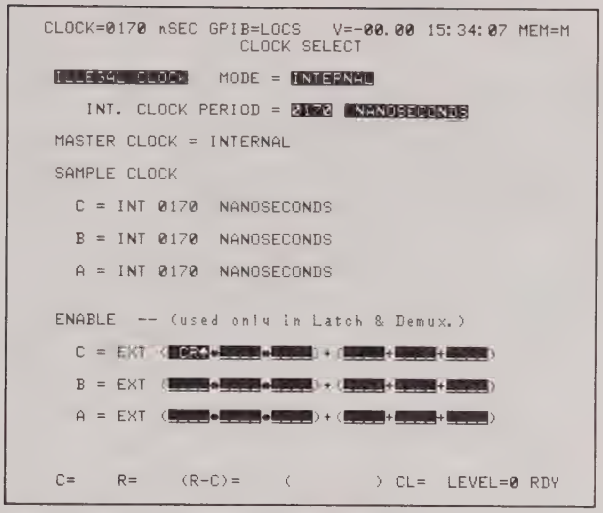
When selecting the desired sample rate, the units used for sampling (nanoseconds, microseconds, or milliseconds) are selected first. This will help you to choose a legal numerical sample rate since some values are not legal for some units. Valid rates are selectable in a 1 through 16 sequence. For example, rates such as 10, 20, 30, and 40 microseconds (i.e., multiples of 10, up through 160 microseconds) are all valid choices, whereas rates such as 11, 24, 78, and 170 microseconds (which do not follow a 1 through 16 sequence) are not valid choices.

If you try to enter an illegal clock rate, the error message ILLEGAL CLOCK will appear (see Figure 5-13). You will be locked out from leaving the internal clock period field until a valid rate is selected.

5.6.5 EXTERNAL SINGLE-PHASE MODE

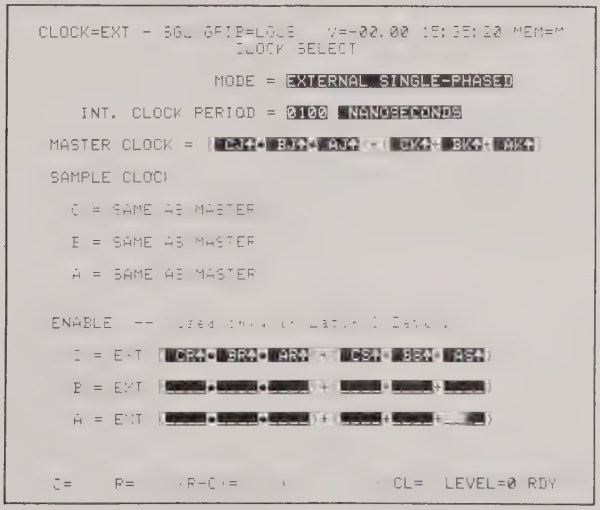
The External Single-Phase mode uses the master clock to synchronously sample all three sections. This master clock is formed by a menu-driven, Boolean expression consisting of six separate sample clock fields (see Figure 5-14). The form of this expression is identical to that of the expressions used for the enable clock fields (three AND clocks "ORed" with three OR clocks). The six sample clocks, however, are edge sensitive, rather than level sensitive like the six enable clocks.

The master clock expression is used not only to control the data presented to the trace control but also for accumulating the sample count within each trace control level whenever clock delay is used. The trace control, on a sample by sample basis, can enable or disable the capture of data for all three sections.


CLOCK=0170 nSEC GPIB=LOCS V=-00.00 15:34:07 MEM=M
CLOCK SELECT
ILLEGAL CLOCK MODE = INTERNAL
INT. CLOCK PERIOD = 0170 NANOSECONDS
MASTER CLOCK = INTERNAL
SAMPLE CLOCK
C = INT 0170 NANOSECONDS
B = INT 0170 NANOSECONDS
A = INT 0170 NANOSECONDS
ENABLE -- (used only in Latch & Demux.)
C = EXT
B = EXT
A = EXT
C= R= (R-C)= ( ) CL= LEVEL=0 RDY

Note: Correct selections of the internal clock rate are aided by the error message ILLEGAL CLOCK which appears whenever a nonvalid rate is chosen.

Figure 5-13. Illegal Clock Display.


MODE = EXTERNAL SINGLE-PHASED
INT. CLOCK PERIOD = 0100 NANOSECONDS
SAMPLE CLOCK
C = SAME AS MASTER
B = SAME AS MASTER
A = SAME AS MASTER

Note: The six sample clocks are shown as the master clock expression, all selected for a rising edge or active low state. The six enable clocks are also shown as the latch enable expression for section C.

Figure 5-14. Master Clock Expression.

When the expression used for the master clock comes true, the data present at that time pass through the pipeline for evaluation, by the trace control, as a potentially valid sample for memory M. The expression is true when either all three AND clocks are true or when any of the OR clocks is true. The three AND sample clocks are CJ, BJ, and AJ. The three OR sample clocks are CK, BK, and AK. The selections for each clock field are active high, active low, and not selected.

5.6.6 EXTERNAL MULTIPHASE MODE

The External Multiphase mode (see Figure 5-15) allows you to specify a separate sample clock expression for each section in addition to specifying the master clock expression. When recording in this mode, the data for each section are first clocked into a sample register under the control of that section's sample clock expression. Every time a sample clock expression comes true, new data are placed in that section's sample register and the old data are discarded. When the master clock expression comes true, the current contents of the registers of all three sections are sent through the pipeline to be evaluated concurrently by the trace control. Regardless of whether that master sample is stored, if delay by clocks is being used in the current trace control level, one count is added to the sample counter in that level.

The form and entry of the sample clock expressions are exactly the same as for the master clock expression and use the same six clock inputs.

5.6.7 MIXED SINGLE-PHASE MODE

The Mixed Single-Phase mode (see Figure 5-16) lets you record asynchronous timing information in one or more sections while using an external clock defined by the master clock expression. This allows you to present synchronous data to the trace control and to record that data in the sections selected for external clocking. Each section's sample

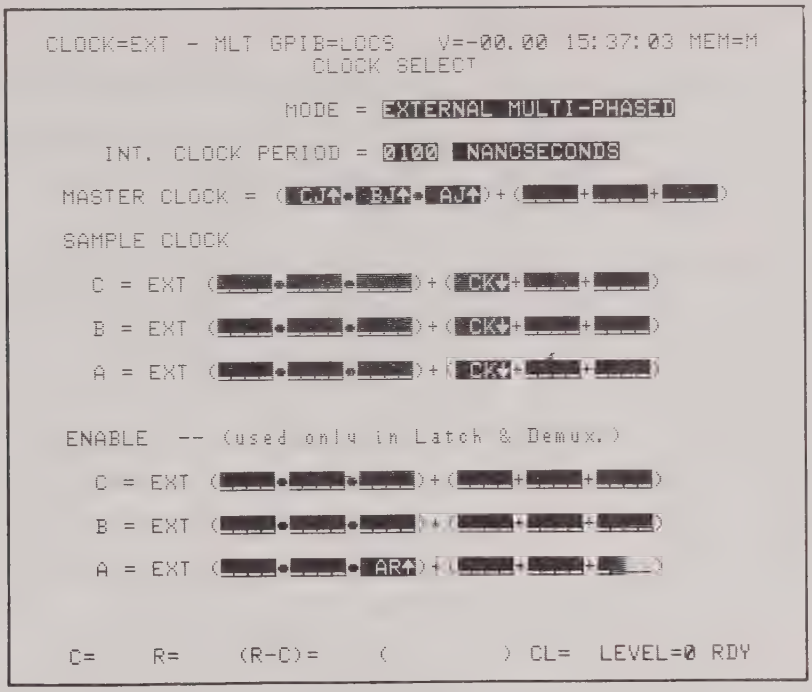

CLOCK=EXT - MLT GPIB=LOCS V=-00.00 15:37:03 MEM=M
CLOCK SELECT
MODE = EXTERNAL MULTI-PHASED
INT. CLOCK PERIOD = 0100 NANOSECONDS
MASTER CLOCK = (CJ↑ • BJ↑ • AJ↑) + (+ +)
SAMPLE CLOCK
C = EXT (• •) + (CK↓ + +)
B = EXT (• •) + (CK↓ + +)
A = EXT (• •) + (CK↓ + +)
ENABLE -- (used only in Latch & Demux.)
C = EXT (• •) + (+ +)
B = EXT (• •) + (+ +)
A = EXT (• • AR↑) + (+ +)
C= R= (R-C)= ( ) CL= LEVEL=0 RDY

Figure 5-15. External Multiphase Mode Clock Select Screen.

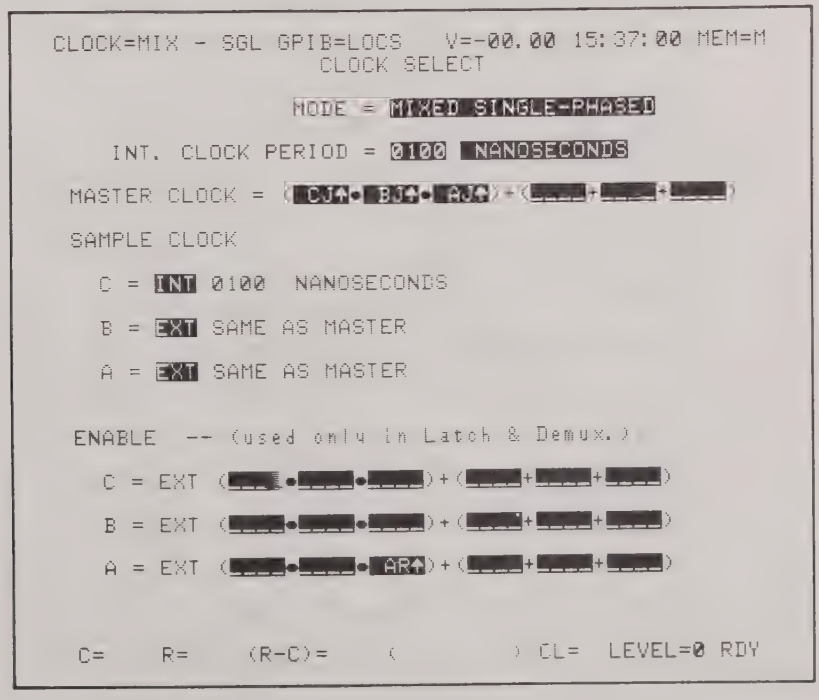
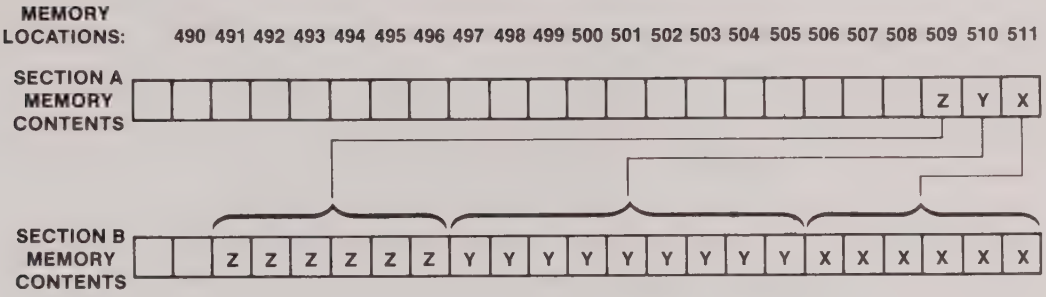

CLOCK=MIX - SGL GPIB=LOCS V=-00.00 15:37:00 MEM=M
CLOCK SELECT
MODE = MIXED SINGLE-PHASED
INT. CLOCK PERIOD = 0100 NANOSECONDS
MASTER CLOCK = (CJ↑ • BJ↑ • AJ↑) + (+ +)
SAMPLE CLOCK
C = INT 0100 NANOSECONDS
B = EXT SAME AS MASTER
A = EXT SAME AS MASTER
ENABLE -- (used only in Latch & Demux.)
C = EXT (• •) + (+ +)
B = EXT (• •) + (+ +)
A = EXT (• • AR↑) + (+ +)
C= R= (R-C)= ( ) CL= LEVEL=0 RDY

Figure 5-16. Mixed Single-Phase Mode Clock Select Screen.

clock can be selected for either the "Same As Master" or for the currently specified internal clock period by selecting either EXT or INT, respectively. When EXT is selected, "Same As Master" appears in the second half of the field. When INT is selected, the current internal clock period appears in the second half of the field. Note that when all three sections are selected for EXT, the unit records just as though it was selected for External Single-Phase mode. Alternately, by selecting all three sections for INT, you can capture asynchronous timing information from all 48 inputs simultaneously, and still use an externally derived master clock expression to present only valid synchronous data to the trace control.

Note

For successful analysis of recordings made in the mixed clocking modes, you must consider the correlation among data captured in separate sections using different sample rates. No fixed relationship exists among the data presented to the trace control, or the data captured in the externally clocked section(s). As each consecutive external clock occurs, an additive skew accumulates between preceding external clocks and the corresponding timing information (see Figure 5-17 for a typical example). The time between clocks is not constant because the master clock expression forming the clocks is usually composed of several control signals, the timing of which is dependent on the types of instructions and machine cycles being executed. The best way to synchronize the data captured between sections is to record the signals used to form the master clock


MEMORY LOCATIONS:
490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511
SECTION A MEMORY CONTENTS
Z Y X
SECTION B MEMORY CONTENTS
Z Z Z Z Z Z Y Y Y Y Y Y Y Y Y X X X X X X

Note: Mixed mode acquisitions by definition contain information captured with unrelated, asynchronous clock signals. In this example the entire memory contents of Section B was captured during the same period of time that the last few words were captured in Section A.

Figure 5-17. Example of Skew Accumulation from Mixed Mode Clocking.

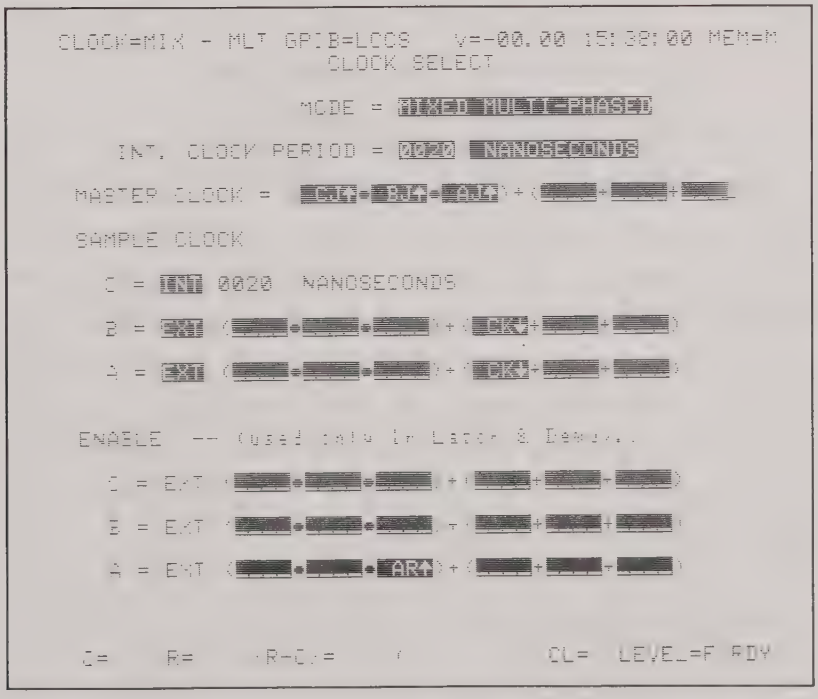


Figure 5-18. Mixed Multiphase Mode Clock Select Screen.

expression on some unused inputs of the asynchronous section(s). In the asynchronous section(s) for which the master clock comes true, every location (beginning with the word just before the end of memory, i.e., location 513, P-1) corresponds to one sample in the synchronous section(s).

5.6.8 MIXED MULTIPHASE MODE

The Mixed Multiphase mode (see Figure 5-18) extends the Mixed Single-Phase mode to allow you to use separate external sample clock expressions for each section. An external master clock expression is always used to present data to the trace control. Each section can be selected for either EXT or INT. When EXT is selected, you can enter an expression for that section's sample clock. This expression can be the same as, or entirely different from, the expression used for the master clock expression.

When the external sample expression(s) used is just the same as the master clock expression, the unit records data in that section as though in External Single-Phase mode. When a different external sample expression is used, recording for that section occurs as though in External Multiphase mode. When a section is selected for INT, that section is sampled at the rate currently specified in the internal clock period field; recording occurs as though in Mixed Single-Phase mode. Entry is very similar to that for Mixed Single-Phase mode except that when EXT is selected for a section, that section's sample clock expression appears next to the EXT.

5.6.9 INTERNAL EXTENDED MODE

The Internal Extended mode (see Figure 5-19) allows you to make asynchronous recordings at a 10 ns (100 MHz) sampling interval for very high

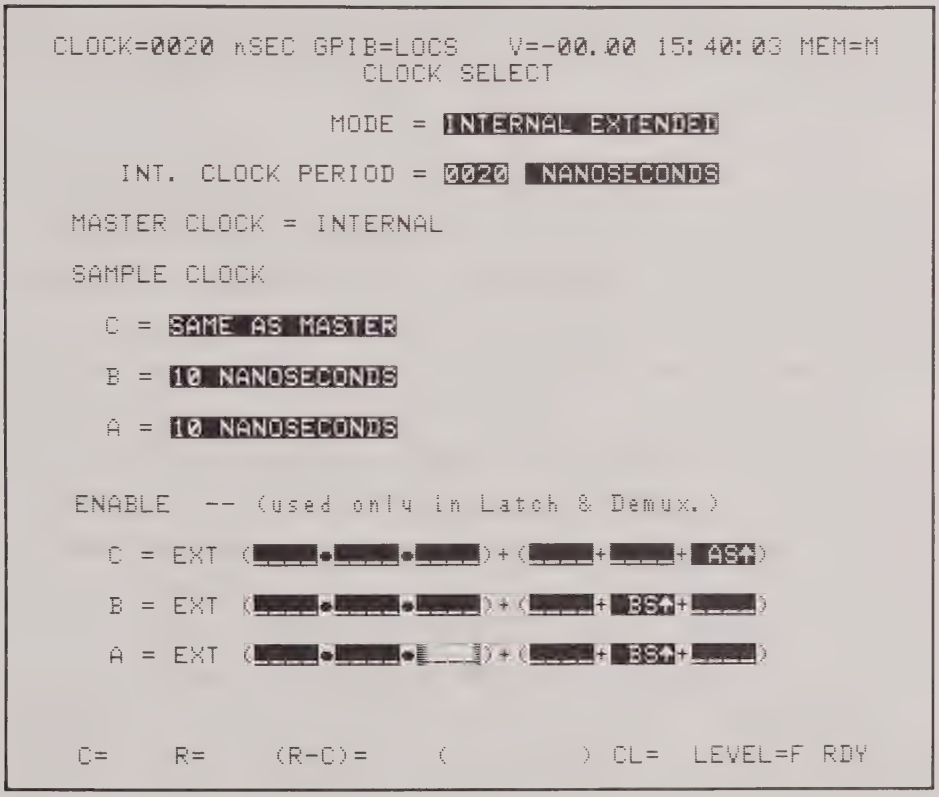

CLOCK=0020 nSEC GPIB=LOCS V=-00.00 15:40:03 MEM=M
CLOCK SELECT
MODE = INTERNAL EXTENDED
INT. CLOCK PERIOD = 0020 NANOSECONDS
MASTER CLOCK = INTERNAL
SAMPLE CLOCK
C = SAME AS MASTER
B = 10 NANOSECONDS
A = 10 NANOSECONDS
ENABLE -- (used only in Latch & Demux.)
C = EXT (• •)+(+ + AS↑)
B = EXT (• •)+(+ BS↑+)
A = EXT (• •)+(+ BS↑+)
C= R= (R-C)= ( ) CL= LEVEL=F RDY

Figure 5-19. Internal Extended Mode Clock Select Screen.

resolution of system timing characteristics. All three sections are capable of simultaneously recording at a 10 ns rate and can be individually selected for that rate via this mode. The master clock is also selected for an internal rate (any legal clock from 160 ms to 20 ns) using the standard internal clock period field. Each section can be sampled either at that slower rate or at 10 ns intervals. To set the desired option for each section, select either "10 nanoseconds" or "Same As Master."

The master clock is selected for a slower rate to ensure that the trace control functions properly. Due to the complexity of the decisions that the trace control must make between every sample, 20 ns is the fastest rate at which data can be reliably evaluated. While this point should be understood, in practice it proves to be a minor restriction.

When you change levels or use conditional trace in this mode, the captured data may shift a sample or two at the decision points because of the difference in sample rates between the section(s) and the trace control. For example, if the trace control is clocked at 20 ns intervals and the sections are clocked at 10 ns intervals, the resulting recording will have an uncertainty at each trace decision point of ±20 ns rather than ±10 ns. At all other points in the trace the actual data will be recorded with a ±10 ns accuracy.

Note

The same type of additive skew discussed in connection with mixed clocking occurs in the Internal Extended mode if you select sections to sample at different rates (either not all "10 nanoseconds" or not all "Same as Master"). Since the internal rates are constant ratios of one another, however, this skew between sections accumulates at a constant rate. Once understood,

you can use this mode to gather data covering a longer time period with a lower resolution and a shorter time period with a higher resolution, both tied to the same recording parameters and traced during the same acquisition. If all three sections are operated at the same rate, no skew occurs.

5.7 DATA FORMAT SCREENS

By changing the Data Format screen specifications, you can control the manner in which the 48 data inputs of the K101-D are grouped and displayed. The Data Format screen determines the format available for trace control, for the search field, and for the data display format, which is used to display the contents of memories A and B. The top half of the menu is used to specify data format; the bottom half is used for entering search words.

Five of the six basic format choices are always available: "Mixed User Seqn" (mixed radices, user-defined sequence); "Mixed CF-A0 Seqn" (mixed radices, fixed sequence); and three fixed sequences, "Hex," "Octal," and "Binary." A sixth choice, "Device Mnemonics," is available only when using an RTE-816; it shows the disassembly data format used for those devices. The two mixed format screens are the only ones that allow you to specify radices or data display formats. The selections for these two screens are binary, octal, hexadecimal, ASCII, and EBCDIC formats. The Hex, Octal, and Binary screens specify fixed display of all inputs in the chosen format. Only one data format can be used at a time (i.e., the one that was last selected).

5.7.1 FIXED FORMATS

There are three fixed formats: hexadecimal, octal, and binary. They provide a fixed display of all 48 data inputs, in the order CF through A0. No editing is available in fixed mode.

a. Fixed hexadecimal: Inputs are grouped by four, forming a hexadecimal character. Each section (C, B, and A) forms a separate word (see Figure 5-20).

b. Fixed octal: Inputs are grouped by three, forming four words composed of four octal characters (see Figure 5-21).

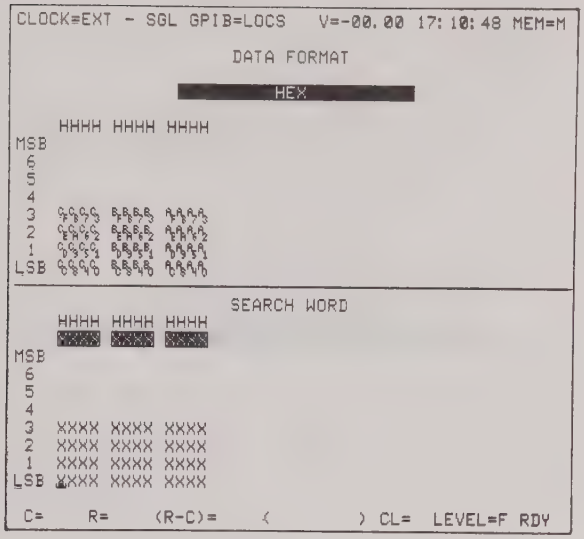
c. Fixed binary: Each input is displayed as a binary value (see Figure 5-22).

Fixed display is quick and easy to specify. Mixed modes are more involved to specify but give flexibility and allow the placement of an input signal in more than one group.

5.7.2 MIXED RADICES, FIXED SEQUENCE

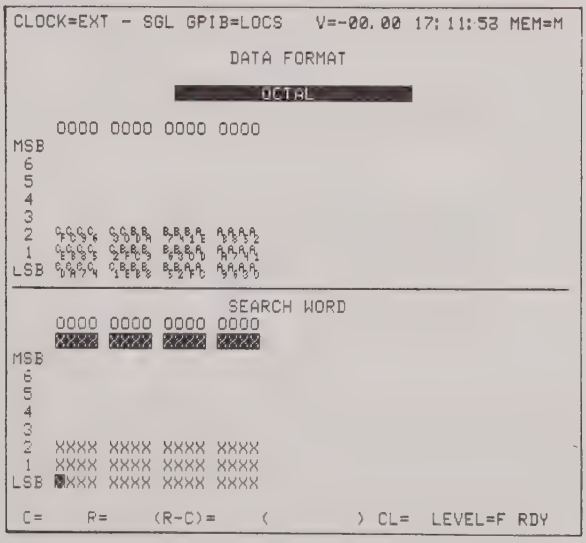
This screen (see Figure 5-23) allows you a choice of five formats but restricts you to the fixed sequence (CF through A0). Separate entry of each input signal is eliminated, although the fixed sequence can be inconvenient. Which format screen is best to use for a particular application depends on the relative difficulty of attaching the probes to your system in a fixed sequence vs. attaching the probes in any convenient manner and then entering each input separately to define each character.

Only the column specification field is used in this mode. As you specify the format for each character, data inputs are be automatically assigned to form each character, beginning with data input CF. If all



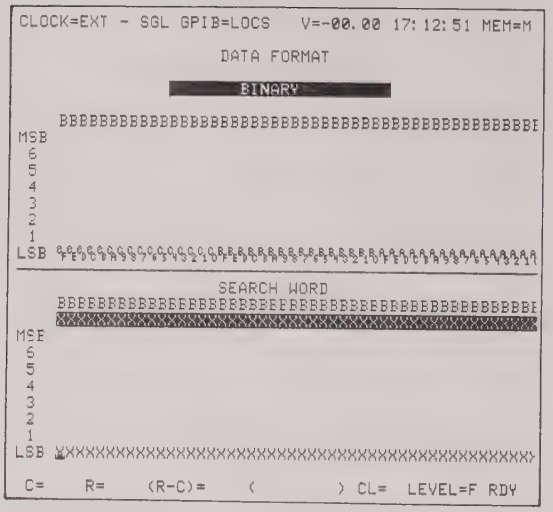
Note: A fixed hexadecimal display lets you quickly review all data input formatted as hexadecimal characters.

Figure 5-20. Fixed Hexadecimal Display.



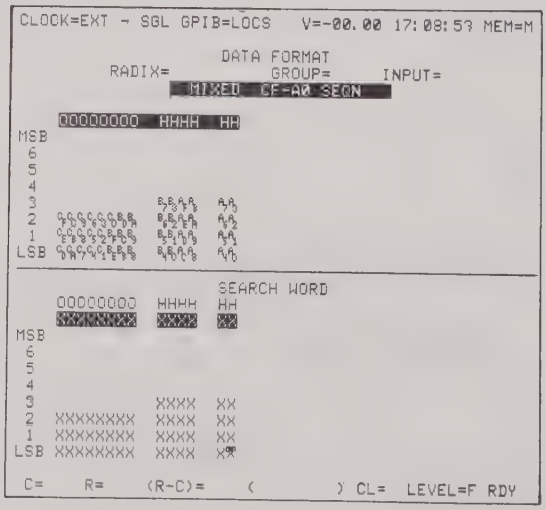
Note: A fixed octal display lets you quickly review all data input formatted as octal characters.

Figure 5-21. Fixed Octal Display.



Note: A fixed binary display lets you quickly review all data inputs individually as binary characters.

Figure 5-22. Fixed Binary Display.



Note: This screen provides flexible format definition for each character and automatically assigns the data inputs needed to form those characters.

Figure 5-23. Mixed Format, Fixed Sequence Data Format Screen.

of the inputs through A0 are assigned, the next input selected is again CF. You may specify as many characters as you need in whatever format (binary, octal, hex, ASCII, or EBCDIC) you desire.

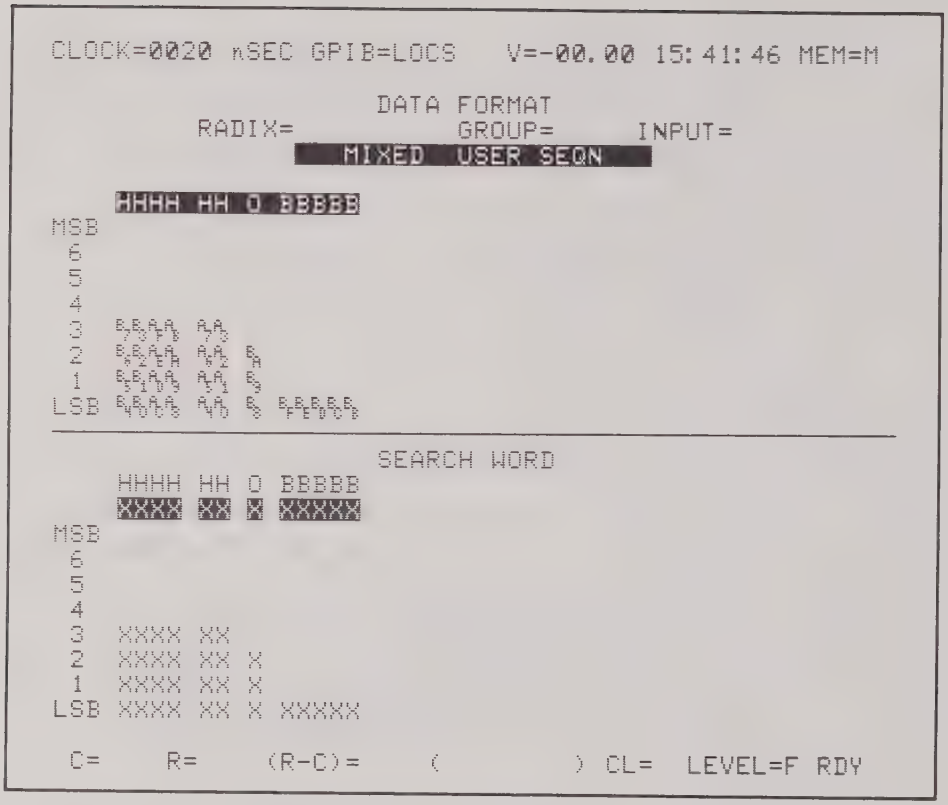
The choice between the two mixed radices screens -- fixed sequence or user-defined sequence -- is a trade-off of convenience in specification vs. flexibility in use. Fixed sequence eliminates the need to separately enter each input, but it constrains the grouping of inputs and does not allow multiple use of an input signal. User-defined sequence gives complete flexibility at the cost of more specification.

5.7.3 MIXED RADICES, USER-DEFINED SEQUENCE

This screen provides the most flexible data formatting available. Up to 48 separate columns of data characters can be specified for simultaneous display. Each character is defined using the format of your choice, and each format is composed using the data inputs of your choice. Binary, octal, hex, ASCII, and EBCDIC characters can all be mixed as desired to show data in whatever format is best suited to your system and application, and you can use an input in more than one definition.

Character placement and definition are accomplished by using the column specification field (see Figure 5-24). Use direct entry (EBCDIC, ASCII, hex, octal, or binary) to select the desired format for that column. The cursor then drops into that column's character definition field, to the location of the most significant bit needed to define that character in the chosen format. Each data input is identified first by its section (C, B, or A), then by its location within that section as input (F through 0). Use direct entry (C, B, or A followed by F through 0) to identify the desired data input for position. Each data input can be used as many times as needed in any column or position desired.

Once you have entered a character definition field you must enter all the data inputs needed for the specified radix. However, if you make a



Note: Your choice of binary, octal, hexadecimal, ASCII, and EBCDIC formats. Using any of the 48 data inputs whenever you want, you can form up to 48 columns of separately defined characters for data displays.

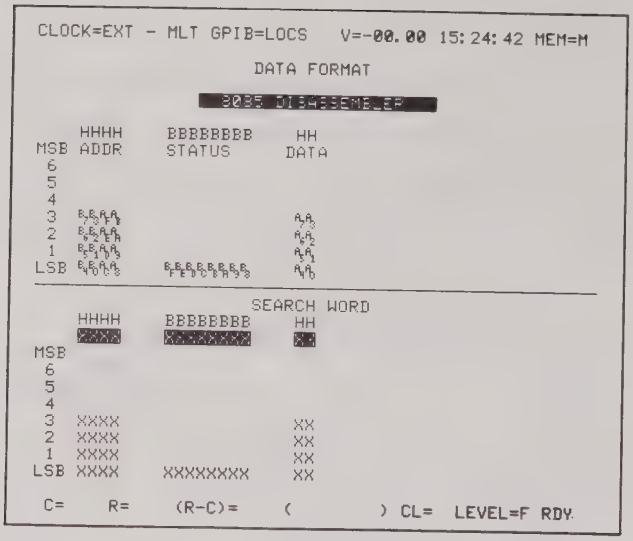
Figure 5-24. Mixed Format, User Sequence Data Format Screen.

mistake and enter the field accidentally or realize halfway through that you are specifying the wrong character, you can press the **DELETE** key to cancel character definition for that column. The partially specified character will be immediately eliminated and the cursor will return to the column specification field.

The **INSERT** and **DELETE** keys allow you to quickly change and rearrange the Data Format screen in either of the mixed formats. Whenever you are in the column specification field, pressing the **INSERT** key inserts a space at that location by moving the currently specified character for that column and all following columns one space to the right. By repeatedly pressing or holding down the **INSERT** key, you can add as many spaces as you want (until the rightmost defined character reaches the end of the column specification field, which means the maximum number of 48 columns has been defined). Each space can either be left as a space or used to enter a new character. Pressing the **DELETE** key while in the column specification field eliminates whatever character is specified for that column and moves all following columns one space to the left. You can delete all but the last character by repeatedly pressing or holding down the **DELETE** key; at least one specified column must be left somewhere on the screen. **SHIFT, DELETE** removes all columns to the right of the field cursor.

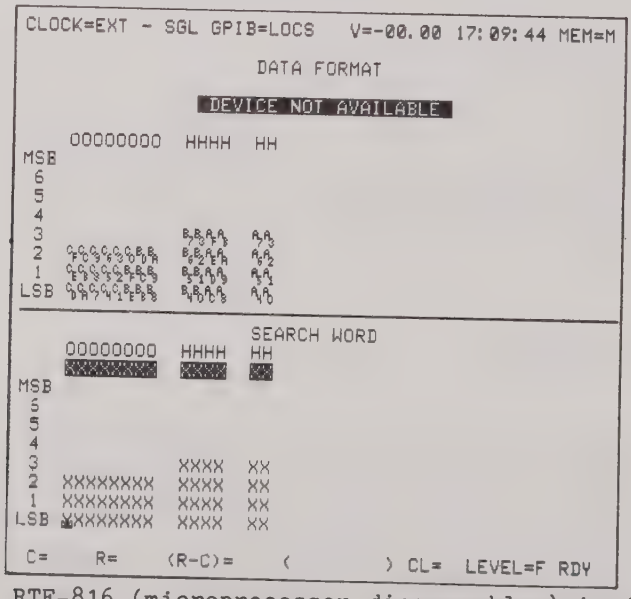
5.7.4 DEVICE MNEMONICS

This screen (see Figure 5-25) is available only with the RTE-816 Microprocessor Execution Disassembly Module. This module must be attached to the K101-D and must show the necessary format for disassembly of microprocessor program flow. A fixed format of address, status, data, and flags is provided, depending on the microprocessor the module supports. If no module is connected, "Device Not Available" will flash in the screen selection field whenever this choice is made (see Figure 5-26). No editing is available in this mode.



Note: The 8085 Disassembler Data Format screen is an example of a Device Mnemonics display.

Figure 5-25. Device Mnemonics Display.



Note: When no RTE-816 (microprocessor disassembler) is in use, paging to the Device Mnemonics screen shows the preceding mixed format selection and the message "Device Not Available."

Figure 5-26. "Device Not Available" Message.

5.8 TRACE CONTROL SCREENS

When the most efficient and applicable input, clocking, and data formatting have been determined, you still have to isolate the essential portions of your system's program activity. Even when only valid and qualified data samples are considered, a typical digital system processes several million bytes of data per second. Capturing and reviewing more than a very small portion of that data in an intelligent manner can be a task ranging from tedious and impractical to humanly impossible. Earlier logic analyzers tackled this problem by offering a variety of features designed to help you capture a narrowly defined "window" of activity around some very specific event in the program flow. Features such as combinational triggering (bit-pattern recognition), delay by clocks, delay by events, multilevel triggering, and selective trace (trace only when certain data inputs are in specified states) provided a means of precisely defining the desired window.

While these triggering features are sufficient in many cases, they provide no means of capturing data separated in time by any significant number of samples. Only selective trace offers any means of recording time independent data and these data are restricted to tasks such as monitoring the status of an I/O port or specific memory location.

Often, the true causes of a program aberration occur a relatively long time before their effects are observed. Gaining an understanding of the interaction requires gathering segments of data around several separate areas of program activity rather than around just one area or only at one location.

The conditional trace control of the K101-D allows you to isolate and capture the essential portions of your system's program activity in a single, compact recording, even if they are widely separated in the program flow. Trace control offers multilevel trace combined with sophisticated control commands that incorporate both pattern recognition

and delay qualification. These features allow rapid capture of complex and otherwise unobtainable data. In addition to all of the previously mentioned means of capturing information, trace control provides these powerful new capabilities.

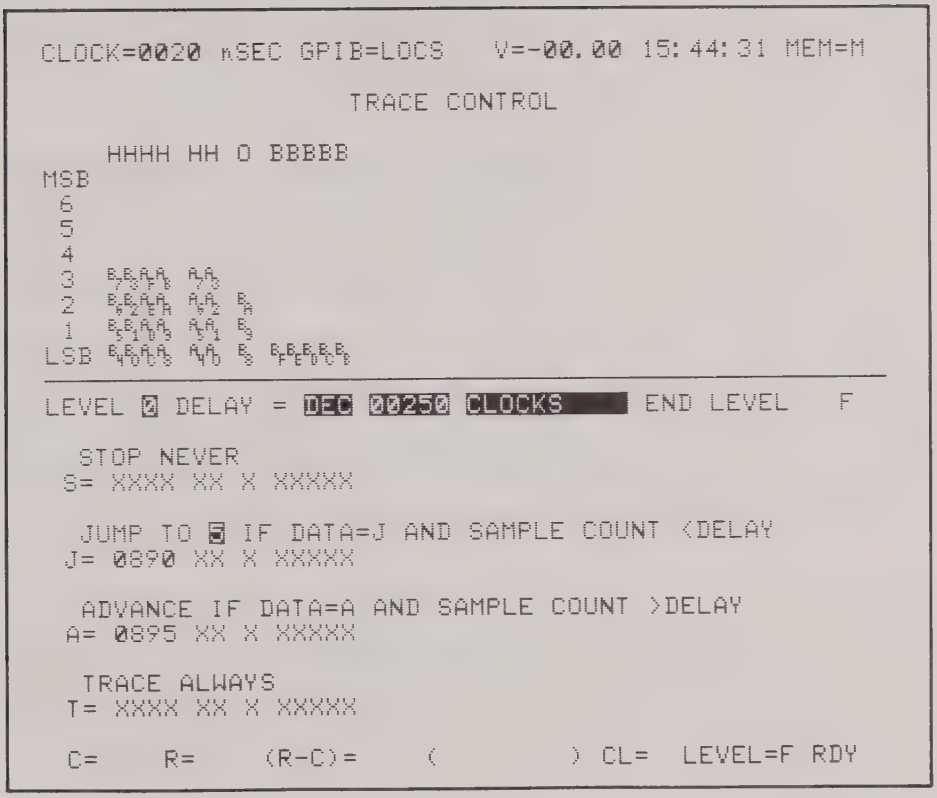
Once you have specified the other recording parameters, you will probably find that these screens are the primary ones that you will change when you want to make new recordings. Up to 16 separate trace control levels (0 through F) can be specified for each recording. Trace control always begins at level 0. The level on which trace control stops and the number of levels used for each recording are user-specified; you only have to enter the number of levels required. Each level, identical in form to the others, has its own menu screen for changing and reviewing that level's specifications. The specifiable parameters are contained on the bottom half of the screen (see Figure 5-27). The top half of the screen shows the currently specified data format: you can readily see which inputs were used to define each character of the data patterns (which you can use within the level's conditional commands).

5.8.1 TYPES OF TRACE CONTROL

An individual delay count and four basic conditional commands (STOP, JUMP, ADVANCE, and TRACE) are offered at each level.

5.8.1.1 **DELAY**

Delay can be entered as either a decimal or hex number. Any value from 1 to 65,535 decimal counts (1 to FFFF in hex) is acceptable. The sample count used for delay is specifiable using either occurrences of the master clock or of the level's advance pattern. The sample count is re-initialized by each level entry.



Note: This Trace Control screen shows the current level 0 selections that will be used for capturing the next recording in memory M.

Figure 5-27. Trace Control Parameter Specification.

5.8.1.2 **STOP**

Nine different commands can be used to immediately stop tracing: STOP IF DATA = S; STOP ALWAYS; STOP NEVER; and STOP IF DATA = S AND SAMPLE COUNT >, <, =, ≥, ≤, OR ≠ DELAY. "S" may be any noncontradictory data pattern possible given the current format of the 48 data inputs shown at the top of the screen. All logical values for each specified character can be entered in "S," including "Don't Care" states.

Various combinations of the nine STOP commands allow you to specify all logical relationships of the stop pattern, delay, and sample count including STOP ALWAYS and STOP NEVER. These commands are independent of any conditions other than whether the trace control is currently active in that level. STOP IF DATA = S allows you to use the stop pattern independently of Delay. The remaining commands require both the stop pattern to be true and the sample count to have the specified relation to delay. By entering all "Don't Cares" in the stop pattern field, you can effectively use only delay as the stop condition.

Each of the other three basic trace control commands (JUMP, ADVANCE, and TRACE) offers the same types of conditional commands and are used in the same manner. STOP has priority over the JUMP and ADVANCE commands; if all three come true simultaneously, the unit will stop.

5.8.1.3 **JUMP**

If the specified conditional command for JUMP comes true, trace control jumps immediately to the user-defined level (0 through F). The same nine types of commands are available as for STOP, except that JUMP replaces STOP as the command word and "J" replaces "S" for the pattern label. A JUMP can be used for either a partial or total sequence restart of the recording or to follow an alternate data path. Since the trace control looks for all four conditional command patterns simultaneously, the nature of the JUMP and ADVANCE commands allow you to also

use them as "ORed" trace patterns. JUMP has priority over the ADVANCE command; if both commands come true simultaneously, the unit executes the JUMP command.

5.8.1.4 **ADVANCE**

When the ADVANCE command comes true, the trace control advances immediately to the next level. The same nine types of commands are available for ADVANCE as for STOP; again, ADVANCE replaces STOP as the command word and "A" replaces "S" for the pattern label. Using the various ADVANCE commands where appropriate in each level allows you to follow extremely intricate sequential program behavior.

5.8.1.5 **TRACE**

Selective trace recording of each valid data sample is decided based on whether or not that sample meets the level's specified trace conditions. These conditions are defined using the same nine types of commands available for STOP. TRACE replaces STOP as the command word and "T" replaces "S" for the pattern label.

TRACE commands are not prioritized relative to the STOP, JUMP, or ADVANCE commands; if one of these commands comes true, the unit selectively traces samples independently of these other commands.

5.8.1.6 **End Level**

The end level value is usually set to F, but can be set to any value 0 through F. When the trace control logic advances out of the specified end level, the trace control process stops. A jump from the specified end level, however, will execute normally and will not cause the recording process to stop. This can be used as a means of specifying an alternate stop condition on a level or as a debugging tool for your trace control program. By moving the end level value up and repeating the record cycle, you can move through your trace control program, stopping after the advance from each level and viewing the results.

5.8.2 GENERAL APPROACH TO TRACE CONTROL

The general approach in specifying a sequence of trace control menus is to use ADVANCE to progress along the expected course of events and JUMP to follow possible sidelines.

Leave room for new insertions so that you do not have to make awkward jumps merely to get around a screen level you have already used. For example, you might reserve levels 0 through 8 for the main line, even though you have defined only five main-line levels. Then jump out to levels 9, 11, and so on for exceptions, allowing two screens for each even if you think only one is needed. This approach leaves room for expansion. If you have to insert a new screen between others, you don't have to respecify all the later screens.

Be careful with ALWAYS and NEVER; TRACE NEVER means just that.

Work up to complex logic. Try simpler approaches, verify that they work, and gradually increase your complexity. Build on solid steps of progress. The end level specification, explained above, can be very useful in developing a sequence of trace control screens.

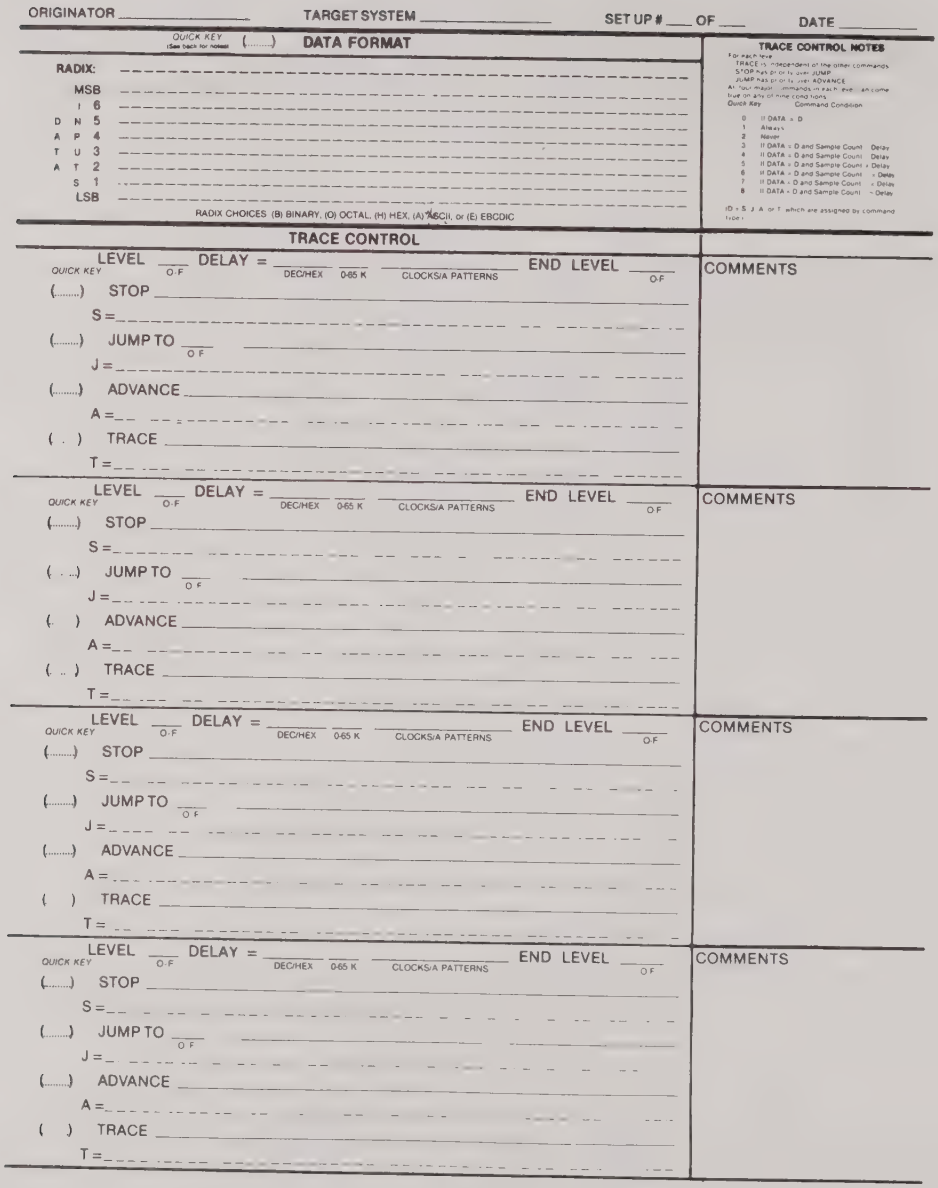
Section 8 (Applications) has many examples of trace control screens that show how the different elements of trace control work together.

A form for specifying trace control is available from Gould (see Figure 5-28). Note that it has a table showing the QUICK key values for the nine condition choices available for STOP, JUMP, ADVANCE and TRACE.

5.9 **INTERFACE**

The Interface menu is the only Specify menu not discussed in this section. It refers to specification of the communication process and is discussed in Section 9 (Communications).

There is one point about communications that does relate to specifying recording parameters: these recording parameters can be specified remotely. The settings discussed in this section can be coded and sent to a remote K101-D.



ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

QUICK KEY (.....) **DATA FORMAT**

RADIX: _____

MSB _____
I 6 _____
D N 5 _____
A P 4 _____
T U 3 _____
A T 2 _____
S 1 _____
LSB _____

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level become true on any of nine conditions

Quick Key	Command Condition	
0	If DATA = D	
1	Always	
2	Never	
3	If DATA = D and Sample Count	Delay
4	If DATA = D and Sample Count	Delay
5	If DATA = D and Sample Count	> Delay
6	If DATA = D and Sample Count	= Delay
7	If DATA = D and Sample Count	< Delay
8	If DATA = D and Sample Count	~ Delay

ID = S, J, A, or T which are assigned by command type

TRACE CONTROL

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

(.....) STOP _____
S = _____
(.....) JUMP TO ___ (O-F) _____
J = _____
(.....) ADVANCE _____
A = _____
(.) TRACE _____
T = _____

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

(.....) STOP _____
S = _____
(. ..) JUMP TO ___ (O-F) _____
J = _____
( ) ADVANCE _____
A = _____
(..) TRACE _____
T = _____

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

(.....) STOP _____
S = _____
(.....) JUMP TO ___ (O-F) _____
J = _____
(.....) ADVANCE _____
A = _____
( ) TRACE _____
T = _____

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

(.....) STOP _____
S = _____
(.....) JUMP TO ___ (O-F) _____
J = _____
(.....) ADVANCE _____
A = _____
( ) TRACE _____
T = _____

Note: This is the front side of Form DWG. 24. The other side contains all supporting specifications.

Figure 5-28. Trace Control Form.

Section 6

MAKING A RECORDING

6.1 OVERVIEW AND STRATEGY

The recording process can take place any time simply by pressing the **ARM** key. For meaningful recordings, however, the desired inputs should have already been connected and the input and trace conditions specified. When these tasks have been completed, your next step is to decide how you want the recording(s) to be made.

This section explains how to specify and control the recording process from the front panel. There are several possible approaches to controlling the recording process. At one extreme, you can sit and monitor the process, and even intervene manually. At the other extreme, you can set up the system for automatic operation and let it run for several days.

6.1.1 ARMING SPECIFICATIONS

Arming specifications are set using the Input Mode screen. For convenience, the choices are shown again:

Manual
Auto
Auto stop if A=B
Auto stop if A≠B
Auto stop if A=B within limits
Auto stop if A≠B within limits

6.1.2 MANUAL CONTROL

You control the recording process with four keys in the ACQUIRE section of the control panel. These keys are red, and they have the following functions:

a. **ARM:** Starts the recording process

b. **ADVANCE:** Can be used to force an advance to the next level of tracing

c. **M->A:** Stops the recording process and moves the recorded information to display memory A

d. **STOP:** Stops the recording process but does not move the recorded information to the display memory

The recording process ends either (a) automatically when the specified conditions and the conditions of the arm mode are met, or (b) the user stops the process. Different stop conditions can be specified for each level using the trace control stop commands (see paragraph 5.8.1.2) or the end level option (see paragraph 5.8.1.6). Depending on the arm mode and its conditions, the end of a recording cycle may end the recording process or a new recording cycle may be initiated. Arm modes and their conditions are discussed below. Even when an automatic mode is used, manual control is still provided: you can stop a recording in process at any time by pressing either the **M->A** key or the **STOP** key.

6.1.3 MONITORING THE RECORDING PROCESS

While the analyzer is actually tracing and recording, you can monitor progress by watching the status and level messages displayed in the lower right corner of the CRT screen. These messages are shown on every menu and data screen in the same location. Assuming a clock is present,

the current trace control level number shows, along with a status of busy or ready. Busy means that the trace logic is attempting to complete the conditions specified for that trace level. Ready means that the conditions are satisfied and the user can view the results.

6.2 **ARMING CHOICES**

Pressing the **ARM** key starts the sampling process that leads to the acquisition of the desired information on the behavior of the target system. Control of this recording process is preset by the selection of an arming mode. Although there are six possible specifications, they can be thought of as three basic arm modes: Manual, Auto, and Auto Stop by Compare. The modes differ, essentially, in what conditions may be specified to stop the recording process.

An explanation of the arm modes is given below. "Recording cycle" means the entire cycle of sampling data and acquiring those data which meet trace specifications. A recording cycle ends when the trace logic reaches a stop condition or an end level.

6.2.1 MANUAL ARM MODE

Manual arm mode initiates only one recording cycle and stops at the end of that acquisition. (The other arm modes may repeat recording cycles.) If the recording conditions are not met as expected, you can end the recording cycle by pressing **M->A** or **STOP**.

Use: This mode is used for gaining insight on problems involving general system characterization, checkout, and debugging.

6.2.2 AUTO ARM MODE

The Auto arm mode automatically re-arms the K101-D after the first recording cycle has been completed, and continues indefinitely to re-arm

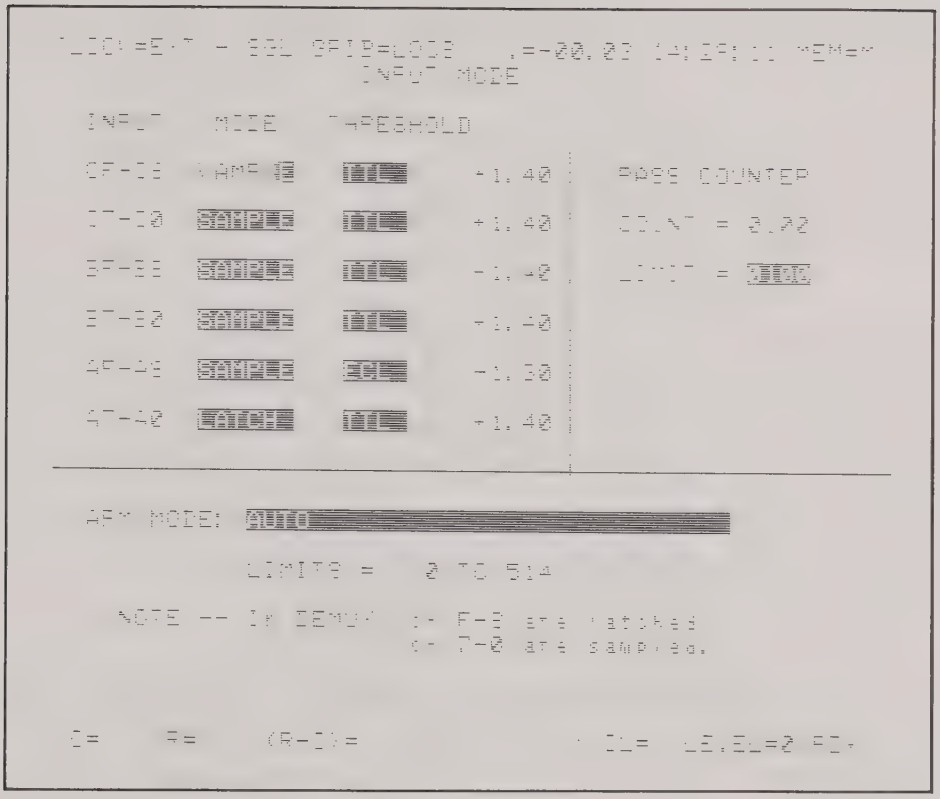
and record after each completed cycle. The same trace parameters are used for every recording cycle. Each re-arm sets the trace memory M to all zeros and the associated trace level tracking bits all to F. The first valid master clock pulse that is sensed by the trace control logic causes an unconditional advance to level 0 where the recording process begins.

After each cycle is completed, the Data, Graph, and Timing displays are automatically updated to show the new information acquired. Auto arm mode allows you to select the desired display and observe changes in system behavior as each new recording is completed.

Auto arm mode has a pass counter available, which can be used to redefine a specific limit to the number of recording passes the analyzer is to complete before stopping. The **M->A** and **STOP** keys can also be used. The pass counter is set by accessing the pass counter limit field (see Figure 6-1) on the upper right side of the Input Mode screen. The pass count limit can be set to any value from 0 (not used) to 9,999.

Pressing the **ARM** key resets the pass count to zero and begins a fresh recording process with a new count, even if the unit is already armed. When the instrument reaches the specified number of completed acquisitions, recording stops automatically.

Use: Auto arm mode allows you to monitor selected displays (Data, Graph, or Timing) to observe specific changes in system behavior as each recording cycle is completed. This mode can also be used to set the analyzer up to look for an error indefinitely (up to the pass counter limit). If an error occurs, the recording process may hand in a trace level waiting for an expected event that has not been sampled. Every time you enter the Input Mode screen, a count field above the pass counter entry field shows the number of acquisition cycles completed. This figure is updated when you enter the Input Mode screen, but is not maintained dynamically or transferred to memory A when a recording is completed.



Note: The pass counter is on the upper right of the screen.

Figure 6-1. Input Mode Screen.

The count is retained on the memory M Input Mode screen until the next arm cycle is initiated.

6.2.3 AUTO STOP BY COMPARE ARM MODE

There are four possible Auto Stop specifications:

a. Auto stop if A=B
b. Auto stop if A≠B
c. Auto stop if A=B within limits
d. Auto stop if A≠B within limits

Auto Stop arm mode is similar to Auto arm mode. The additional specifications are provided to extend your control over the conditions that automatically stop the instrument's recording cycle. All four specifications compare the contents of memories A and B. The first two specifications compare the complete memories, checking either for equal or not equal; the second two specifications compare only a specified portion of the memories for equal or not equal.

Other stop conditions are the same as those for Auto arm mode, including the pass count and the manual stop keys. Pressing the **ARM** key resets the pass count to zero and begins a new count, even if the unit is already armed.

Use: Auto Stop mode is also called "baby sitting" mode, because the logic analyzer can be left without an operator for long periods of time to monitor the system under test. This allows looking for a particular set of conditions or for intermittent faults. Because the time of day is stored with a recording, the time of day at which the results of interest occur can be captured and stored.

When used with the pass counter, Auto Stop can also be used to verify or ensure that your target system is operating properly as opposed to

searching for intermittent faults. Although certainly not a quantitatively exhaustive approach, this application is based on the rather simple assumption that if your system is able to repeatedly perform the activities required to complete each pass, then that aspect of the system is probably functioning properly. The validity of this assumption depends primarily on your ability to define the basic recording parameters. A side benefit is that if a problem does show up, chances are also good that you have automatically captured the clues necessary for quickly isolating and eliminating the problem.

Note

If the analyzer hangs up between levels rather than reaching a specified stop, it is still quite possible that the critical symptoms were captured. Memory A will contain the last successfully recorded pass and memory M will contain the partial recording leading up to the problem. If you notice the recording has hung up and want to maximize the information available to find out why, press **A->B** to save the last recording, then **M->A** to transfer the partial recording.

The reference memory used for Auto Stop comparisons can be loaded in three basic ways: via the Edit mode, from communications port, or by direct transfer from memory A to B. The edit functions can be used to provide an idealized reference memory for comparison. Details on the four specifications for this mode follow.

6.2.3.1 **Auto Stop by Full Compare**

Either "A equal to B" or "A not equal to B" can be specified as the stop condition. When the last recording made compares to the reference

memory B contents in the specified manner, the recording cycle stops and that recording is held in display memory A for review. Otherwise, recording continues just as in Auto mode. The pass counter, **M->A** key, and **STOP** key function as with Auto mode to stop the recording process.

6.2.3.2 **Auto Stop Compare Within Limits**

Auto Stop within limits lets you choose only a portion of the recording for the Auto Stop comparison, rather than the whole memory. In all other respects, Auto Stop within limits functions the same as the Auto Stop with full compare, including the use of the pass counter, **M->A** key, and **STOP** key as alternate methods to stop a recording cycle.

Use: If even a portion of the recording is expected to remain stable for each new acquisition, you can use the Auto Stop feature to check that stable portion. When this arm mode is used, you can limit data comparison in two ways. First, only the inputs currently displayed from memory A, which were selected using the data format field, are considered. Second, the Control Cursor and Reference Cursor can be used to limit a portion of the display. Only data from the Control Cursor location through the Reference Cursor location are considered. (If, however, the Reference Cursor is in front of the Control Cursor, the entire contents of both memories are considered over all currently displayed inputs, as though the Control Cursor were located at 0 and the Reference Cursor at SAM).

6.3 **MANUAL CONTROL**

6.3.1 ADVANCE

The **ADVANCE** key can be used to force the trace logic to advance to the next level of tracing.

Use: There are several situations in which the **ADVANCE** key is useful. For example, in setting the trace logic, the user may have assumed that level 2 would quickly result in conditions to be traced at level 3. Instead, the display continues to show that level 2 is busy. By forcing the trace logic to advance to level 3, the user can attempt to investigate whether the level 3 conditions have been reached some other way and are now active.

To give another example, the user might set up two or three independent trace specifications, each requiring unexpected activity for level exit to occur, and move manually through these specifications to check for the nonoccurrence of various events in the system.

6.3.2 MANUAL STOPS

There are two ways to manually stop the recording process: press either the **M->A** key or the **STOP** key. The **M->A** moves the recorded information to the display memory, whereas the **STOP** key does not.

Use: The difference is useful, even though you need to have the information in display memory in order to analyze it. You might choose **STOP** in order to examine prior display information or to ensure saving that information in reference memory before replacing it with a new recording.

STOP may also be the better choice if for some reason the recording process is botched. In such a case, there is no reason to continue to gather or display meaningless data.

Section 7

RECORDING ANALYSIS

7.1 OVERVIEW AND STRATEGY

The goal of recording analysis is to determine if one has solved a problem, or at least to reveal the steps necessary to obtain a solution. Depending on the results of your analysis, you may stop immediately or return to a prior step and try again, perhaps with changed specifications based on the insights gained through the review of captured information.

The analytic tools explained in this section represent a powerful problem solving capability and provide the best means to reach the aforementioned goal. With these tools -- Data, Graph, and Timing displays -- you can review, search, and compare recorded information in both memories A and B.

This section discusses how to examine the results of the recording process set up using the techniques explained in Sections 5 and 6. It explains how to use the choices available for the DISPLAY keys, EDIT keys, and other ways to review recordings. (See Section 3 for detailed reference material on these keys and Section 4 for information on how to use them.) The emphasis here is the rationale behind making particular choices.

Here are some of the topics addressed in this section:

a. The Data, Graph, and Timing displays

b. The use of the SEARCH and COMPARE functions and of the Control Cursor and Reference Cursor

c. How and why to edit reference memory B

Keep in mind that the Data, Graph, and Timing displays are alternate presentations of the same information, as shown in Figures 7-1, 7-2, and 7-3, respectively.

The Data display allows you to see every record captured. It uses the format specified by the Data Format screen.

The Graph display allows you to see an overview of the sequence of captured events. The emphasis is on comparison of events over time rather than the details of events occurring at each sample.

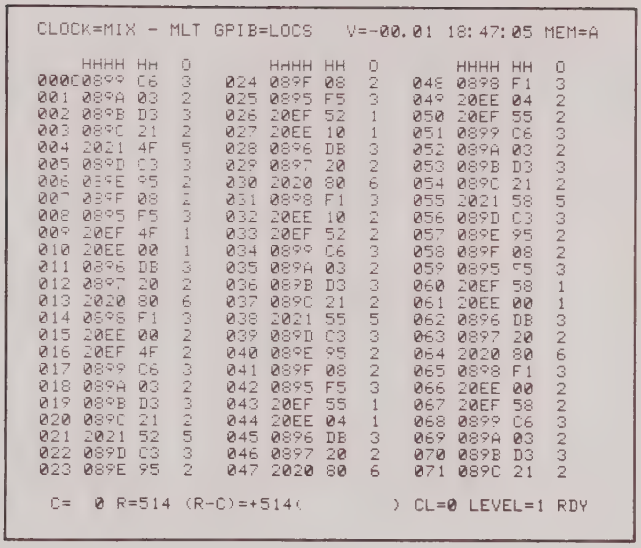
The Timing display allows you to see the timing relationships among events. This display shows the rise and fall over time of each sample input relative to its selected threshold level.

7.2 **OVERVIEW OF KEYS**

For convenience, here is a brief review of the keys used in recording analysis. They are discussed in detail in Section 4 (User Controls and Displays). The keys are the DISPLAY keys, the EDIT keys from the GENERAL key area, hexadecimal keys and ASCII keys, several direct keys used for manipulating the displays, and the FIELD keys for manipulating the Control and Reference Cursors.

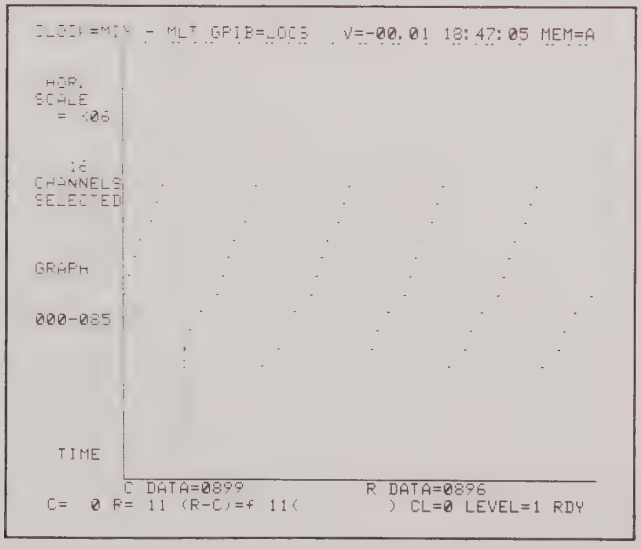
7.2.1 DISPLAY KEYS

The **DATA**, **GRAPH**, and **TIMING** keys are used to bring up the appropriate display. The **A** and **B** keys select the current memory, which is the memory to be displayed or searched. The **SEARCH** key is a toggle which sets the SEARCH function on or off; it is used to search the current memory for the presence of specific bit combinations or patterns. This search pattern is set from the Data Format screen, called from the SPECIFY area of the keyboard. **COMPARE** is also a toggle; it turns the



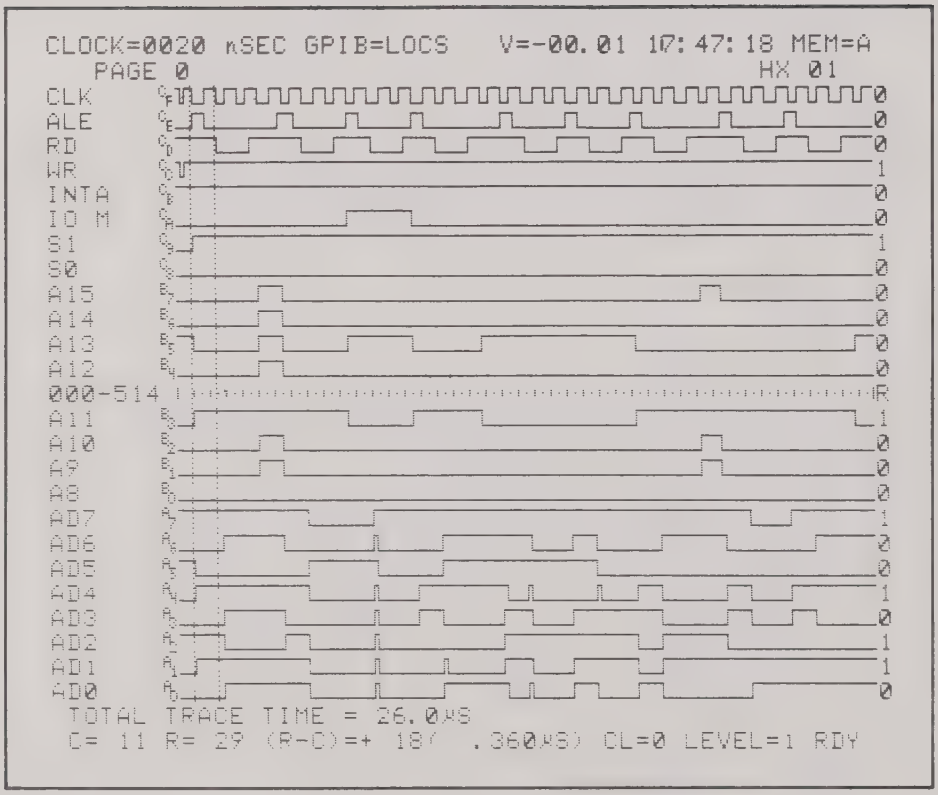
Note: The data shown are in the format specified by the current Data Format display. The display shows the exact events as captured.

Figure 7-1. Data Display.



Note: The same data as in Figure 7-1, shown graphically.

Figure 7-2. Graph Display.



Note: Some of the input signals from Figure 7-1 shown over time.

Figure 7-3. Timing Display.

COMPARE function on or off, and compares all samples present in memories A and B. Finally, **A->B** transfers the contents of memory A to memory B.

7.2.2 THE EDIT KEYS

Three blue (action) keys in the GENERAL key area control the EDIT function. **EDIT** turns on Edit mode, **INSERT** inserts a blank line in the Data display, and **DELETE** deletes a line. When in Edit mode, you can use hexadecimal keys to change or insert data in the Data display. Also in this mode, you can insert labels in the Timing display, using the ASCII keys.

7.2.3 DISPLAY MANIPULATION

The Timing display can be expanded using the vertical or horizontal expansion keys (**V6** or **H x 3**, for example) and can be scrolled using **PAGE UP** and **PAGE DOWN**. The Graph display can be expanded using the horizontal expansion keys and **EDIT** key.

7.2.4 CURSOR KEYS

The FIELD keys for moving the Control Cursor (labelled CURSOR) and the Reference Cursor (labelled REFERENCE) are used in reviewing all three displays. In the Data display, the cursors move vertically, and in the Graph and Timing displays, horizontally.

7.3 DISPLAY FORMATS

There are three display formats: Data, Graph, and Timing. Data is the basic display; the other two are derived from it. These displays show the current memory, which may be A or B memory according to whether the **A** or **B** key was last pressed. **A** or **B** can be pressed before pressing **DATA**, **GRAPH**, or **TIMING**, or while displaying one of those three formats.

The current memory is shown in the upper right of the display, as "Mem=A" or "Mem=B."

7.4 **DATA DISPLAY**

This is also called a "state display," because it shows the exact state of the captured events. The information is in the format set by the current Data Format specification (from the SPECIFY area). The format can be changed; this would be reflected in a change of the display. Input signals that are not formatted are not displayed; however, all input signals that are eligible at trace time are captured, and they can be displayed if the format is changed to show them.

The conditions used at the time of capture are also preserved, and changes in the conditions of capture, such as changes in threshold or polarity, do not change a prior display.

PAGE UP and **PAGE DOWN** can be used to move through the Data display. The Control Cursor and Reference Cursor also move through the display. Their locations are shown by "C" and "R" at the left of the data.

7.4.1 DATA SEARCHES

The **SEARCH ON/OFF** key is an alternate action or toggle key which turns SEARCH on or off. It refers to the current memory. The search pattern is entered by using the lower half of the Data Format menu.

There are two modes for specifying the search word (see Figure 7-4).

a. By bytes: enter data in the same format that you specify in the upper half of this menu.

b. By bits: enter (in the MSB/LSB field) 1, 0, or "Don't Care" bits. This gives you the ability to specify a hex byte, for

example, and then specify a range of hex words by setting to "Don't Care" one or more of the bits of the hex byte.

The bottom of the Data display shows the search results, including the total number of cases matching the pattern and the first and last locations. In Figure 7-5, the tally at screen bottom shows two occurrences of the search word, at memory locations 139 and 395. An asterisk on the Data display entry shows the matching locations. The **NEXT** key allows you to sequence through memory from one matching event location to the next.

7.4.2 MEMORY COMPARISON

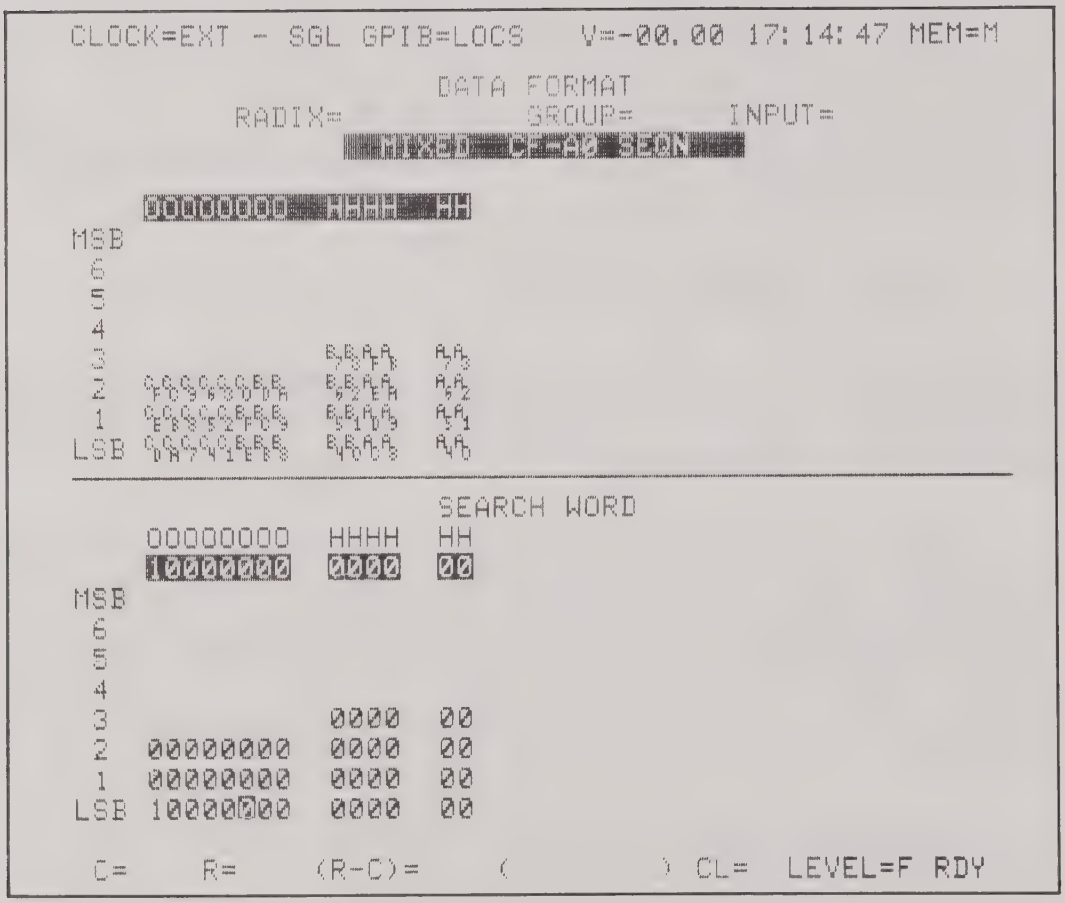
You can compare the contents of A and B memories. The DISPLAY key **COMPARE A/B** is an alternate action or toggle key; it turns the COMPARE feature on and off (see Figure 7-6).

By using Data display for A or B, you can visually determine the exact differences between the two memories. The instrument finds and tallies the unmatched locations. An unequal sign (≠) denotes those locations in memory A that are not equal to the corresponding locations in memory B. The **NEXT** key allows you to sequence through the memory locations that do not match.

7.4.3 REFERENCE EDITING

If the data format is not a fixed format, you can edit or enter data in memory B (see Figure 7-7 for an example).

When you press the **EDIT** key, a cursor appears at the top of the left hand column of data. Position the cursor to the desired memory location, using the UP/DOWN arrow keys in FIELD area.



Note: At the lower half of screen, search is ON. Line of hex, ASCII, octal, and binary allows byte level selection of the search word. Column MSB/LSB allows bit level selection.

Figure 7-4. Data Searches.

```
CLOCK=0020 nSEC GPIB=LOCS    V=-00.00 00000000 MEM=B
    OOCCOOOI  HHHH  H-          I  OOOOOOO  ==HH  =H
130C40501202  8282  8C      5~ 4E:1'282  =A8A  =A
131 40701603  8383  83     155 46715633  =B9B  =B
132 41102204  8484  84     156 47116234  9C9C  =C
133 41302605  8585  85     157 47316635  9D9D  =D
134 41503206  8686  86     158 47517236  9E9E  =E
135 41703607  8787  87     159 47717637  9F9F  =F
136 42104210  8888  88     160 50120240  A0A0  A0
137 42304611  8989  89     161 50320641  A1A1  A1
138 42505212  8A8A  8A     162 50521242  A2A2  A2
139*10000000  0000  00     163 50721643  A3A3  A3
140 43106214  8C8C  8C     164 51122244  A4A4  A4
141 43306615  8D8D  8D     165 51322645  A5A5  A5
142 43507216  8E8E  8E     166 51523246  A6A6  A6
143 43707617  8F8F  8F     167 51723647  A7A7  A7
144 44110220  9090  90     168 52124250  A8A8  A8
145 44310621  9191  91     169 52324651  A9A9  A9
146 44511222  9292  92     170 52525252  AAAA  AA
147 44711623  9393  93     171 52725653  ABAB  AB
148 45112224  9494  94     172 53126254  ACAC  AC
149 45312625  9595  95     173 53326655  ADAD  AD
150 45513226  9696  96     174 53527256  AEAE  AE
151 45713627  9797  97     175 53727657  AFAF  AF
152 46114230  9898  98     176 54130260  B0B0  B0
153 46314631  9999  99     177 54330661  B1B1  B1
    TOTAL * =  2    FIRST * =139    LAST * =395
 C=130 R=514 (R-C)=+384(  7.68MS) CL=F LEVEL=F RDY
```

Note: Data entry at the bottom of the screen shows that there were two words, at locations 139 and 395.

Figure 7-5. Search Tabulation.

```
CLOCK=0020 nSEC GPIB=LOCS    V=-00.00 00000000 MEM=B

    OOOOOOOO  HHHH  HH        OOOOOOOO  HHHH  HH
085C25252525  5555  55    109 33266555  6D6D  6D
086 25453126  5656  56    110 33467156  6E6E  6E
087 25653527  5757  57    111 33667557  6F6F  6F
088 26054130  5858  58    112 34070160  7070  70
089 26254531  5959  59    113 34270561  7171  71
090 26455132  5A5A  5A    114 34471162  7272  72
091 26655533  5B5B  5B    115 34671563  7373  73
092 27056134  5C5C  5C    116 35072164  7474  74
093 27256535  5D5D  5D    117 35272565  7575  75
094 27457136  5E5E  5E    118 35473166  7676  76
095 27657537  5F5F  5F    119 35673567  7777  77
096 30060140  6060  60    120 36074170  7878  78
097≠55555541  6161  61    121 36274571  7979  79
098 30461142  6262  62    122 36475172  7A7A  7A
099 30661543  6363  63    123 36675573  7B7B  7B
100 31062144  6464  64    124 37076174  7C7C  7C
101 31262545  6565  65    125 37276575  7D7D  7D
102 31463146  6666  66    126 37477176  7E7E  7E
103 31663547  6767  67    127 37677577  7F7F  7F
104 32064150  6868  68    128 40100200  8080  80
105 32264551  6969  69    129 40300601  8181  81
106 32465152  6A6A  6A    130 40501202  8282  82
107 32665553  6B6B  6B    131 40701603  8383  83
108 33066154  6C6C  6C    132 41102204  8484  84
    TOTAL ≠ =  2    FIRST ≠ = 97    LAST ≠ =353
 C= 85 R=200 (R-C)=+115(  2.30MS) CL=F LEVEL=F RDY
```

Note: Data entry shows two nonmatches, at locations 22 and 49. The **NEXT** key shifts to subsequent qualifying locations.

Figure 7-6. Memory Comparison.

```
CLOCK=0020 nSEC GPIB=LOCS    V=-00.00 00000000 MEM=B
     OOOOOOOO  HHHH  HH          OOOOOOOO  HHHH  HH
105C32264551  6969  69     129 40300601  8181  81
106 32465152  6A6A  6A     130 40501202  8282  82
107 32665553  6B6B  6B     131 40701603  8383  83
108 33066154  6C6C  6C     132 41102204  8484  84
109 33266555  6D6D  6D     133 41302605  8585  85
110 33467156  6E6E  6E     134 41503206  8686  86
111 33667557  6F6F  6F     135 41703607  8787  87
112 34070160  7070  70     136 42104210  8888  88
113 34270561  7171  71     137 42304611  8989  89
114 34471162  7272  72     138 42505212  8A8A  8A
115 34671563  7373  73     139 42705613  8B8B  8B
116 35072164  7474  74     140 43106214  8C8C  8C
117 35272565  7575  75     141 43306615  8D8D  8D
118 35473166  7676  76     142 43507216  8E8E  8E
119 35673567  7777  77     143 43707617  8F8F  8F
120 36074170  7878  78     144 44110220  9090  90
121 36274571  7979  79     145 44310621  9191  91
122 36475172  7A7A  7A     146 44511222  9292  92
123 36675573  7B7B  7B     147 44711623  9393  93
124 37076174  7C7C  7C     148 45112224  9494  94
125 37276575  7D7D  7D     149 45312625  9595  95
126 37477176  7E7E  7E     150 45513226  9696  96
127 37677577  7F7F  7F     151 45713627  9797  97
128 40100200  8080  80     152 46114230  9898  98
    TOTAL ≠ =  2    FIRST ≠ = 97    LAST ≠ =353
 C=105 R=200 (R-C)=+ 95(  1.90uS) CL=F LEVEL=F RDY
```

Note: The cursor is at location 105. You can write over the existing data using the hexadecimal keys.

Figure 7-7. Reference Editing.

To alter individual entries, use the LEFT/RIGHT arrow keys to position the cursor at the character to be changed. Using the keyboard, write over the existing entry. You can use any appropriate hexadecimal characters.

The **INSERT** and **DELETE** keys allow you to insert or delete memory entries when in Edit mode.

In Figure 7-8, the edit cursor is placed at memory location 105 and the data stored is 6969. Pressing **INSERT** clears the line to all zeros. This action also shifts all subsequent memory contents down one line. The last word in memory is lost.

To delete an entry, place the edit cursor at the desired line and press the **DELETE** key. The data at that memory location disappear and are replaced with the data from the line below. All data in memory get shifted up, and the last memory location is loaded with zeros (see Figure 7-9).

7.5 GRAPH DISPLAY

This display shows events plotted over time. It is useful for a quick comparison among events. Only the first 14 characters of the Data display are plotted. Depending on the data format specified, there may be data beyond the range of the display; if so, they are ignored.

By editing or respecifying the data format, it is possible to display some other data or the same data in a different order.

The Graph display provides an X-Y coordinate graph of the magnitude of the data value in memory vs. the memory location. Because the memory contents are sequential in time, the graph shows events over time. However, the events may have been captured at greatly varying intervals, so the time component is arbitrary.

```
CLOCK=0020 nSEC GPIB=LOCS    V=-00.00 00000000 MEM=B
    00000000  HHHH  HH          00000000  HHHH  HH
105C 0000000  0000  00    129 40100200  8080  80
106 32264551  6969  69    130 40300601  8181  81
107 32465152  6A6A  6A    131 40501202  8282  82
108 32665553  6B6B  6B    132 40701603  8383  83
109 33066154  6C6C  6C    133 41102204  8484  84
110 33266555  6D6D  6D    134 41302605  8585  85
111 33467156  6E6E  6E    135 41503206  8686  86
112 33667557  6F6F  6F    136 41703607  8787  87
113 34070160  7070  70    137 42104210  8888  88
114 34270561  7171  71    138 42304611  8989  89
115 34471162  7272  72    139 42505212  8A8A  8A
116 34671563  7373  73    140 42705613  8B8B  8B
117 35072164  7474  74    141 43106214  8C8C  8C
118 35272565  7575  75    142 43306615  8D8D  8D
119 35473166  7676  76    143 43507216  8E8E  8E
120 35673567  7777  77    144 43707617  8F8F  8F
121 36074170  7878  78    145 44110220  9090  90
122 36274571  7979  79    146 44310621  9191  91
123 36475172  7A7A  7A    147 44511222  9292  92
124 36675573  7B7B  7B    148 44711623  9393  93
125 37076174  7C7C  7C    149 45112224  9494  94
126 37276575  7D7D  7D    150 45312625  9595  95
127 37477176  7E7E  7E    151 45513226  9696  96
128 37677577  7F7F  7F    152 45713627  9797  97
   TOTAL ≠ =  2     FIRST ≠ = 97     LAST ≠ =353
 C=105 R=200 (R-C)=+ 95(  1.90µS) CL=F LEVEL=F RDY
```

Note: The edit cursor is at location 105. Press **INSERT** to fill location 105 with all zeros. Locations 105 through 515 move down one location. Enter new data at 105.

Figure 7-8. Insert.

```
CLOCK=0020 nSEC GPIB=LOCS    V=-00.00 00000000 MEM=B

    00000000  HHHH  HH          00000000  HHHH  HH
105C 2665553  6B6B  6B    129 40701603  8383  83
106 33066154  6C6C  6C    130 41102204  8484  84
107 33266555  6D6D  6D    131 41302605  8585  85
108 33467156  6E6E  6E    132 41503206  8686  86
109 33667557  6F6F  6F    133 41703607  8787  87
110 34070160  7070  70    134 42104210  8888  88
111 34270561  7171  71    135 42304611  8989  89
112 34471162  7272  72    136 42505212  8A8A  8A
113 34671563  7373  73    137 42705613  8B8B  8B
114 35072164  7474  74    138 43106214  8C8C  8C
115 35272565  7575  75    139 43306615  8D8D  8D
116 35473166  7676  76    140 43507216  8E8E  8E
117 35673567  7777  77    141 43707617  8F8F  8F
118 36074170  7878  78    142 44110220  9090  90
119 36274571  7979  79    143 44310621  9191  91
120 36475172  7A7A  7A    144 44511222  9292  92
121 36675573  7B7B  7B    145 44711623  9393  93
122 37076174  7C7C  7C    146 45112224  9494  94
123 37276575  7D7D  7D    147 45312625  9595  95
124 37477176  7E7E  7E    148 45513226  9696  96
125 37677577  7F7F  7F    149 45713627  9797  97
126 40100200  8080  80    150 46114230  9898  98
127 40300601  8181  81    151 46314631  9999  99
128 40501202  8282  82    152 46515232  9A9A  9A
   TOTAL ≠ =  2     FIRST ≠ = 97     LAST ≠ =353
 C=105 R=200 (R-C)=+ 95(  1.90µS) CL=F LEVEL=F RDY
```

Note: The new data are at location 105. To delete, move the edit cursor to 105 and press the **DELETE** key. Locations 106 through 515 move up one location.

Figure 7-9. Delete.

The Graph display is useful for determining if repeated occurrences of a particular data word occurred or if the data in memory are all within a particular range.

7.5.1 SELECTING VERTICAL DISPLAY LIMITS

The upper and lower limits of the Y axis are data values that can be specified by the user. When Graph mode is first entered, the plotted data span all 48 channels in the range from 0000 0000 0000 to FFFF FFFF FFFF. To change the limits, press the **EDIT** key. Note the EDIT UPPER and LOWER fields which appear just beneath the X axis. The upper and lower limits of the Y axis can now be specified using the hexadecimal keys. Pressing the **EDIT** key again exits Edit mode and replaces the upper and lower limit data with the display of Control and Reference Cursor data.

Note

In Figure 7-2, the C and R displays show the actual contents from the Data display at the locations in memory where the Control Cursor and Reference Cursor are positioned at that moment. The cursors show as vertical lines on the display.

7.5.2 HORIZONTAL DISPLAY EXPANSION

You can expand the display horizontally by factors of 3, 6, and 12 by using the **H x 3**, **H x 6**, and **H x 12** keys, respectively. The display is expanded from the Control Cursor position. The Control Cursor always appears on the left axis. Moving the Control Cursor scrolls the display to the left and right when in expanded modes. The Reference Cursor may or may not appear, depending on conditions.

The left margin of the graph displays the horizontal scale, the number of selected channels, and the memory locations. With a broader horizontal scale, fewer memory locations are shown.

7.6 **TIMING DISPLAY**

The Timing display shows events across all 48 input signals over time. They are displayed in order of specification. As with the Graph display, the time component is arbitrary because the events may have been captured at greatly varying intervals. Not all input signals can be shown at once, and therefore various means are provided to review the display.

7.6.1 VERTICAL DISPLAY EXPANSION AND PAGING

The unit can display as many as 24 input signals at a time. The **V24** key displays 24 input signals, the **V12** displays 12, and the **V6** displays 6. All 48 inputs may be viewed by paging up and down. **PAGE UP** pulls the Input displays up six at a time; **PAGE DOWN** pushes them down six at a time.

7.6.2 HORIZONTAL DISPLAY EXPANSION

You can expand the display horizontally by factors of 3, 6, and 12, by using the **H x 3**, **H x 6**, and **H x 12** keys, respectively. Expansion takes place to the right of the cursor position.

To use a cursor or reference key to specify a GO-TO MEMORY operation, press **SHIFT**, and the CURSOR **SET** (cursor left) key or the REFERENCE **SET** (reference left) key. Then enter the memory location number and press **TIMING**.

7.6.3 MODIFYING THE TIMING DISPLAY

In Edit mode, you can change the order of display or replace existing input signals with any other signal. The **EDIT** key turns on the cursor, which is then positioned at the input signal to be replaced by using the FIELD UP/DOWN arrow keys (see Figure 7-10).

Use the hex keys, **0** through **9** and **A** through **F**, to enter the desired input signal. Any input signal may be used as many times as desired.

7.6.4 LABELLING TIMING DISPLAYS

You can also label each Timing display when in Edit mode. The edit cursor may be moved into the open field to the left of the timing traces by using the LEFT/RIGHT arrow keys. This allows you to label each trace with up to seven alphanumeric characters (see Figure 7-11). You can use any ASCII character.

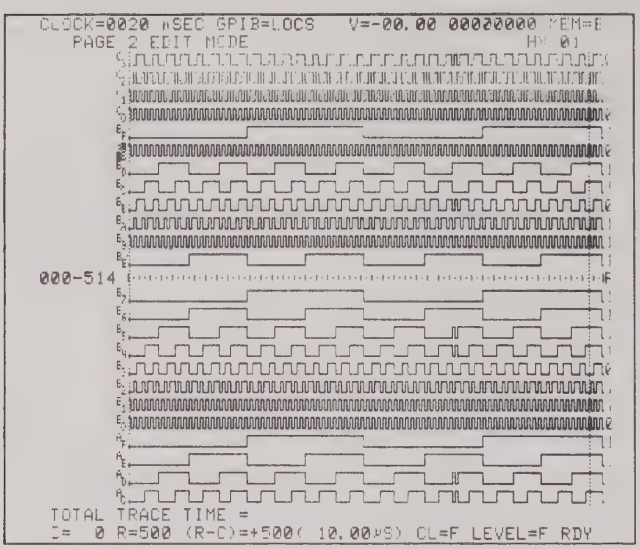
For **0** through **9** and **A** through **F** characters, use the hexadecimal keys directly. For letters **G** through **Z** (shown in yellow), press **SHIFT** for each character. To cancel a shift, press **SHIFT** second time.

7.7 **AUXILIARY MEASUREMENTS**

Five auxiliary measurements are discussed here: the digital voltmeter, the frequency counter, the date/time display, the total trace time display, and the trace level tracking displays (see Figure 7-12).

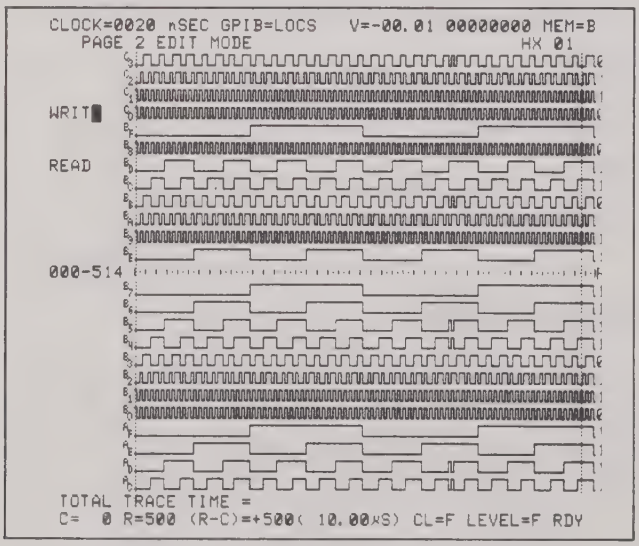
7.7.1 DVM (DIGITAL VOLTMETER)

The digital voltmeter readout appears on all display formats on the top right side of all screens (V = $\pm$00.00). The readout is real time, from any of the memory M screens, and shows the reading at the time each


CLOCK=0020 nSEC GPIB=LOCS V=-00.00 00000000 MEM=B
PAGE 2 EDIT MODE HX 01
000-514
TOTAL TRACE TIME =
C= 0 R=500 (R-C)=+500(10.00µS) CL=F LEVEL=F RDY

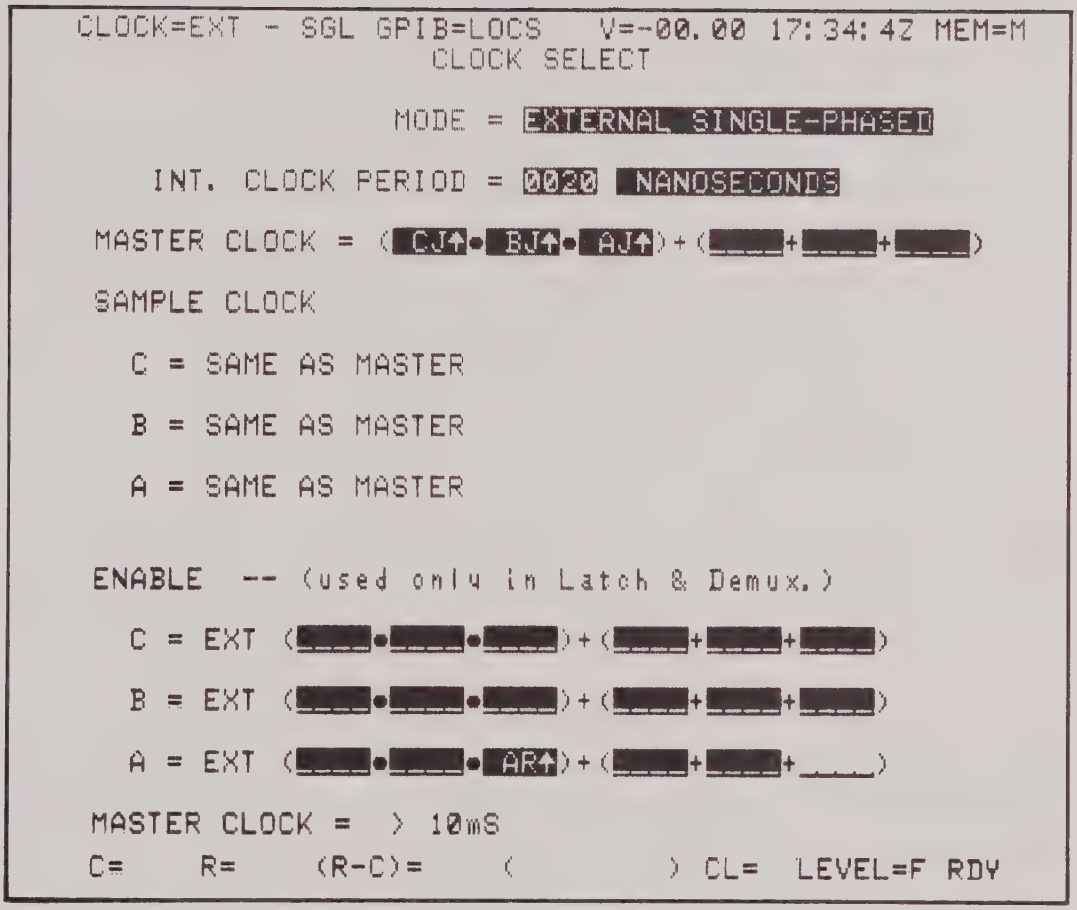
Note: The edit cursor is at position formerly occupied by input signal BE. Input signal B8 is now positioned there.

Figure 7-10. Trace Sequence Modification.



Note: The edit cursor was moved to the left of timing traces and a label was entered.

Figure 7-11. Trace Label Assignment.


CLOCK=EXT - SGL GPIB=LOCS V=-00.00 17:34:42 MEM=M
CLOCK SELECT
MODE = EXTERNAL SINGLE-PHASED
INT. CLOCK PERIOD = 0020 NANOSECONDS
MASTER CLOCK = (CJ↑• BJ↑• AJ↑)+(+ +)
SAMPLE CLOCK
C = SAME AS MASTER
B = SAME AS MASTER
A = SAME AS MASTER
ENABLE -- (used only in Latch & Demux.)
C = EXT (• •)+(+ +)
B = EXT (• •)+(+ +)
A = EXT (• • AR↑)+(+ +)
MASTER CLOCK = > 10mS
C= R= (R-C)= ( ) CL= LEVEL=F RDY

Note: DVM, TOD clock, frequency counter, and the trace level tracking are all shown. Press **CLOCK SELECT** to update the frequency counter display. Total trace time can only be viewed from the Timing display.

Figure 7-12. Auxiliary Measurements.

recording was completed when viewing the memory A or B screens. The DVM

recording was completed when viewing the memory A or B screens. The DVM measures voltages between ±20 VDC. Input impedance is 20 kilohms.

7.7.2 FREQUENCY COUNTER

This readout is a latched value. The counter measures the period of the master clock, and functions in any external clock mode. It is also a real time measurement and is updated when accessed. To access the current reading of the master clock, press **CLOCK SELECT**. The range of the of the frequency counter extends from 100 Hz to 50 MHz (10 msec to 20 nsec).

7.7.3 DATE AND TIME

This clock measures actual time of day. It is backed up by the internal battery when the K101-D is shut off. The date can be read from the interface screen while the time of day is shown on all memory M screens.

When necessary to reset the date or time, use the Interface menu. Position the cursor with the FIELD keys and enter the values with the numeric keys. The clock starts keeping time when you enter the second digit of the minutes field.

Month/day/year and time-of-day information are stored in a register at the end of, and saved with, the recording (similar to the DVM reading). Thus, when you examine or photograph the CRT you have a convenient record of the exact time the information was recorded, along with the system voltage level present at that time.

7.7.4 TOTAL TRACE TIME

The total time that the trace logic is enabled (TRACE ALWAYS is selected or TRACE IF DATA = T is true) for each recording is displayed on the bottom left side of the timing display. This feature allows you to

easily make a variety of precise timing measurements ranging from a simple measurement of the time between any two events to a complex measurement of non-seqential segments of program execution activity. For measuring the time between any two events, simply leave the trace turned off until the occurrence of the first event, turn trace on until occurrence of the second event, then turn it off again (or stop). For more complex measurements, you must define each interval (for example: subroutine entry and exit points, port write to peripheral response times, and memory access/refresh times) using Trace Control.

The STOP, JUMP, and ADVANCE commands can be used to follow program activity independent of whether or not samples are loaded into memory. The trace commands let you select all or only specific intervals along the specified execution path for loading into memory and accumulating total trace time. By altering the trace commands on each level you can accurately measure virtually any combination of time intervals that are of interest to your analysis, without altering the path being followed or your desired stop condition.

The minimum resolution of the total trace time counter is 0.5 microsecond. Automatic ranging allows display of times from 0.00 microsecond to 1638.35 seconds (27.3 minutes). The count resets to zero on all overflows (t>1638.35 seconds). To measure even longer time intervals, you can manually note the time of the arm event as shown on the Time of Day field, then compare it to the reading stored at the end of the recording. To measure less than 0.5 microsecond intervals, simply select the appropriate internal clock rate for recording with the desired resolution, then use the Control and Reference Cursors to find the time between any two events in memory.

7.7.5 TRACE LEVEL TRACKING

This feature allows you to review the current trace level of any recording in progress, the level where recording stopped, and the level

through which each sample entered memory. Each sample loaded into memory is tagged with four trace level tracking bits corresponding to the active trace control level (0-F) at the time the sample was loaded.

To determine the trace level associated with each sample, move the Control Cursor (C) to the desired sample location and read the cursor level display ("CL = n," n is 0 through F). This display field is located just to the left of the Trace Level field on the lower right side of all displays.

A short review of the recording process may be helpful in better understanding this feature. When each new recording cycle begins, trace memory M is loaded with zeros on all sample inputs and all ones on the trace level tracking bits (corresponding to level F). The first master clock pulse advances the trace logic to level 0. If the next sample meets the trace criterion as defined for level 0 then that sample is loaded in trace memory M at location 511 and tagged as being traced at level 0 by the sample's trace level tracking bits. If the next sample also meets the trace criteria, it too is tagged and loaded into location 511, and the preceding sample is shifted to 510. If the following sample does not meet the trace criteria then that sample is ignored and the preceding samples remain at locations 511 and 510 respectively. This process of sequencing selected samples through the trace memory continues until a desired stop condition is reached.

You can monitor the progress of a recording as it changes levels by observing the trace level shown on the bottom right corner of all displays as "Level = n" (n is 0 through F). Should a recording happen to remain longer than expected in a particular level, you can review the Trace Control commands specified for that level and decide whether to let the recording continue, to manually advance to the next level, to transfer the partial recording, or to totally cancel the recording.

Assuming a recording is completed, the level displayed will be the level where the stop condition came true. A special exception to this rule

exists when the stop occurs due to advancing out of the specified End level rather than meeting one of the specified Stop commands. In that case, the level shown will be the specified End level plus one. For example, if level 3 is specified as the end level, then an advance from level 3 will cause the recording to stop and the trace level will read "Level = 4 RDY," even though no samples were actually taken at level 4. This exception allows you to easily determine whether a stop occurred because the Stop command came true at that level, or because the Advance command came true meeting the specified End level condition.

If memory M is filled before a stop condition occurs, the first samples taken are sequenced past location 000 and then discarded as new samples are loaded into location 511. If the total number of samples taken into memory M during the recording process is less than the memory's length (512) then the unfilled portion is still displayed at the beginning of memory. These "false" samples are easy to recognize since they are all zero and tagged as entered by level F.

7.8 **USE OF THESE TECHNIQUES**

By examination of the results, you may determine the solution to a problem and validate the solution. Some of the ways the techniques described in this section can be used in conjunction with earlier techniques are mentioned below.

7.8.1 THE ITERATIVE APPROACH

As you work your way through successive recordings by modifying the conditional trace screens, you can disable tracing in the verified areas and increase your focus on the problem areas in order to maximize the capture of meaningful information. By using the results of each recording to more clearly define the problem's symptoms, you can quickly gain the insight needed for a solution.

7.8.2 USE OF SEARCH AND COMPARE

Some examples may indicate uses of these tools. Say that you suspect a problem relating to an interaction of three signals: MEMORY READ, MEMORY WRITE, and an INTERRUPT signal. There are eight state possibilities for these three lines. You can specify them as one octal or three binary characters and search for particular combinations, then see what is associated with each case.

You can edit the reference memory for particular cases and then compare. Using the SEARCH and COMPARE functions together, you can isolate very specific conditions. Alternately, using very broad searches (with many "Don't Care" specifications), you can examine both memories for general patterns or possible relationships, and then try various comparisons between the two.

7.8.3 USE OF AUTOMATIC ARM MODE

When you believe you have corrected the problem, you can set the K101-D to rerun in Automatic mode, looking for a repetition of the error. The area of comparison can be limited to the memory space between the Control Cursor and Reference Cursor and to the inputs currently selected on the data format.

7.9 SUMMARY

The above examples are not meant to be exhaustive but merely to provide a springboard for your own imagination. As stated in Section 5, use of the K101-D depends on knowledge of its capabilities and of the system under test. Fortunately, as you use the K101-D, you will gain knowledge about both.

The next section presents a number of applications. These are actual specific examples, in contrast to Sections 5, 6, and 7, which presented many broad possibilities. Examining these applications will further your grasp of the practical uses of the K101-D.

Section 8

APPLICATIONS

8.1 GENERAL

This section presents some building block approaches that can be used with the K101-D. Practical examples for clocking and trace control are presented. Examples of probe connection, polarity specification and threshold specification can be found in Section 10. Specification of input mode and clocking are somewhat interdependent and the clocking applications of paragraph 8.2 discuss both considerations. Similarly, the trace control section shows some practical applications of data format.

8.2 CLOCKING

The most efficient way to use the K101-D is to spend some time in pretest analysis and preparation before initiating any tests. You must decide (with regard to clocking) what type of analysis you want to perform: timing (asynchronous sampling), state (synchronous sampling), or a combination of both. An internal clock is used for asynchronous sampling, an external clock for synchronous sampling, and both for the combination of the two.

8.2.1 TIMING ANALYSIS

Timing analysis (asynchronous sampling) requires the use of an internal clock signal. The purpose of a timing analysis is to study the timing characteristics of your system to see how each signal functions in relation to the other signals. This is done by looking at all signals with the same K101-D internal sample clock.

When you initiate a timing analysis, you can make precise pulse width and skew measurements, look for errors and glitches, observe

characteristic timing relationships, and compare actual system performance to documented or desired specifications.

Skew measurements may be simple or complex. Simple skew is a measurement between one point on one input and one point on another input. Complex skew is between a point in time on a group of inputs and another point in time on another (or same) group of inputs (see Figure 8-1).

The recommended approach is to study the documentation associated with your system and its subsystems and choose the signals you think you need to observe to solve your system problem. Connect these signals to the sample inputs. The order of connection is not necessarily important. After recording, you can rearrange their order on screen to suit your viewing needs. The main considerations are resolution and sampling frequency, window size, and glitch capturing. These items are discussed below.

8.2.1.1 **Resolution and Sampling Frequency**

Resolution is the smallest time interval in which you can observe an event. With a resolution of X you can only determine whether or not an event occurred sometime during X.

Determine the degree of detail you need for your application. Study the system's timing characteristics to define the shortest time interval to be measured, then decide how accurately you need to measure that interval. (Alternately, determine the largest acceptable measurement error window or uncertainty.)

Once you have determined that you need to make measurements to a specific resolution then you can calculate the asynchronous sampling frequency needed. A resolution of X seconds means you must take at least two samples every X seconds (see Figure 8-2). Nyquists' sampling

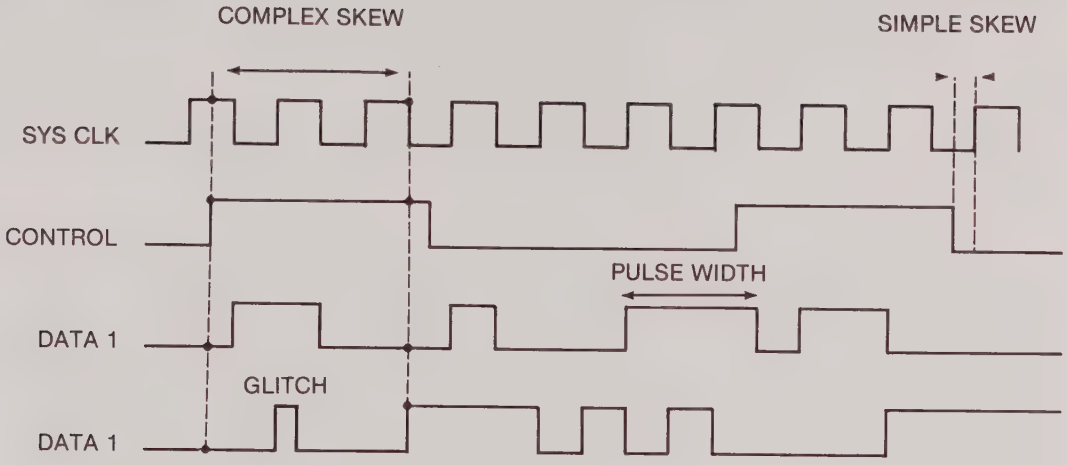
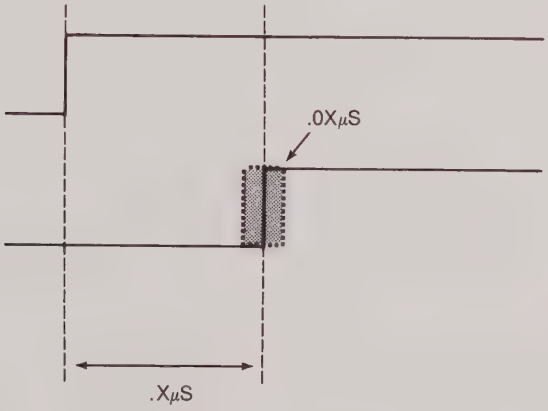


Figure 8-1. Typical Timing Analysis Measurements.



Note: The shortest time interval that needs to be measured is a skew of 0.X μS. If that interval is off by 10% (0.0X μS), however, it could cause a system error. Therefore a resolution of 0.0X μS or less is required. The second pulse can only be said to have risen sometime during a 0.0X μS interval. The skew measured will be 0.X μS ± 1/2 0.0X μS.

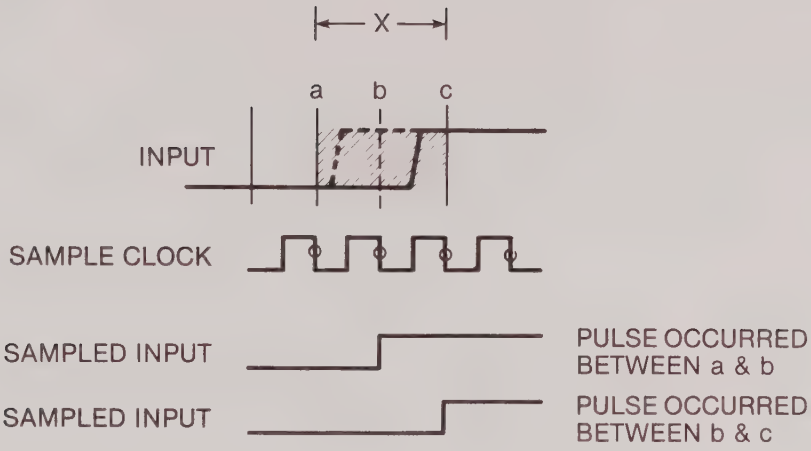
Figure 8-2. Shortest Time Limit.

theory states that a signal must be sampled at a rate at least twice as fast as the signal's own frequency in order for every transition to be detected (see Figures 8-3 and 8-4). For example, a resolution of 1 microsecond requires sampling at least every 500 nanoseconds. The sampling frequency should be equal to (2/X) hertz or higher (see Figure 8-5).

Another approach to calculating a good sampling frequency is to consider the resolution or precision you want in reconstructing an input signal. The signal transition can occur either before or after a sample clock edge because they are asynchronous by definition. There is always an uncertainty of one sample period between the actual signal and the digitized signal as to when a transition actually occurred. This one-sample uncertainty determines the resolution of your digitized sample input. For example, sampling five times faster than the input signal gives an uncertainty of 1 part in 5 (20%) and the best resolution possible is 80%. Sampling 10 times faster gives an uncertainty of 1 part in 10 (10%) for a 90% resolution. Sampling 100 times faster gives an uncertainty of 1 in 100 (1%) and a 99% resolution. For example, if the signal frequency is 1 megahertz (period of 1 microsecond) and you want 10% maximum uncertainty, sample at least every 100 nanoseconds. If you need X% resolution, your sampling frequency must equal the input signal frequency multiplied by 1/X (where X is a decimal number such as 0.1, 0.25, and so on).

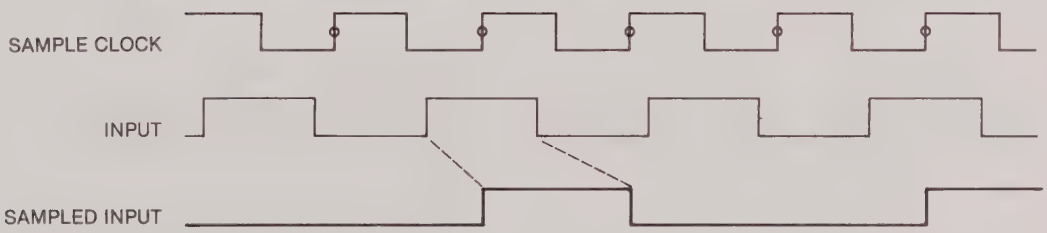
8.2.1.2 **Window Size**

Next you need to consider how much timing information to obtain, that is, the size of the information "window" (see Figure 8-6). Memory capacity is limited. The higher the resolution the more memory required and the smaller the available window. You must make tradeoffs between the amount of system activity you can see at one time and the amount of detail you can see for that activity. The decision can only be made by knowing your application and system characteristics. Often you will want to start with a wide window and narrow it to see finer detail.



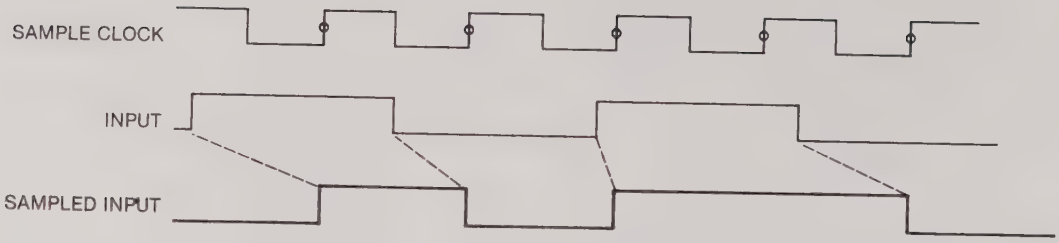
Note: With a sampling frequency of 2/X Hz, a pulse transition will be detected regardless of where it occurred between a and c. If the pulse transition occurred between points a and b, it is displayed as rising at b. If the pulse transition occurred between points b and c, it is displayed as rising at c.

Figure 8-3. Appropriate Sampling Frequency.



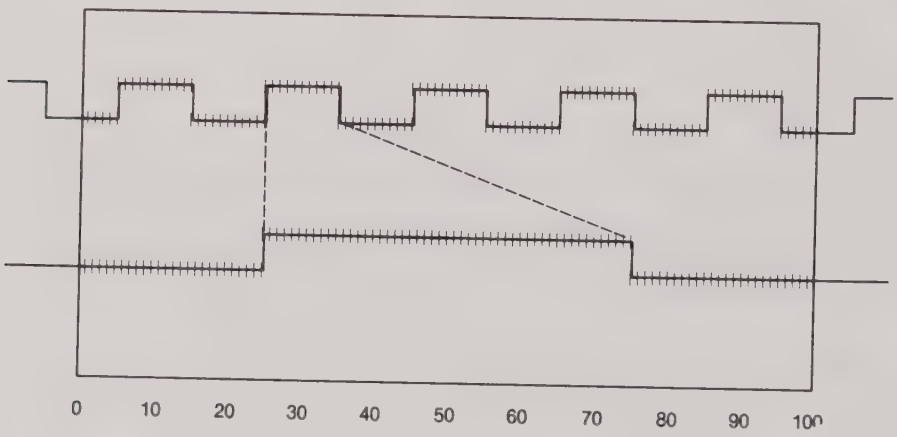
Note: Entire pulses are missed because the sampling frequency is less than twice as fast as the input signal's frequency.

Figure 8-4. Missed Pulses Due to Low Sampling Frequency.



Note: Every pulse is sampled since the sampling frequency is greater than twice the input signal's frequency.

Figure 8-5. Sampling at More Than 2X the Input Frequency.



Note: Sampling the same signal five times faster only lets you see 1/5th the amount of the initial information. In a 100 location memory, five full pulses can be seen when taking 20 samples per cycle. However, only one full cycle can be seen if the sampling rate is increased to 100 samples per cycle.

Figure 8-6. Window Versus Sampling Frequency.

Determine the amount of timing information you wish to see and the resolution you desire. Calculate whether these are compatible with the number of memory locations. Adjust the values if necessary.

8.2.1.3 **Glitch Capture**

You should consider the choice of input mode for recording. Latch mode can also be used as a sophisticated sample filter that prevents the trace control logic from evaluating samples during specified periods. For isolating general noise, however, Glitch mode should be selected. Although any of the four input modes may be used for timing analysis, Sample and Glitch are the most likely choices. A glitch is an unexpected narrow noise spike or transition. Glitches (large or small) often cause a system to operate incorrectly. If your system is acting in an unexplainable manner, it is a good idea to search for a glitch. In many cases, glitches can be detected in Sample mode if the sample clock is approximately ten or more times faster than your system's signals. Glitch mode is useful when the sample clock frequency is close to the system's signal frequencies (say, two to ten times faster), when you need to see noise spikes much narrower than the sample clock period but do not want to compromise window length, or when you suspect the presence of noise. By holding all other parameters constant, a difference between a recording made in Glitch mode and a recording made in Sample mode is a clear indication of a system noise problem.

8.2.1.4 **Typical Setup and Result**

A typical setup is shown in Figure 8-7 and a timing analysis display in Figure 8-8.

8.2.2 STATE ANALYSIS

State analysis (synchronous sampling) requires the use of an external clock signal. The purpose of a state analysis is to observe specific

CLOCK SELECT

MODE = INTERNAL or INTERNAL EXTENDED

INTERNAL CLOCK PERIOD = nearest legal value to required rate (1-16 sequence for each range)

MASTER CLOCK = INTERNAL

SAMPLE CLOCKS

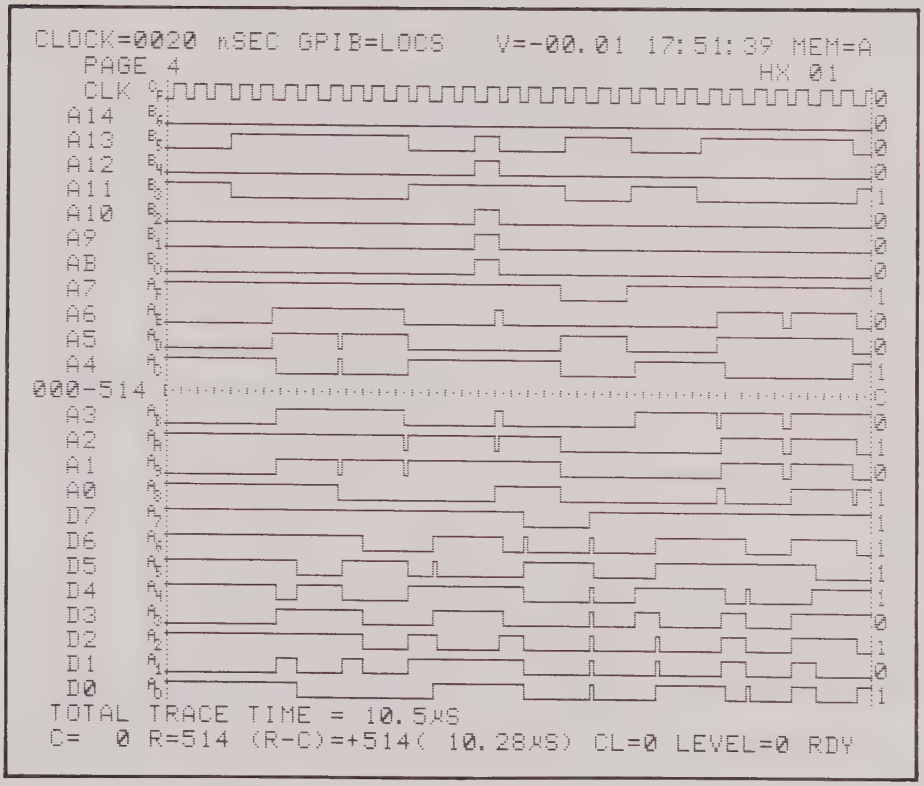
SECTION C = SAME AS MASTER or 10 NANOSECONDS
SECTION B = SAME AS MASTER or 10 NANOSECONDS
SECTION A = SAME AS MASTER or 10 NANOSECONDS

ENABLE

INPUT MODE

Input	Mode	Threshold
CF-C8	SAMPLE or GLITCH	as required
C7-C0	SAMPLE or GLITCH	as required
BF-B8	SAMPLE or GLITCH	as required
B7-B0	SAMPLE or GLITCH	as required
AF-A8	SAMPLE or GLITCH	as required
A7-A0	SAMPLE or GLITCH	as required

Figure 8-7. Typical Setup.



Note: Inputs may be labelled and rearranged to better see the time relationships between them. Each section's sampled inputs are time aligned. Up to 24 inputs may be simultaneously displayed.

Figure 8-8. Typical Timing Display.

activities in synchronization with all or only some portion of system activity. This allows you to see the execution and sequence of specific system states by recording comprehensive samples. By definition, a comprehensive sample gives you all the information you need about the specific system states (i.e., machine cycles, functions, or instructions), you have selected to observe.

State analysis allows you to precisely follow program flow and observe specific machine states. Comprehensive synchronous state samples increase the power, efficiency, and capabilities of trace control and, therefore, your problem solving abilities.

The approach recommended is to determine the states you want to observe, when and how to sample them, and the clocking plan you want to use.

8.2.2.1 **System State**

Determine what system state(s) you want to observe or follow: every state, only one type of state, or several particular states. This decision determines the amount and type of system activity you will see and what you will be able to learn about your system. Based on the problem at hand and the specifications of your system, clarify the states you need to sample.

Examples of system states you may want to select are clock cycle, read instruction, write instruction, wait, interrupt, I/O operation, memory access, instruction fetch, machine cycle, machine instruction, machine operation, subsystem function, and so on.

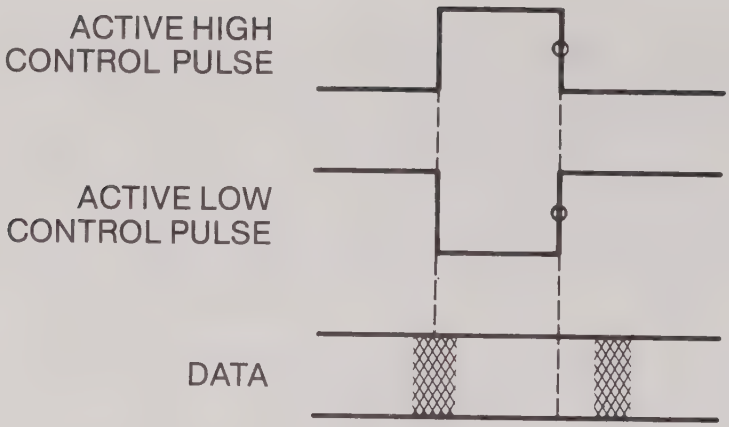
8.2.2.2 **When and How to Sample**

After you know what states you want to sample, you must next analyze when and how to sample them. This involves analyzing the functional descriptions of your system and its subsystems, their timing

characteristics, pinouts, schematics, specifications, operation, and so on. Information sources may be published documents, your own in-house documents, or previous tests. The latter may even include the results of a timing analysis performed by the K101-D. The purpose of this analysis is to determine the signal or combination of signals that define a particular state, indicate when the state is valid and for how long the signal is available for sampling. Ideally you want to determine a single method for obtaining one sample of each unique state. This will create your comprehensive sample.

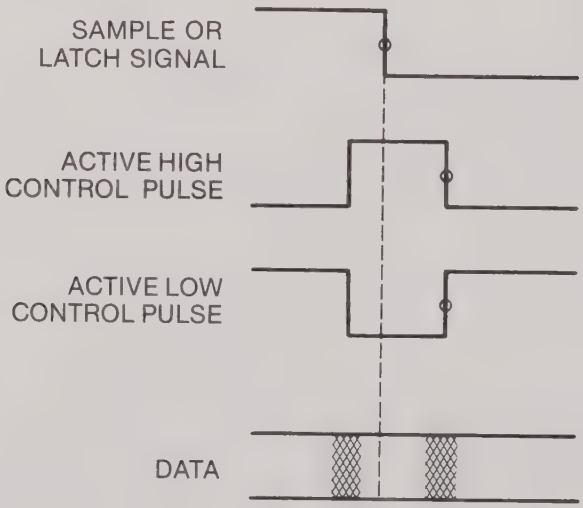
It is generally best to sample on the trailing edge of a pulse, whether the pulse is an active high or active low signal. This is because it is unlikely the data will have had time to become stable and valid at the rising edge of the pulse, especially if that rising edge initiates the transition from invalid to valid. However, the data are definitely valid and stable during and toward the end of the pulse. In most cases the data even remain stable a short time after the validating pulse has gone false. The data are therefore very likely to be valid on the trailing pulse edge. For an active high signal, the high-to-low (falling) edge is the trailing edge. For an active low signal, the low-to-high (rising) edge is the trailing edge (see Figures 8-9 and 8-10).

For example, from your analysis you may find any of the following situations: you need to take one sample every system clock cycle; a special control line exists solely to define the state you want to see; the state exists only when six control signals are in a particular relationship with each other; a particular combination of two lines indicates when your state is valid, but the signal you need to actually take the sample doesn't occur until after that valid period; the data of the state you want are multiplexed along with some other information you don't want. Several of these situations may apply concurrently. Whatever the situation is for your system, you now need to translate it into K101-D expressions.



Note: Data are generally valid on the trailing edge of their control signal pulse. It is best to sample on the falling edge of an active high signal and the rising edge of an active low signal.

Figure 8-9. Trailing Edge Detection.



Note: If the data are not valid on either pulse edge, then a separate signal must be found to indicate when to sample or to latch the data until they can be sampled on the trailing edge.

Figure 8-10. Alternate to Trailing Edge Detection.

8.2.2.3 **Calculate Specific Clocking Scheme**

Calculate the exact combination of sample clock expressions, master clock expression, latch enable expressions, and input modes that will fulfill your sampling needs. This often requires using Boolean algebra, including De Morgan's theorem, to generate the expressions. You also need to select the active edge of each signal that forms the expression and specify its rising edge for active low signals [X = X↑] and falling edge for active high signals [X = X↓]. Keep in mind that, by definition, the master and sample clocks sample on their rising edge.

There is no single method for producing the right expressions. As you approach the problem, consider both what you want to accomplish and what your actual capabilities are, given the available Boolean expressions. All Boolean expressions can be considered to be built out of two basic operations: two terms logically "ANDed" or "ORed" together, with either term able to be in one of two states (see Figure 8-11). These resulting expressions can then become terms in another operation, that resulting expression a term in yet another expression, and so on. Conversely, a complex equation can be reduced by the same method.

To help you calculate the specific sampling plan you need, the K101-D's state analysis clocking capabilities can be considered to be comprised of eight basic building blocks. Combining the specific blocks you need lets you create the sampling scheme you need. The eight basic clocking building blocks are shown in Figure 8-12 and explained in the list below.

A sample is taken only when the resultant changes from false to true. This occurs at the active edge of the signal that causes the expression to become true. Even if changes in the signal's state cause the expression to become true again, no sample is taken if the expression is already true.

$$X'' + Y' =$$
$$(X' \cdot Y) + Y' =$$
$$(X' \cdot Y) + [(X + Y) + Z] =$$
$$[(X + Y) \cdot Y] + [(X + Y) + Z] =$$

Note: A single-term expression can actually represent another multiple-term expression.

Figure 8-11. Boolean Expressions.

1. $R = X\uparrow + Y\uparrow$
2. $R = X\uparrow + Y\downarrow$
3. $R = X\downarrow + Y\uparrow$
4. $R = X\downarrow + Y\downarrow$
5. $R = X\uparrow \cdot Y\uparrow$
6. $R = X\uparrow \cdot Y\downarrow$
7. $R = X\downarrow \cdot Y\uparrow$
8. $R = X\downarrow \cdot Y\downarrow$

Where R is a resultant, sample or master clock expression, or sub-expression. This resultant can be substituted for a $Y\uparrow$ or $X\uparrow$ term of another operation when a combination of more than two input signals is needed. In this manner you can create the up to six term K101-D clock expression.

Figure 8-12. Basic Clock Building Blocks.

It may also be helpful to consider the disqualifier concept. The state of a disqualifier signal masks out any transitions of its partner signal. If one term is already true, any change in the other term is disqualified from causing the resultant to become true, and therefore no sample will occur.

a. $R = X\uparrow + Y\uparrow$

This expression is true when either X or Y is high. Therefore, R clocks when going from false to true (low to high). This occurs when X is low while Y is going from low to high, or when X is going from low to high while Y is low. X high disqualifies Y; Y high disqualifies X (see Figure 8-13).

b. $R = X\uparrow + Y\downarrow$

This expression is true when either X is high or Y is low. Therefore, R clocks when going from false to true (low to high). This occurs when X is low while Y is going from high to low, or when X is going from low to high while Y is high. X high disqualifies Y; Y low disqualifies X (see Figure 8-14).

c. $R = X\downarrow + Y\uparrow$

This expression is true when either X is low or Y is high. Therefore, R clocks when going from false to true (low to high). This occurs when X is high while Y is going from low to high, or when X is going from high to low while Y is low. X low disqualifies Y; Y high disqualifies X (see Figure 8-15).

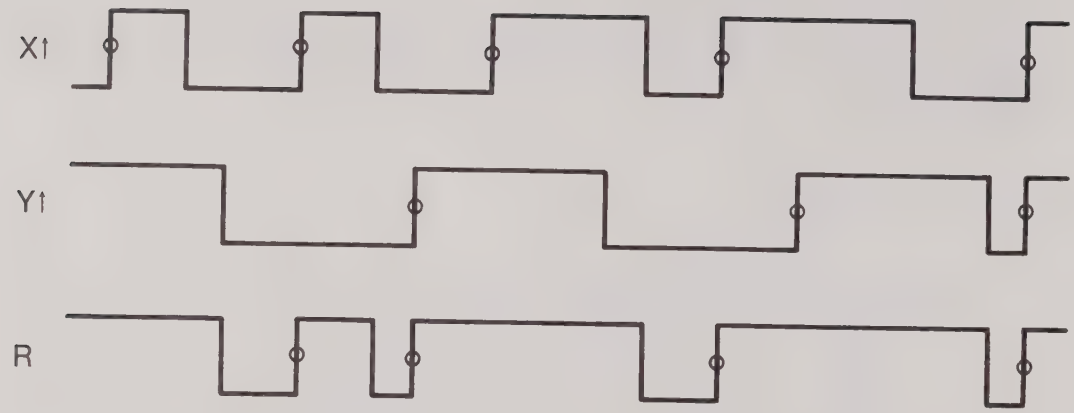


Figure 8-13. X↑ = Y↑.

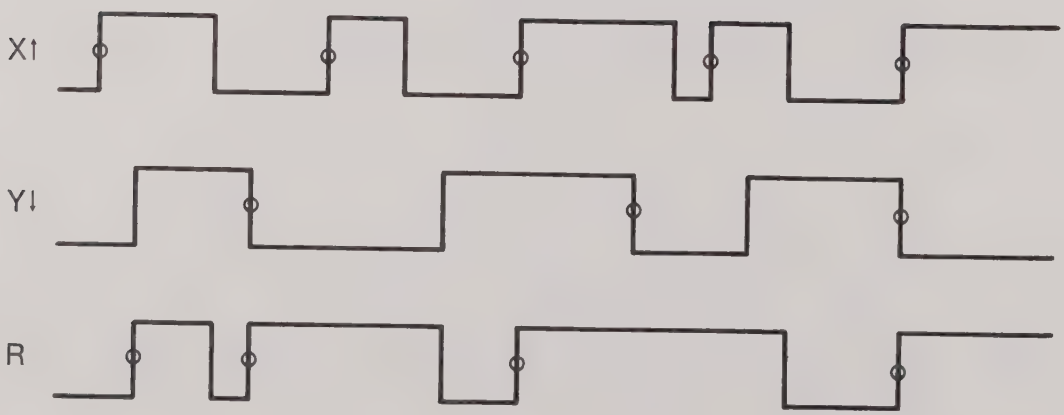


Figure 8-14. X↑ + Y↓.

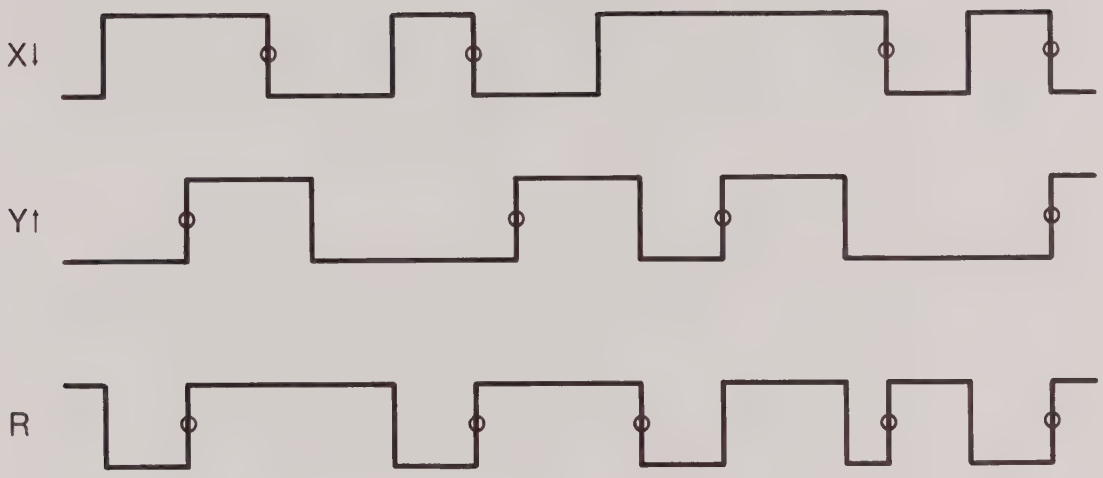


Figure 8-15. X↓ + Y↑.

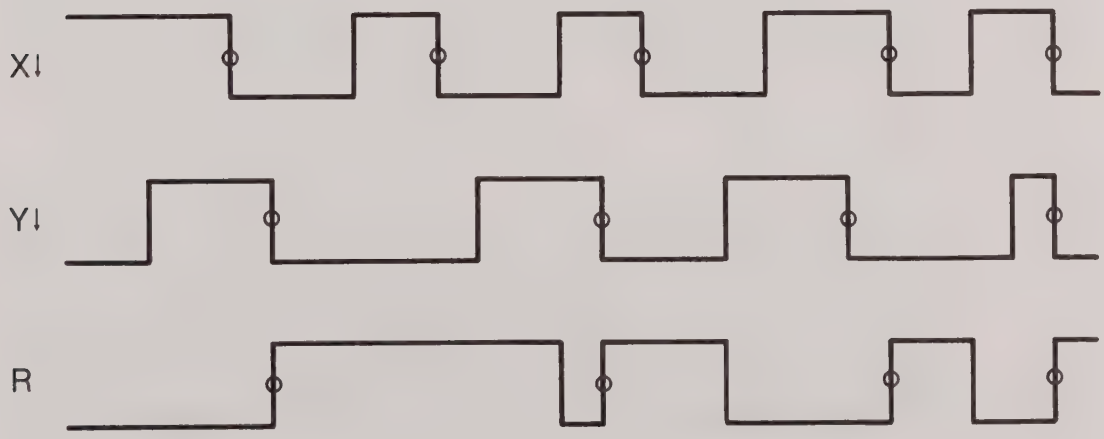


Figure 8-16. X↓ + Y↓.

d. $R = X\downarrow + Y\downarrow$

This expression is true when either X or Y is low. Therefore, R clocks when going from false to true (low to high). This occurs when X is high while Y is going from high to low, or when X is going from high to low while Y is high. X low disqualifies Y; Y low disqualifies X (see Figure 8-16).

e. $R = X\uparrow \cdot Y\uparrow$

This expression is true only when both X and Y are high. Therefore, R clocks when going from false to true (low to high). This occurs when X is high while Y is going from low to high, or when X is going from low to high while Y is high. X low disqualifies Y; Y low disqualifies X (see Figure 8-17).

f. $R = X\uparrow \cdot Y\downarrow$

This expression is true only when X is high and Y is low. Therefore, R clocks when going from false to true (low to high). This occurs when X is high while Y is going from high to low, or when X is going from low to high while Y is low. X low disqualifies Y; Y high disqualifies X (see Figure 8-18).

g. $R = X\downarrow \cdot Y\uparrow$

This expression is true only when X is low and Y is high. Therefore R clocks when going from false to true (low to high). This occurs when X is low while Y is going from low to high, or when X is going from high to low while Y is high. X high disqualifies Y; Y low disqualifies X (see Figure 8-19).

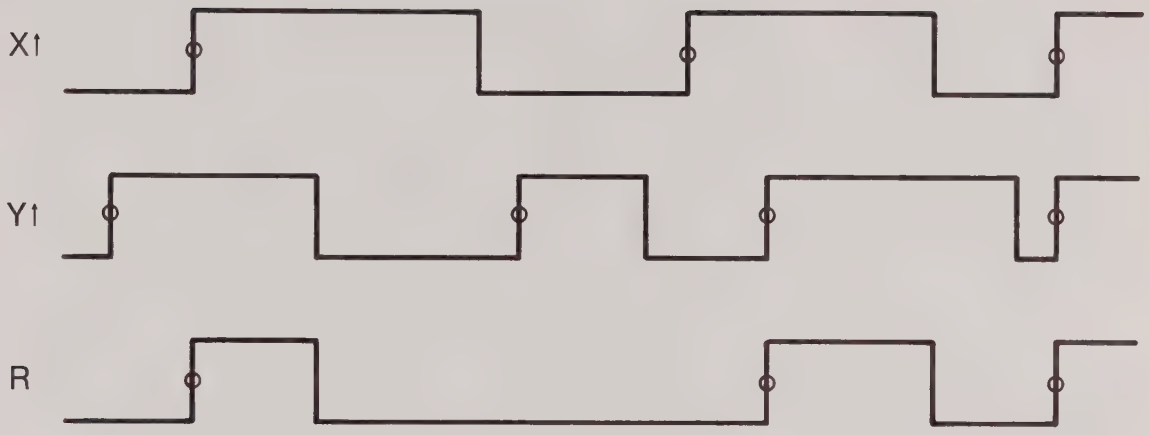


Figure 8-17. X↑ · Y↑.

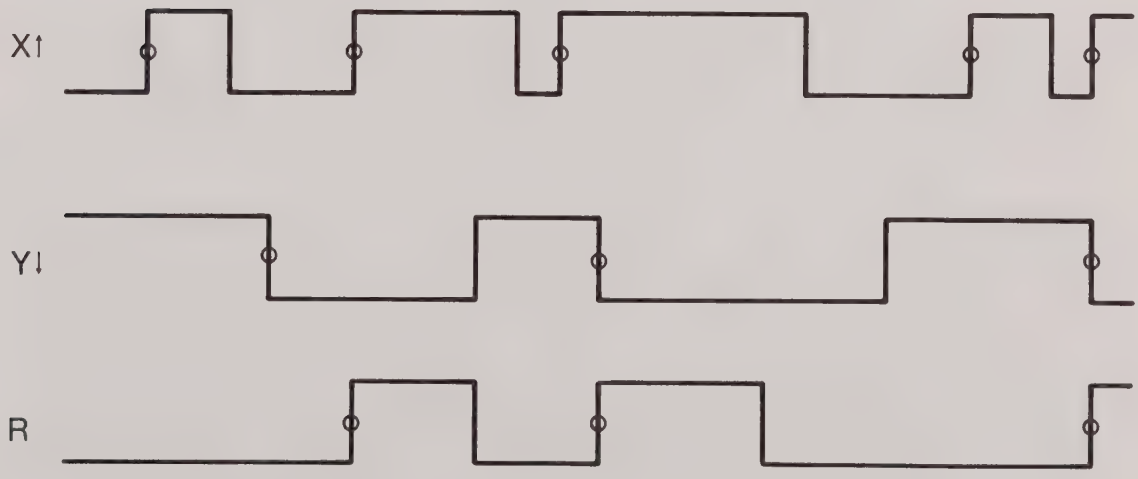


Figure 8-18. X↑ · Y↓.

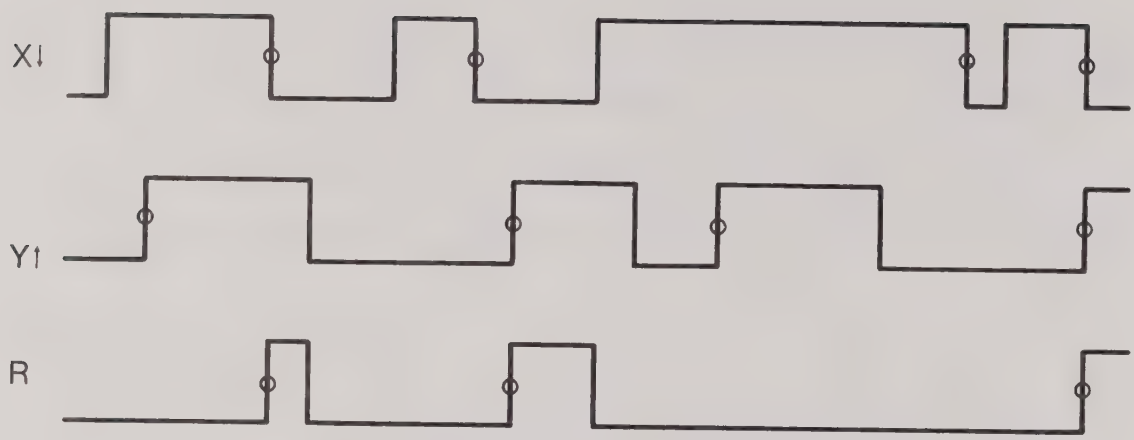


Figure 8-19. X↓ · Y↑.

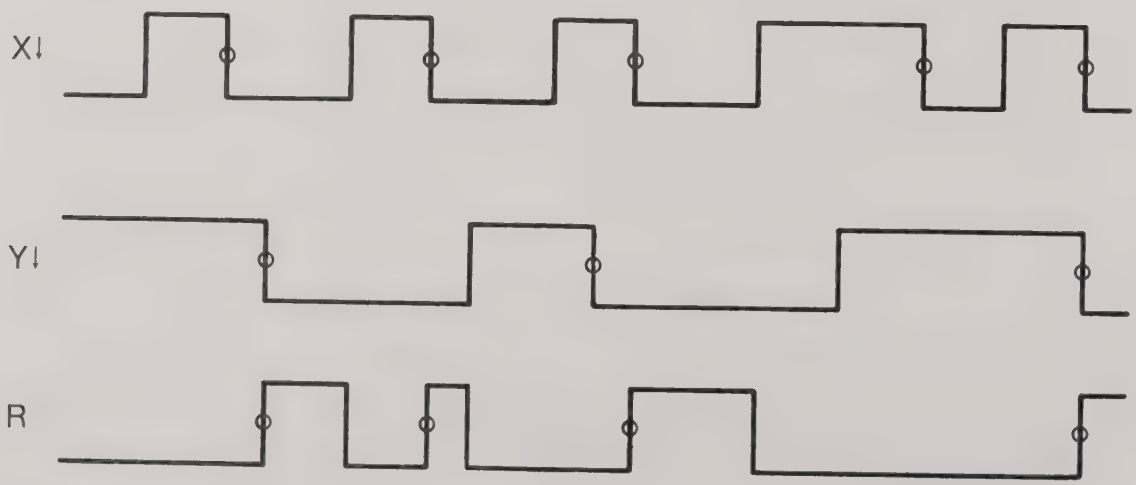


Figure 8-20. X↓ · Y↓.

h. $R = X\downarrow \cdot Y\downarrow$

This expression is true only when both X and Y are low. Therefore, R clocks when going from false to true (low to high). This occurs when X is low while Y is going from high to low, or when X is going from high to low while Y is low. X high disqualifies Y; Y high disqualifies X (see Figure 8-20).

8.2.3 COMBINED STATE AND TIMING ANALYSIS: MIXED SINGLE-/MULTI-PHASE

Combined analysis is used to obtain both timing and state information in the same recording. This allows you to review asynchronous timing relationships when a specified synchronous event occurs.

Combined analysis simultaneously follows both the micro and macro operation of a system. Detailed information on timing and on the relationship of synchronous activity is always available. This is especially helpful in capturing timing errors that cause observed system state errors in real time.

Use the same methods described in paragraphs 8.2.1 and 8.2.2 (Timing Analysis and State Analysis, respectively). Determine which signals to observe and how to sample them. Connect those signals to the sample inputs of a section(s) and set up the required internal sampling rate for that section(s). Using the methods described in state analysis, determine which signals and system states you need to observe and how to comprehensively sample that information. Connect these signals to the clock and sample inputs of a different section(s) and set up the required external master, section sample, and section enable expressions. The signals you observe asynchronously do not have to be the same ones you observe synchronously; they may or may not be the same depending on your application.

Set up the clock and input parameters you need. For trace control to follow the system's state activity, create a data format of the required sample inputs. To have the asynchronous activity flow continuously through memory, select TRACE ALWAYS for each trace control level used.

Once the recording is completed it is important to precisely relate information between section sampling at different rates, i.e., the information recorded by synchronously sampled sections to the information recorded by asynchronously sampled sections. Remember that trace control decisions (including the STOP command and the storage of state activity from all externally clocked sections) occur at the external master clock rate.

The timing information obtained by internally clocked sections is transferred into memory at that section's internal sample rate. Therefore, sections have significantly different information window lengths. Many asynchronous samples are taken in the same time interval in which only a few synchronous samples are taken. This creates a skew between the samples of each section. In other words, at memory location XXX, section A-sampled inputs are not time aligned with the section B-sampled inputs, which in turn are not time aligned with the section C-sampled inputs.

8.2.4 TIME RELATIONSHIP

By definition, the inputs of all sections are time related to each other when they first enter the logic analyzer and are clocked into the Sample Register (location 514 or SAM) by their respective section sample clocks (assuming Latch is not enabled). (It may help to refer to Figure 8-19 during the following discussion.) The Sample Register contents are then sent to Trace control for evaluation and also clocked on towards memory through P-1 (location 513) and P-2 (location 512). It takes two master clock cycles for Trace Control to evaluate a sample against the four trace control conditional commands. If the sample it is evaluating satisfies a stop condition then a HALT signal is generated by Trace Control at the end of that trace period. It is not until the next

sample clock pulse of each section that the HALT signal is accepted and sampling stops. Since it takes one more sample clock pulse to implement the HALT command, the contents of the Sample Register get shifted on to location 513 and replaced by new samples before sampling halts. Therefore the time related section samples are left in location 513 at the end of a recording. This is the only memory location where the inputs of all sections are aligned in time with each other. From that location on the inputs of each section will be skewed since many asynchronous samples continued to flow into memory while the trace control evaluations were being made. Asynchronously clocked information will be much farther forward in memory that its related externally clocked information.

There is usually no fixed relationship between the information presented to Trace Control or recorded by externally clocked sections and information recorded by internally clocked sections. As each master clock edge occurs, an additional skew accumulates between preceeding master clocks and the timing information corresponding to each of these clocks. Typically, master clock active edges do not occur at a uniform rate; they are usually aperiodic. Therefore there is no way to calculate the skew relationship. The best way to see the relationship between the various sections is to record all the signals used to form the master clock expression on unused inputs of an asynchronously clocked section. This way you can see every location in the asynchronous section where a master clock edge occurs. Beginning with location 513, each such occurrance corresponds to one sample in the externally clocked section(s).

A similar time skew will occur between sections clocked at different internal rates, i.e., at the Internal Clock Period (20 ns to 160 ms range) and 10 nanoseconds. However, since the internal rates have a constant ratio the sections will have a fixed time relationship and the skew between them will accumulate at a known constant rate.

In the special case where your master clock is operating at a fixed frequency it is possible to calculate the exact asynchronous sample location (Loc_{Asynch}) where each synchronous sample occurred (Loc_{Sync}) by the following formula.

$$Loc_{Asynch} = 513 - \left[(513 - Loc_{Sync}) \times \frac{\text{Master Period}}{\text{Internal Period}} \right]$$

For example, the same eight inputs are sampled by the clocking scheme of Figure 8-21. The master clock period is constant and the input mode is SAMPLE for all section inputs (see Figure 8-22). Using the above formula the section B sample that corresponds to the section A sample in location 511 is

$$= 513 - \left[(513 - 511) \times \frac{1.00\ \mu s}{50\ ns} \right]$$

$$= 513 - (2 \times 20)$$

$$= 473$$

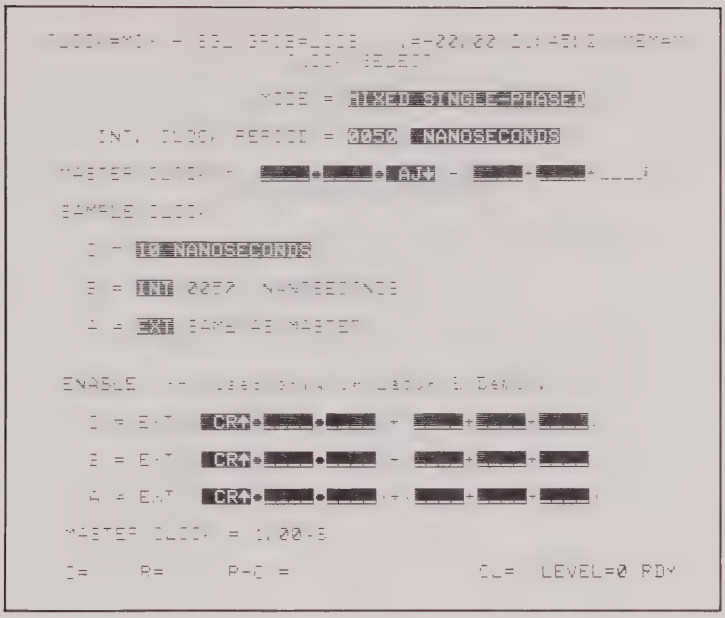
The section C sample that corresponds to the section A sample in location 511 is

$$= 513 - \left[(513 - 511) \times \frac{1.00\ \mu s}{10\ ns} \right]$$

$$= 513 - (2 \times 100ns)$$

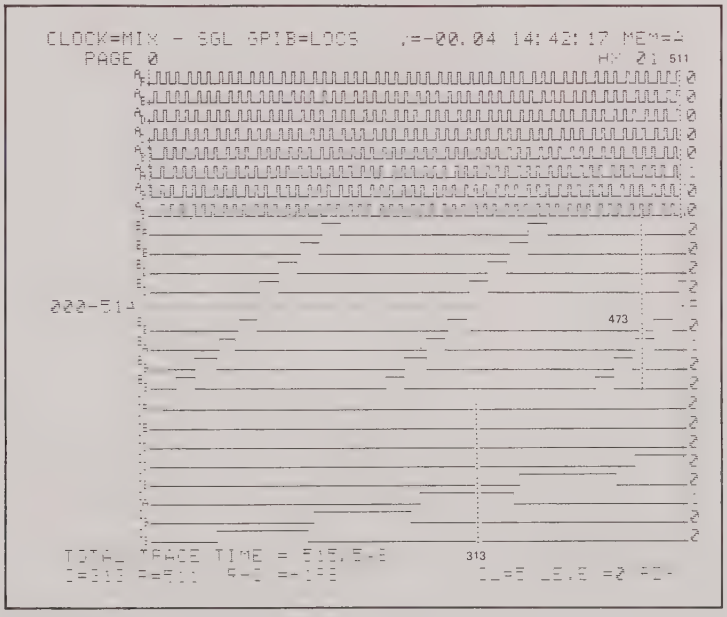
$$= 313$$

The same thing can be seen in the data domain (Figures 8-23 and 8-24). The 20 section B words (08) in location 490 through 509 correspond to the single section A word in location P-2 (512). Similarly, the 20 B words (04) in location 470 through 489 correspond to the single A word in location 511. As calculated previously the section A sample clock that took the location 511 sample occurred at location 473 in section B.


MODE = FIXED SINGLE-PHASED
INT. CLOCK PERIOD = 0050 NANOSECONDS
SAMPLE CLOCK:
1 = 10 NANOSECONDS
3 = EXT SAMPLE AT MASTER
MASTER CLOCK = 1.00-8

Note: The same eight inputs are sampled by these three different internal and external clocks.

Figure 8-21. Sample Location.



Note: Time alignment of section B and C inputs to the section A inputs in location 511 as sampled by the above clocking scheme.

Figure 8-22. Time Alignment of Section Inputs as Sampled In Figure 8-21.

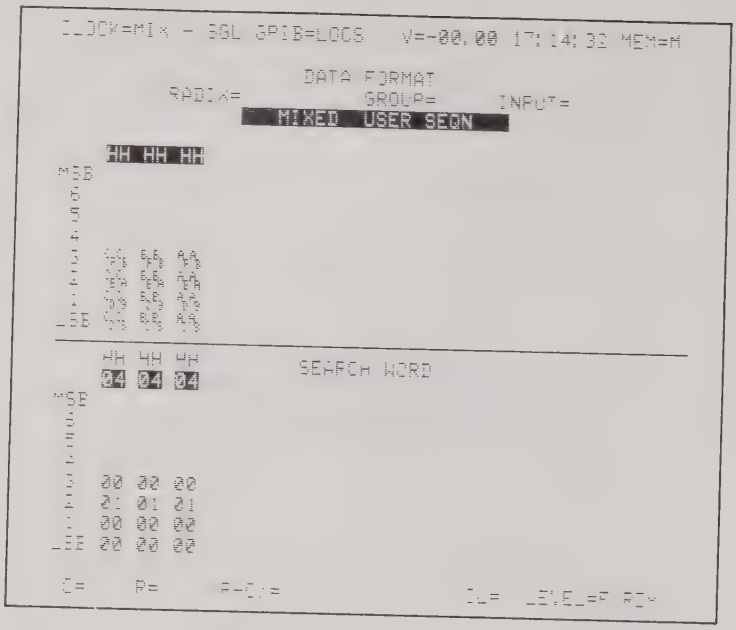


Figure 8-23. Data Format Used to Make the Following Data Display.

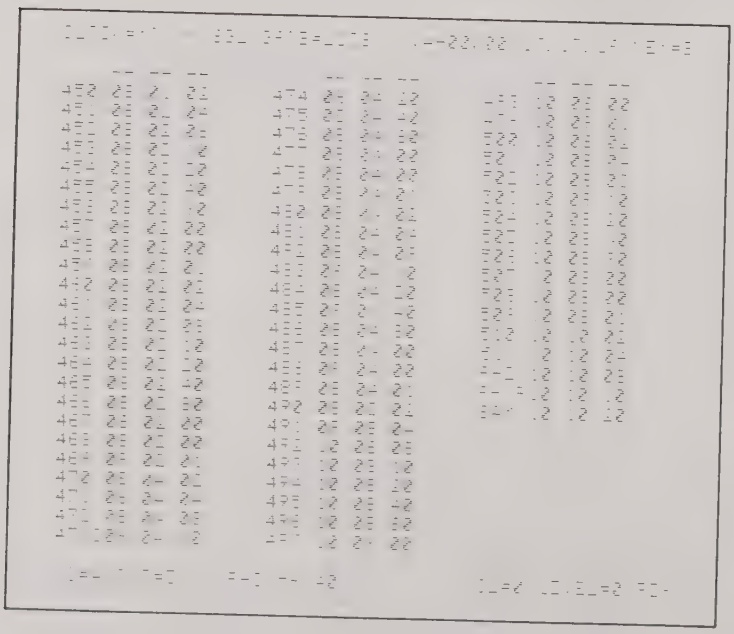


Figure 8-24. The Time-Aligned Section A, B, and C Words (10) in Location P-1 (513).

8.3 TRACE CONTROL

8.3.1 INTRODUCTION

Through the use of the various trace control command options, a virtually unlimited number of different tracing setups can be specified. However, there are several commonly used basic trace routines which can be considered as building blocks. By using variations of these basic building blocks in combination you can easily construct the necessary setups for monitoring and capturing precise information from even the most complex data stream.

The basic components and concepts of trace control are presented in paragraph 8.3.2 (Basic Building Blocks). An understanding of these items is essential to the productive use of the powers of trace control and the K101-D. The commands listed in the trace control setup should be considered as illustrations only. As in all programming, there are various ways to accomplish a particular result.

Paragraph 8.3.3 (Advanced Applications) presents a sampling of more complex and specific trace routine examples, which utilize variations and combinations of the basic building blocks. These examples are by no means exhaustive.

8.3.2 BASIC BUILDING BLOCKS

The basic trace control building blocks are presented in Figures 8-25 through 8-39. These figures are arranged in a standard format. A graphical representation of the item is presented at the top of the figure. The purpose, benefit, procedure and setup data are presented below the graphical representation.

The basic building blocks and their corresponding figure numbers are as follows:

a. Fill memory with samples from anywhere in data stream; Figure 8-25.

b. Wait for a specific event to occur, then record (four cases); Figure 8-26.

c. Record what happens immediately after an event; Figure 8-27.

d. Record what happens immediately before an event; Figure 8-28.

e. Record what happens around an event; Figure 8-29.

f. Record what happens long after an event; Figure 8-30.

g. Capture a segment of samples: record from here to there; Figure 8-31.

h. Exclude recording a segment of samples: don't record from here to there; Figure 8-32.

i. Selectively record only one kind sample (two cases); Figure 8-33.

j. Follow a certain path, then record; Figure 8-34.

k. Record, then follow a certain path; Figure 8-35.

l. Check for Event 1 or Event 2 and take a different path depending on which event occurred; Figure 8-36.

m. Check for Event 1 or Event 2 and take the same path regardless of which event occurred; Figure 8-37.

n. Check for correct timing between two events; Figure 8-38.

o. Continuously monitor for correct operation; Figure 8-39.

8.3.3 ADVANCED APPLICATIONS

These applications are examples of how the basic building blocks can be combined into more complex routines. The examples are presented in Figures 8-38 through 8-44 as follows:

a. Check for correct pulse width or skew; Figure 8-40.

b. Record a nested subroutine; Figure 8-41.

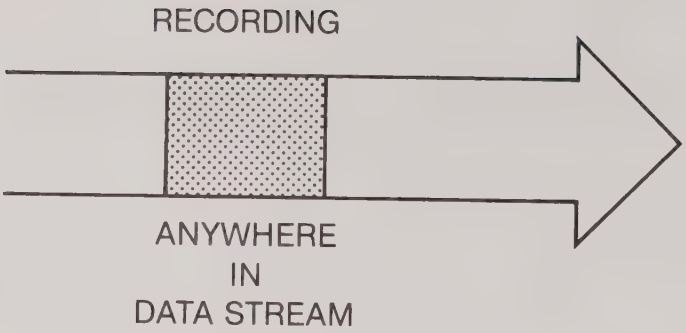
c. Capture multiple subroutines; Figure 8-42.

d. Record main program only; Figure 8-43.

e. Check for unknown errors in real time; Figure 8-44.

f. Record and check for correct execution; Figure 8-45.

g. Isolate program execution essentials; Figure 8-46.



PURPOSE: To capture any sequential data sample window.

BENEFIT: Is the simplest method of checking if the system under test is operational, if the logic analyzer is set up properly, and to see what is happening in the system under test.

PROCEDURE: Samples begin tracing into memory upon the ARM command and stop tracing when the memory is full.

SET UP:

LEVEL 0 DELAY = DEC 512 CLOCKS

COMMENTS

STOP IF DATA = S AND SAMPLE COUNT > DELAY
S=(Don't Care)

Until memory is full,

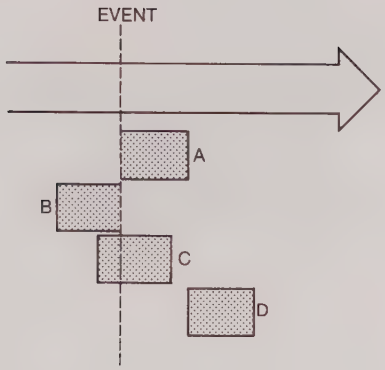
JUMP TO 0 NEVER
J=(Don't Care)

ADVANCE NEVER
A=(Don't Care)

TRACE ALWAYS
T=(Don't Care)

record everything.

Figure 8-25. Fill Memory with Samples from Anywhere in Data Stream.



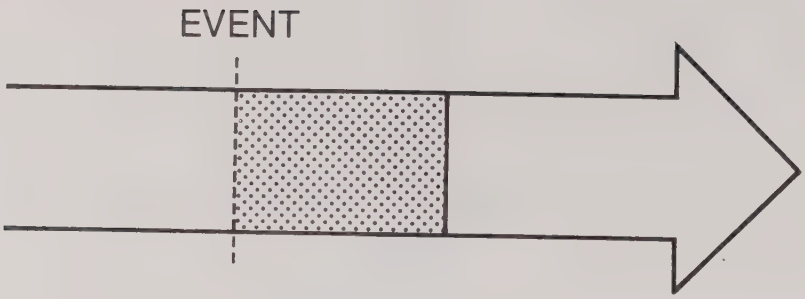
PURPOSE: To record samples around a specific event of interest.

BENEFIT: Focuses in on a specific area of interest. Helps eliminate unwanted samples.

PROCEDURE: See one of the four cases.

SETUP: See one of the four cases.

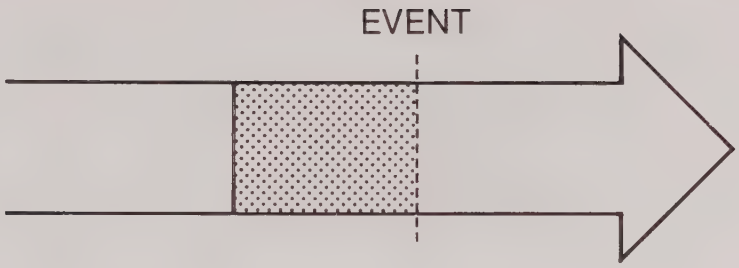
Figure 8-26. Wait for a Specific Event to Occur, Then Record (Four Cases).



PROCEDURE: Upon the occurrence of a specified event, begin tracing and stop when memory is full. (The specified event will be in the first memory location.)

SET UP:	COMMENTS
LEVEL 0 DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Don't Care)	
JUMP TO 0 NEVER J=(Don't Care)	
ADVANCE IF DATA = A A=(EVENT)	Wait for EVENT and advance when found.
TRACE IF DATA = T T=(EVENT)	Record EVENT when found.
LEVEL 1 DELAY = DEC 511 CLOCKS	
STOP IF DATA = S AND SAMPLE COUNT = DELAY S=(Don't Care)	Until memory is full,
JUMP TO 0 NEVER J=(Don't Care)	
ADVANCE NEVER A=(Don't Care)	
TRACE ALWAYS T=(Don't Care)	record everything.

Figure 8-27. Record What Happens Immediately After an Event (Case A).



PROCEDURE: Trace everything until a specific event occurs. Stop tracing immediately. (The event will be in the last location of memory.)

SET UP:

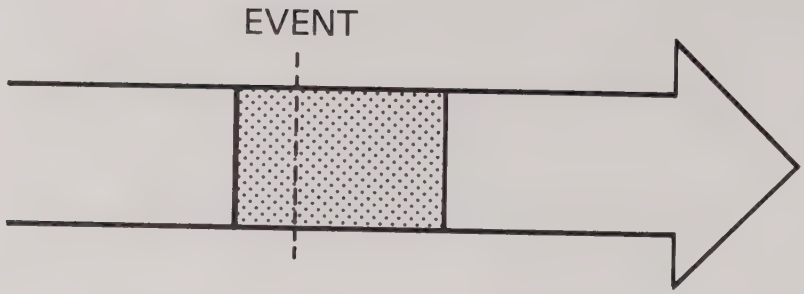
	COMMENTS
LEVEL 0 DELAY = DEC 515 CLOCKS	
STOP IF DATA = S S=(EVENT)	Stop immediately when EVENT occurs.
JUMP TO 0 NEVER J=(Don't Care)	
ADVANCE NEVER A=(Don't Care)	
TRACE ALWAYS T=(Don't Care)	Record everything.

NOTE: The event of interest could occur before 512 samples has occurred, thereby having some samples still in memory which is unrelated to the current recording. The following will "fill" the memory with new samples before advancing to look for the event.

SET UP:

	COMMENTS
LEVEL 0 DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Don't Care)	
JUMP TO 0 NEVER J=(Don't Care)	
ADVANCE IF DATA = A AND SAMPLE COUNT≥ DELAY A=(Don't Care)	Advance after a memory full (515)
TRACE ALWAYS T=(Don't Care)	of sample clocks has occurred. Trace everything.
LEVEL 1 DELAY = DEC 515 CLOCKS	
STOP IF DATA = S S=(EVENT)	Stop immediately when EVENT occurs.
JUMP TO 0 NEVER J=(Don't Care)	
ADVANCE NEVER A=(Don't Care)	
TRACE ALWAYS T=(Don't Care)	Record everything.

Figure 8-28. Record What Happens Immediately Before an Event (Case B).

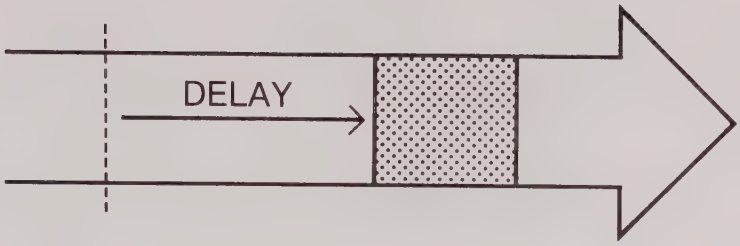


PROCEDURE: Trace everything while waiting for an event to occur. When it occurs, count out the delay needed to position it where you want in memory.

SET UP:

	COMMENTS
LEVEL 0 DELAY = DEC 515 CLOCKS	
STOP NEVER	
S=(Don't Care)	
JUMP TO 0 NEVER	
J=(Don't Care)	
ADVANCE IF DATA = A	Advance when
A=(EVENT)	EVENT occurs.
TRACE ALWAYS	
T=(Don't Care)	Trace everything.
LEVEL 1 DELAY = DEC nnnnn CLOCKS	
STOP IF DATA = S AND SAMPLE COUNT = DELAY	Record for nnnnn
S=(Don't Care)	more clocks and
JUMP TO 0 NEVER	then stop (nnnnn
J=(Don't Care)	must be ≤ 511
ADVANCE NEVER	clocks in order to
A=(Don't Care)	hold EVENT in
TRACE ALWAYS	memory.
T=(Don't Care)	

Figure 8-29. Record What Happens Around an Event (Case C).

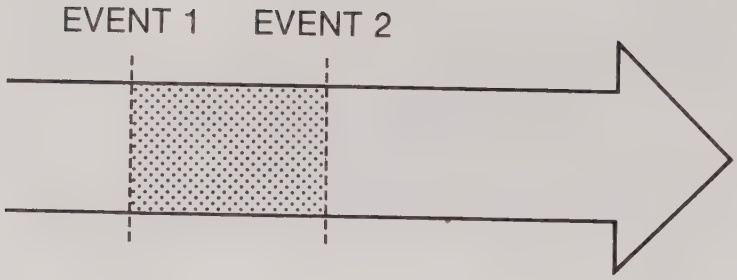


PROCEDURE: After an event occurs, delay the start of recording until a set period of time has passed. Record a segment and stop. (The event need not appear anywhere in memory.)

SET UP:

	COMMENTS
LEVEL 0 DELAY = DEC 515 CLOCKS	
STOP NEVER	
S=(Don't Care)	
JUMP TO 0 NEVER	
J=(Don't Care)	
ADVANCE IF DATA = A	Wait for EVENT to occur, then advance.
A=(EVENT)	
TRACE NEVER	
T=(Don't Care)	
LEVEL 1 DELAY = DEC nnnnn CLOCKS	
STOP NEVER	
S=(Don't Care)	
JUMP TO 0 NEVER	
J=(Don't Care)	
ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY	Wait nnnnn clocks.
A=(Don't Care)	
TRACE NEVER	Don't record anything.
T=(Don't Care)	
LEVEL 2 DELAY = DEC nnn CLOCKS	
STOP IF DATA = S AND SAMPLE COUNT = DELAY	Record a segment nnnnn long and stop.
S=(Don't Care)	
JUMP TO 0 NEVER	
J=(NEVER)	
ADVANCE NEVER	
A=(Don't Care)	
TRACE ALWAYS	Record everything.
T=(Don't Care)	
*To record EVENT, change LEVEL 0 to the following:	
LEVEL 0 DELAY = DEC 515 CLOCKS	
STOP NEVER	
S=(Don't Care)	
JUMP TO 0 NEVER	
J=(Don't Care)	
ADVANCE IF DATA = A	Wait for EVENT, then advance.
A=(EVENT)	
TRACE IF DATA = T	
T=(EVENT)	Record EVENT.

Figure 8-30. Record What Happens Long After an Event (Case D).



PURPOSE: To record samples only between (and including) two specified events.

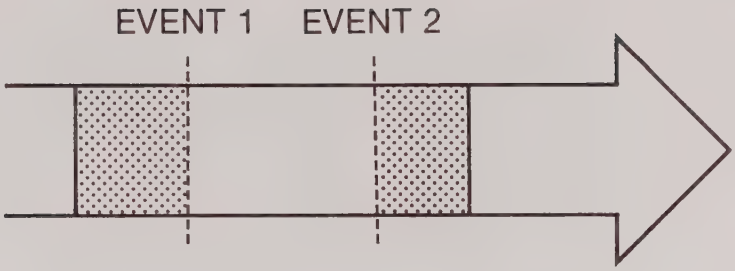
BENEFIT: Records only the segment of interest, helps eliminate unnecessary information.

PROCEDURE: Look for the first event, record it and everything following until the second event occurs, and then stop tracing.

SET UP:

	COMMENTS
LEVEL L DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Don't Care) JUMP TO 0 NEVER J=(Don't Care) ADVANCE IF DATA = A A=(EVENT 1) TRACE IF DATA = T T=(EVENT 1)	Wait for EVENT 1 to occur, then advance. Record EVENT 1.
LEVEL L+1 DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Don't Care) JUMP TO 0 NEVER J=(Don't Care) ADVANCE IF DATA = A A=(EVENT 2) TRACE ALWAYS T=(Don't Care)	Trace everything while waiting for EVENT 2 to occur, then advance.
LEVEL L+2 DELAY = DEC 515 CLOCKS	
STOP ALWAYS S=(Don't Care) JUMP TO 0 NEVER J=(Don't Care) ADVANCE NEVER A=(Don't Care) TRACE NEVER T=(Don't Care)	Stop tracing immediately.

Figure 8-31. Capture a Segment of Samples: Record from Here to There.



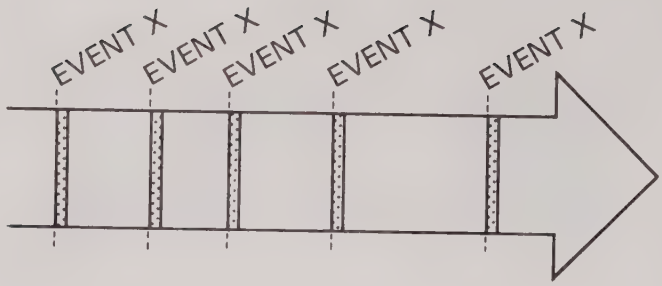
PURPOSE: To not record samples between two specific events.

BENEFIT: Eliminates unwanted information, conserves memory space for wanted information.

PROCEDURE: Record until EVENT 1 occurs and stop recording. Continue tracing but don't start recording again until EVENT 2 occurs.

SET UP:	COMMENTS
LEVEL L DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Don't Care)	
JUMP TO 0 NEVER J=(Don't Care)	
ADVANCE IF DATA = A A=(EVENT 1)	Wait for EVENT 1 to occur, then advance.
TRACE ALWAYS T=(Don't Care)	Record everything before and including EVENT 1.
LEVEL L+1 DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Don't Care)	
JUMP TO 0 NEVER J=(Don't Care)	
ADVANCE IF DATA = A A=(EVENT 2)	Wait for EVENT 2 to occur, then advance.
TRACE IF DATA = T T=(EVENT 2)	Record EVENT 2.
LEVEL L+2 DELAY = nnnnn CLOCKS	
STOP IF DATA = S AND SAMPLE COUNT > DELAY S=(Don't Care)	Stop after nnnnn clocks.
JUMP TO 0 NEVER J=(Don't Care)	
ADVANCE NEVER A=(Don't Care)	
TRACE ALWAYS T=(Don't Care)	Record everything.

Figure 8-32. Exclude Recording a Segment of Samples: Don't Record from Here to There.



PURPOSE: To record only one specific type of sampled event.

BENEFIT: Excludes recording all information except that of specific interest; helps conserve memory space.

CASE A ALL

PROCEDURE: Look for and trace each and every occurrence of a specific event, trace only that event.

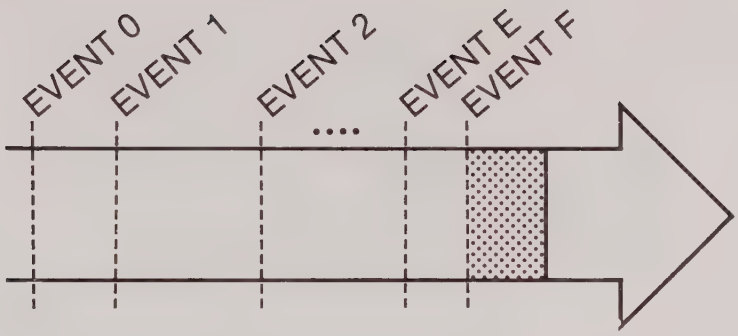
```
SET UP:                                          COMMENTS
LEVEL L DELAY = DEC 515 CLOCKS

  STOP (WHEN DESIRED)                            For as long as
S=(Don't Care)                                   desired,
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE NEVER
A=(Don't Care)
  TRACE IF DATA = T
T=(EVENT)                                        trace only EVENT.
```

CASE B FOR A CERTAIN NUMBER OF TIMES.

PROCEDURE: Look for and record a specific event only a certain number of times while tracing.

```
SET UP:                                          COMMENTS
LEVEL L DELAY = DEC nnnnn A PATTERNS

  STOP IF DATA = S AND SAMPLE COUNT = DELAY      Stop when nnnnn
S=(EVENT)                                        EVENTs (=A PATTERNS) have
  JUMP TO 0 NEVER                                happened.
J=(Don't Care)
  ADVANCE NEVER                                  Specify
A=(EVENT)                                        A PATTERNS=EVENT.
  TRACE IF DATA = T                              Record only
T=(EVENT)                                        EVENTs.
```

Figure 8-33. Selectively Record Only One Kind of Sample (Two Cases).



PURPOSE: A certain series of events must occur before a recording is made.

BENEFIT: Very precisely defines an area of interest to record, provides a way to get inside a multi-nested subroutine or to follow a complex program path.

PROCEDURE: Check for EVENT 0 to occur, then check for EVENT 1 to occur, et cetera, finally check for EVENT F to occur and record around it as desired. (Record immediately after is shown in the following example.)

```
SET UP:                                                    COMMENTS
LEVEL 0 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                                      Check for EVENT
A=(EVENT 0)                                                0; advance if
  TRACE NEVER                                              found.
T=(Don't Care)

LEVEL 1 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                                      Check for EVENT
A=(EVENT 1)                                                1; advance if
  TRACE NEVER                                              found.
T=(Don't Care)


LEVEL E DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A
A=(EVENT F)                                                Check for EVENT
  TRACE IF DATA = T                                        F; advance if
T=(EVENT F)                                                found.
                                                           Record (EVENT F).


LEVEL F DELAY = DEC nnnnn CLOCKS

  STOP IF DATA = S AND SAMPLE COUNT > DELAY                Stop after nnnnn
S=(Don't Care)                                             samples.
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE NEVER
A=(Don't Care)
  TRACE ALWAYS                                             Record everything.
T=(Don't Care)
```

Figure 8-34. Follow a Path, Then Record.

PURPOSE: To check that a specific series of events occurred after making a recording.

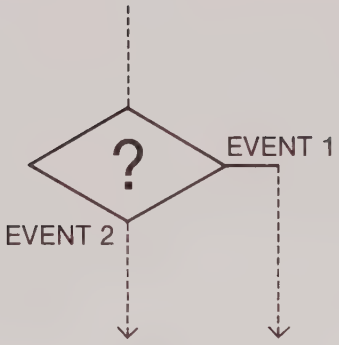
BENEFIT: Without losing the initial recording, later program execution points can be checked.

PROCEDURE: Record a segment of interest, stop recording, yet continue to trace subsequent program execution points.

SET UP:

	COMMENTS
LEVEL 0 DELAY = DEC 512 CLOCKS	
STOP NEVER S=(Don't Care) JUMP TO 0 NEVER J=(Don't Care) ADVANCE IF DATA = A AND SAMPLE COUNT > DELAY A=(Don't Care) TRACE ALWAYS T=(Don't Care)	Fill memory, then advance. Record everything.
LEVEL 1 DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Don't Care) JUMP TO 0 NEVER J=(Don't Care) ADVANCE IF DATA = A A=(EVENT 1) TRACE NEVER T=(Don't Care)	Check for EVENT 1; advance if found.
LEVEL 2 DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Don't Care) JUMP TO 0 NEVER J=(Don't Care) ADVANCE IF DATA = A A=(EVENT 2) TRACE NEVER T=(Don't Care)	Check for EVENT 2; advance if found.
. . .	Check for EVENT 3; advance if found. . . .

Figure 8-35. Record, Then Follow a Path.



PURPOSE: Monitor a particular point in the program flow for the occurrence of one of two possible events.

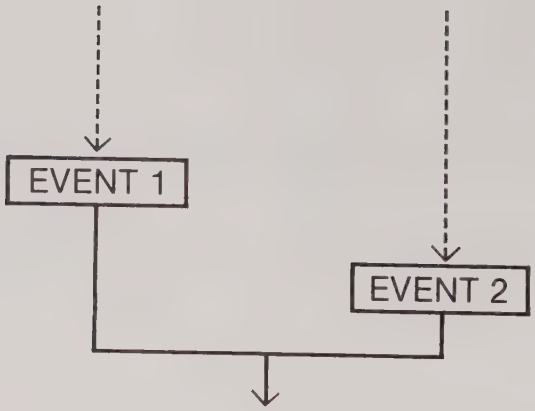
BENEFIT: Gives the ability to follow program branches, take alternative paths, and make decisions in real time.

PROCEDURE: Simultaneously check for 2 events. If EVENT 1 occurs, follow trace routine 1. If EVENT 2 occurs, follow trace routine 2.

SET UP:

	COMMENTS
LEVEL L DELAY = DEC 515 CLOCKS	
STOP NEVER	
S=(Don't Care)	
JUMP TO x IF DATA = J	
J=(EVENT 1)	Look for EVENT
ADVANCE IF DATA = A	1 or 2.
A=(EVENT 2)	
TRACE ALWAYS	
T=(Don't Care)	Trace everything, including the event that does occur.
LEVEL L+1 DELAY = DEC 515 CLOCKS	
STOP NEVER	
S=(Don't Care)	
JUMP TO 0 NEVER	If EVENT 2
J=(Don't Care)	happened, follow
ADVANCE IF DATA = A	trace routine 2.
A=(TR2)	
TRACE ALWAYS	
T=(Don't Care)	
LEVEL x DELAY = DEC 515 CLOCKS	
STOP NEVER	
S=(Don't Care)	
JUMP TO 0 NEVER	If EVENT 1
J=(Don't Care)	happened, follow
ADVANCE IF DATA = A	trace routine 1.
A=(TR1)	
TRACE ALWAYS	
T=(Don't Care)	

Figure 8-36. Check for Event 1 or Event 2 and Take a Different Path Depending on Which Event Occurred.



PURPOSE: Either of 2 events occurring will initiate the same subsequent action.

BENEFIT: Precise knowledge of which of 2 events will occur or when it will occur is not required. A particular trace routine can be reached by either of 2 paths.

PROCEDURE: Check for the occurrence of EVENT 1 and EVENT 2. If either occurs, advance to the next trace level.

SET UP:

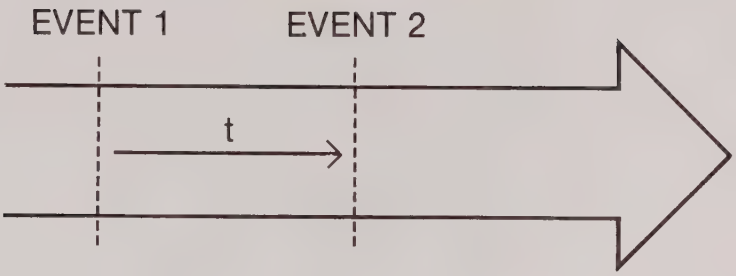
LEVEL L DELAY = DEC 515 CLOCKS

STOP NEVER
S=(Don't Care)
JUMP TO L+1 IF DATA = J
J=(EVENT 1)
ADVANCE IF DATA = A
A=(EVENT 2)
TRACE ALWAYS
T=(Don't Care)

COMMENTS

If EVENT 1 occurs, trace control goes to the next level. If EVENT 2 occurs, trace control goes to the next level. Trace everything, including the event that does occur.

Figure 8-37. Check for Event 1 or Event 2 and Take the Same Path Regardless of Which Event Occurred.



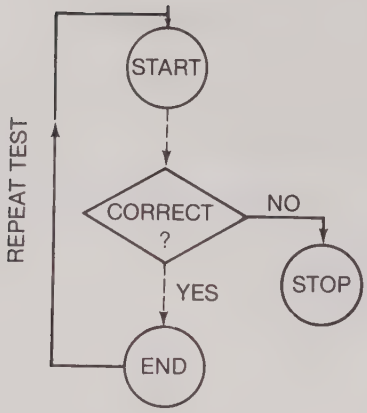
PURPOSE: To see if the time between 2 events is what it should be.

BENEFIT: Verifies correct operation, precisely identifies errors in real time allowing a decision to be made regarding further tracing.

PROCEDURE: Look for EVENT 1, then look for EVENT 2. Keep track of the times between them and compare it to the correct specified time. Take appropriate action based on the result of the comparison.

SET UP:	COMMENTS
LEVEL L DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Don't Care) JUMP TO 0 NEVER J=(Don't Care) ADVANCE IF DATA = A A=(EVENT 1) TRACE (DOESN'T MATTER) T=(Don't Care)	Check for EVENT 1 and advance when found. (Type of trace command chosen is irrelevant.)
LEVEL L+1 DELAY = DEC nnnnn CLOCKS	Where nnnnn is the specified correct time period between EVENT 1 & 2, EVENT 2 should not occur sooner than nnnnn clocks after EVENT 1. EVENT 2 should happen nnnnn clocks after EVENT 1. TRACE everything to be able to see sampled data in case the timing error occurred.
STOP NEVER S=(Don't Care) JUMP TO x IF DATA = J AND SAMPLE COUNT ≤ DELAY J=(EVENT 2) ADVANCE IF DATA = A AND SAMPLE COUNT > DELAY A=(EVENT 2) TRACE ALWAYS T=(Don't Care)	
LEVEL L+2 DELAY = DEC 515 CLOCKS	
STOP_____ S= JUMP TO 0_____ J= ADVANCE _____ A= TRACE_____ T=	Timing was correct; continue tracing as desired.
LEVEL x DELAY = DEC 515 CLOCKS	
STOP ALWAYS S=(Don't Care) JUMP TO 0 NEVER J=(Don't Care) ADVANCE NEVER A=(Don't Care) TRACE NEVER T=(Don't Care)	Timing error occurred; stop tracing immediately.

Figure 8-38. Check for Correct Timing Between Two Events.



PURPOSE: To monitor a particular point in a program through repeated executions of the program.

BENEFIT: Exercises hardware and software through repeated testing. Traps intermittent errors.

PROCEDURE: Check for an expected correct event to occur. If it does, run the program and trace test again. If an error ever occurs, stop tracing and look at what happened.

SET UP:

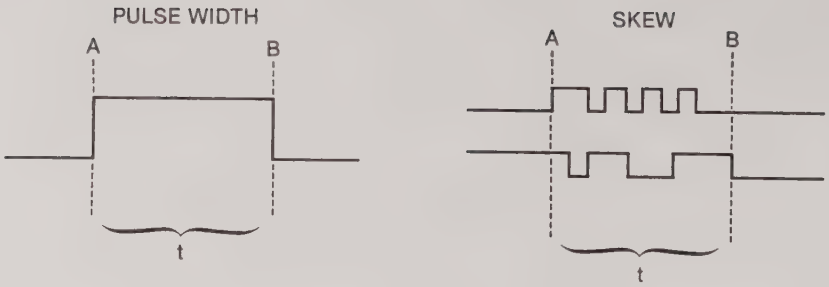
	COMMENTS
LEVEL L DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Don't Care)	
JUMP TO L IF DATA = J J=(CORRECT)	If the correct EVENT happens, loop back and run test again. If correct event didn't happen, an error occurred. Trace everything in case an error occurs.
ADVANCE IF DATA = A A=(Don't Care)	
TRACE ALWAYS T=(Don't Care)	
LEVEL L+1 DELAY = DEC 515 CLOCKS	
STOP ALWAYS S=(Don't Care)	Error occurred; stop and look at recording.
JUMP TO 0 NEVER J=(Don't Care)	
ADVANCE NEVER A=(Don't Care)	
TRACE ALWAYS T=(Don't Care)	

NOTE: In order for the trace routine to know exactly when to check for CORRECT, level L must be entered by an Advance from the event immediately preceeding CORRECT[1], or a time window in which CORRECT should occur must be specified[2], or a specific ERROR word that indicates CORRECT didn't happen must be known[3]. (See Sheet 2)

Figure 8-39. Continuously Monitor for Correct Operation (Sheet 1 of 2).

```
                                                        COMMENTS
[1]add
LEVEL L-1 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER                                       CORRECT should
J=(Don't Care)                                          occur immediately
  ADVANCE IF DATA = A                                   upon entering
A=(CORRECT-1)                                           level L.
  TRACE NEVER
T=(Don't Care)


[2]change
LEVEL L DELAY = DEC nnnnn CLOCKS                        nnnnn is specified
                                                        correct time window.

  STOP NEVER
S=(Don't Care)
  JUMP TO L IF DATA = J AND SAMPLE COUNT ≤ DELAY        CORRECT should happen
J=(CORRECT)                                             within nnnnn sample
  ADVANCE IF DATA = A AND SAMPLE COUNT > DELAY          clocks.
A=(Don't Care)                                          If CORRECT hasn't
  TRACE ALWAYS                                          happened by nnnnn
T=(Don't Care)                                          clocks, then an
                                                        error has occurred.

[3]change to
LEVEL L DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO L IF DATA = J                                 By definition, if
J=(CORRECT)                                             CORRECT doesn't
  ADVANCE IF DATA = A                                   happen then a
A=(ERROR)                                               known ERROR will.
  TRACE IF DATA = T
T=(ERROR)
```

Figure 8-39. Continuously Monitor for Correct Operation (Sheet 2 of 2).



Note: Uses basic building block of Figure 7.2-13.

PURPOSE: To verify if pulse width or skew is within specification.

BENEFIT: Tests pulse width or skew to specifications and allows a decision to be made on further tracing dependent upon the test results.

DESCRIPTION: A test may be run for either a minimum or maximum allowable specification.

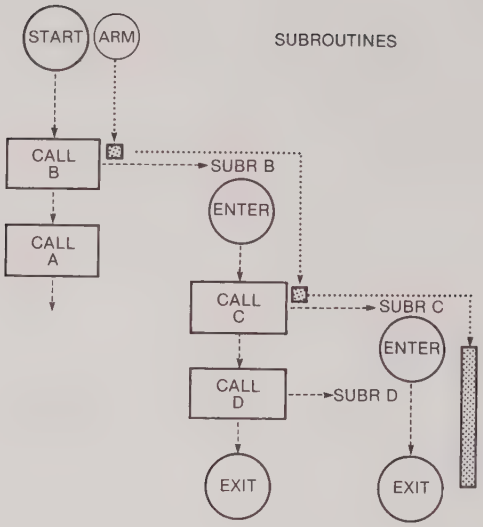
PROCEDURE: MIN - After point A, check that B occurs at least t sample clocks later. MAX - After point A, check that B occurs before t sample clocks have occurred.

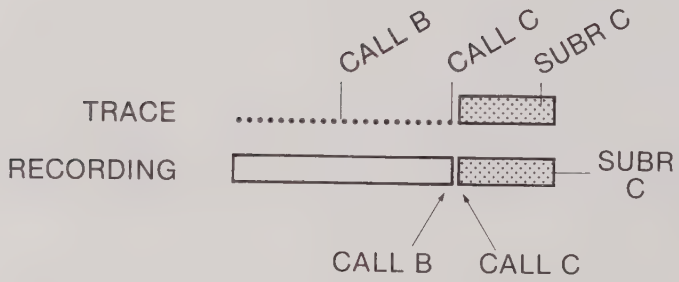
Figure 8-40. Check for Correct Pulse Width or Skew (Sheet 1 of 2).

SET UP:

	COMMENTS
MIN	
LEVEL 0 DELAY = 515 CLOCKS	
STOP NEVER	
S= (Don't Care)	
JUMP TO 0 NEVER	
J= (Don't Care)	
ADVANCE IF DATA = A	
A=(A)	
TRACE ALWAYS	
T=(Don't Care)	
LEVEL 1 DELAY = DEC t CLOCKS	
STOP NEVER	
S=(Don't Care)	
JUMP TO x IF DATA = J AND SAMPLE COUNT < DELAY	Jump to error routine if maximum time is exceeded. Continue testing if maximum is not exceeded.
J=(B)	
ADVANCE IF DATA = A AND SAMPLE COUNT ≥ DELAY	
A=(B)	
TRACE ALWAYS	
T=(Don't Care)	
MAX	
LEVEL 0 DELAY = DEC 515 CLOCKS	
STOP NEVER	
S=(Don't Care)	
JUMP TO 0 NEVER	
J=(Don't Care)	
ADVANCE IF DATA = A	
A=(A)	
TRACE ALWAYS	
T=(Don't Care)	
LEVEL 1 DELAY = DEC t CLOCKS	
STOP NEVER	
S=(Don't Care)	
JUMP TO x IF DATA = J AND SAMPLE COUNT > DELAY	Jump to error if maximum time is exceeded. Continue testing if maximum is not exceeded.
J=(B)	
ADVANCE IF DATA = A AND SAMPLE COUNT ≤ DELAY	
A=(B)	
TRACE ALWAYS	
T=(Don't Care)	

Figure 8-40. Check for Correct Pulse Width or Skew (Sheet 2 of 2).





PURPOSE: To only record 1 pass of a double nested subroutine.

BENEFIT: Execution of the main program and outer subroutines does not have to be recorded in order to capture only the subroutine of interest.

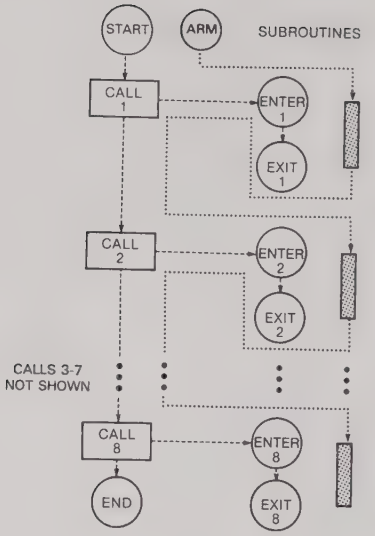
DESCRIPTION: The main program calls subroutines A and B. Subroutine B calls subroutine C and D. It is desired to record only subroutine C.

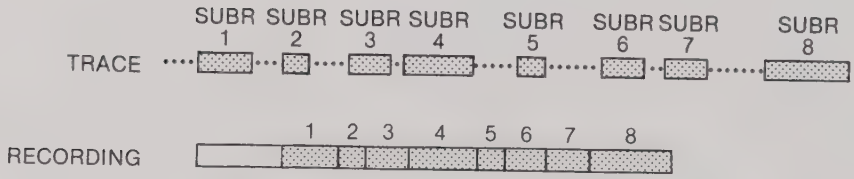
PROCEDURE: Look for subroutine B to be called, then look for subroutine C to be called. Record until subroutine C returns to B.

Figure 8-41. Record a Nested Subroutine (Sheet 1 of 2).

```
SET UP:                                                    COMMENTS

LEVEL 0 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                                      Look for and
A=(Call B)                                                 record Call B.
  TRACE IF DATA = B
T=(Call B)


LEVEL 1 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                                      Look for and
A=(Call C)                                                 record Call C.
  TRACE IF DATA = T
T=(Call C)


LEVEL 2 DELAY = DEC 515 CLOCKS

  STOP IF DATA = S                                         Record all of C
S=(Exit C)                                                 until it exits
  JUMP TO 0 NEVER                                          and stop.
J=(Don't Care)
  ADVANCE NEVER
A=(Don't Care)
  TRACE ALWAYS
T=(Don't Care)
```

Figure 8-41. Record a Nested Subroutine (Sheet 2 of 2).





PURPOSE: To record the execution of a series of subroutines, each of which can be separated by an indefinite period of time.

BENEFIT: Can capture many different subroutines in a single pass of the main program without needing an infinite depth memory or having to record the multitude of data in between each subroutine or record each execution of the same subroutine.

DESCRIPTION: The main program calls 8 non-contiguous sequential subroutines. One pass of each will be recorded as they execute.

PROCEDURE: Check for call subroutine 1, record until it exits, stop recording while checking for subroutine 2 to be called, then record until it exits, stop recording while looking for subroutine 3 to be called, et cetera. Stop tracing at the end of subroutine 8.

Figure 8-42. Capture Multiple Subroutines (Sheet 1 of 4).

```
SET UP:                                          COMMENTS
LEVEL 0 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                            Look for
A=(Call 1)                                       subroutine 1 to
  TRACE NEVER                                    be called.
T=(Don't Care)


LEVEL 1 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                            Record
A=(Exit 1)                                       subroutine 1.
  TRACE ALWAYS
T=(Don't Care)


LEVEL 2 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                            Look for
A=(Call 2)                                       subroutine 2.
  TRACE NEVER
T=(Don't Care)

                                                 COMMENTS
LEVEL 3 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                            Record
A=(Exit 2)                                       subroutine 2.
  TRACE ALWAYS
T=(Don't Care)


LEVEL 4 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                            Look for
A=(Call 3)                                       subroutine 3.
  TRACE NEVER
T=(Don't Care)
```

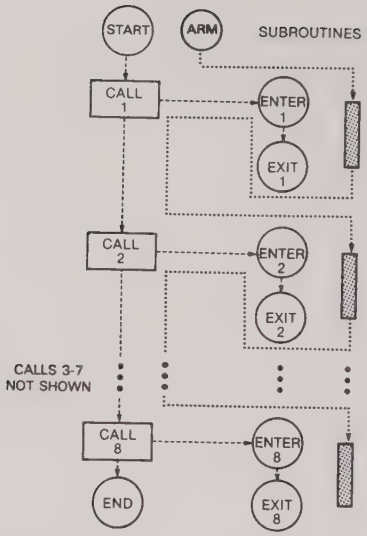
Figure 8-42. Capture Multiple Subroutines (Sheet 2 of 4).

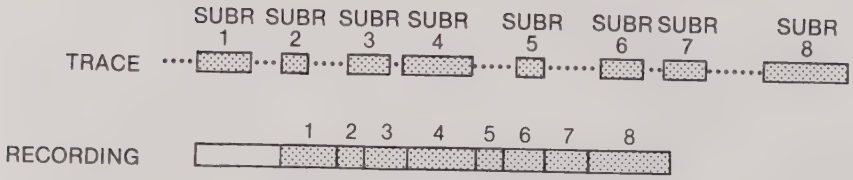
```
LEVEL 5 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                          Record
A=(Exit 3)                                     subroutine 3.
  TRACE ALWAYS
T=(Don't Care)


LEVEL 6 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                          Look for
A=(Call 4)                                     subroutine 4.
  TRACE NEVER
T=(Don't Care)


LEVEL 7 DELAY = DEC  515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE  IF DATA = A                         Record
A=(Exit 4)                                     subroutine 4.
  TRACE ALWAYS
T=(Don't Care)


LEVEL 8 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                          Look for
A=(Call 5)                                     subroutine 5.
  TRACE NEVER
T=(Don't Care)


LEVEL 9 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                          Record
A=(Exit 5)                                     subroutine 5.
  TRACE ALWAYS
T=(Don't Care)
```

Figure 8-42. Capture Multiple Subroutines (Sheet 3 of 4).

```
LEVEL A DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                    Look for
A=(Call 6)                               subroutine 6.
  TRACE NEVER
T=(Don't Care)

LEVEL B DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                    Record
A=(Exit 6)                               subroutine 6.
  TRACE ALWAYS
T=(Don't Care)


LEVEL C DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                    Look for
A=(Call 7)                               subroutine 7.
  TRACE NEVER
T=(Don't Care)


LEVEL D DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                    Record
A=(Exit 7)                               subroutine 7.
  TRACE ALWAYS
T=(Don't Care)

LEVEL E DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                    Look for
A=(Call 8)                               subroutine 8.
  TRACE NEVER
T=(Don't Care)


LEVEL F DELAY = DEC 515 CLOCKS

  STOP IF DATA = S                       Record
S=(Exit 8)                               subroutine 8
  JUMP TO 0 NEVER                        and stop.
J=(Don't Care)
  ADVANCE NEVER
A=(Don't Care)
  TRACE ALWAYS
T=(Don't Care)
```

Figure 8-42. Capture Multiple Subroutines (Sheet 4 of 4).





PURPOSE: To only record execution of the main program, don't record any of its subroutines.

BENEFIT: The entire main program's execution can be recorded without filling (or over filling) memory with each and every subroutine execution (just their call statements). Valuable memory space is not wasted by umpteen executions of numerous individual subroutines.

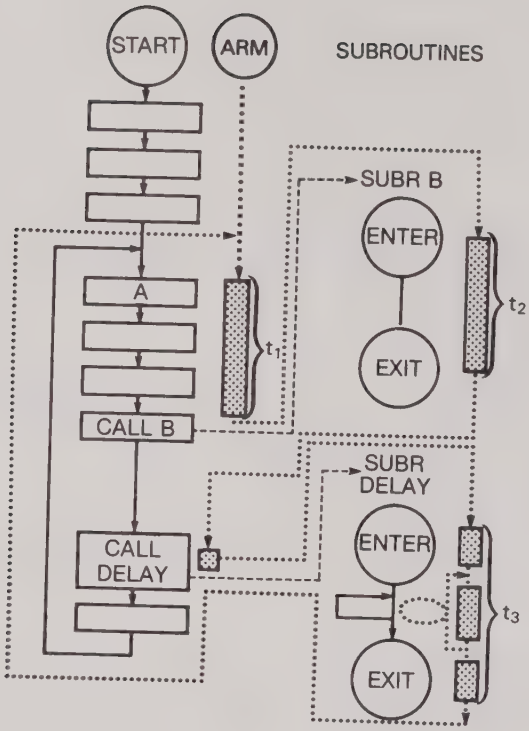
DESCRIPTION: The main program (which consists of 8 statements) calls 2 subroutines. The first subroutine calls 2 others; the second is a delay routine.

PROCEDURE: Start tracing at the beginning of the main program. When a subroutine is called, stop recording until control returns to the main program.

Figure 8-43. Record Main Program Only (Sheet 1 of 2).

```
SET UP:                                                    COMMENTS

LEVEL 0 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A
A=(Main 1)
  TRACE IF DATA = T                                        Start recording
T=(Main 1)                                                 main program.


LEVEL 1 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                                      Look for first
A=(Call A)                                                 subroutine call.
  TRACE ALWAYS
T=(Don't Care)


LEVEL 2 DELAY = DEC 515 CLOCKS
  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                                      Do not record
A=(Main 5)                                                 until control
  TRACE IF DATA  = T                                       returns to the
T=(Main 5)                                                 main program.


LEVEL 3 DELAY = DEC 515 CLOCKS
  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                                      Record main
A=(Call delay)                                             program until
  TRACE ALWAYS                                             delay routine
T=(Don't Care)                                             is called.

LEVEL 4 DELAY = DEC 515 CLOCKS
  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A
A=(Main 7)
  TRACE IF DATA = T                                        Do not record
T=(Main 7)                                                 until control
                                                           returns to the
                                                           main program.


LEVEL 5 DELAY = DEC 515 CLOCKS
  STOP NEVER
S=(Don't Care)
  JUMP TO 1 IF DATA = J                                    Follow the program's
J=(Main 8)                                                 jump and repeat
  ADVANCE NEVER                                            the recording
A=(Don't Care)                                             process.
  TRACE ALWAYS
T=(Don't Care)
```

Figure 8-43. Record Main Program Only (Sheet 2 of 2).



PURPOSE: To continuously monitor a program for a correct sequence of events and the execution time between them to check for unknown or intermittent errors.

BENEFIT: A potential error does not have to be known beforehand in order for it to be captured. Check points will window any error.

DESCRIPTION: Several check points in a program are monitored to make sure they happen in their correct sequence and within the correct time frame. The program and testing repeat as long as everything is OK but stops if any error occurs.

PROCEDURE: Check for A to occur then check that the time between A and call B is t_1 (=x clocks). Verify correct execution time t_2 (=y clocks) of subroutine B, and then of subroutine Delay (t_3=z clocks). If the sequence of events or timing is incorrect, stop tracing to see exactly what happened.

Figure 8-44. Check for Unknown Errors in Real Time (Sheet 1 of 3).

```
SET UP:                                                    COMMENTS

LEVEL 0 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A                                      Look for EVENT A.
A=(EVENT A)
  TRACE IF DATA = T
T=(EVENT A)


LEVEL 1 DELAY = DEC x CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 5 IF DATA = J AND SAMPLE COUNT > DELAY           Check time
J=(Call B)                                                 between A and
  ADVANCE IF DATA = A AND SAMPLE COUNT ≤ DELAY             Call B.
A=(Call B)
  TRACE ALWAYS
T=(Don't Care)


LEVEL 2 DELAY = DEC y CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 5 IF DATA = J AND SAMPLE COUNT > DELAY
J=(Call delay)
  ADVANCE IF DATA = J AND SAMPLE ≤ DELAY                   Check execution
A=(Call delay)                                             time of B.
  TRACE ALWAYS                                             (Call delay is
T=(Don't Care)                                             first statement
                                                           after returning
                                                           from B.)
```

Figure 8-44. Check for Unknown Errors in Real Time (Sheet 2 of 3).

```
LEVEL 3 DELAY = DEC z CLOCKS

  STOP NEVER
S=(Don't Care)
  JUMP TO 5 IF DATA = J AND SAMPLE COUNT > DELAY      Check execution
J=(Exit delay)                                        time of delay.
  ADVANCE IF DATA = J AND SAMPLE ≤ DELAY
A=(Exit Delay)
  TRACE ALWAYS
T=(Don't Care)


LEVEL 4 DELAY = DEC 515 CLOCKS

  STOP NEVER
S=(Don't Care)                                        Everything checked
  JUMP TO 0 ALWAYS                                    out OK; follow
J=(Don't Care)                                        program loop and
  ADVANCE NEVER                                       run test again.
A=(Don't Care)
  TRACE NEVER
T=(Don't Care)


LEVEL 5 DELAY = DEC 515 CLOCKS

  STOP ALWAYS
S=(Don't Care)                                        Something went
  JUMP TO 0 NEVER                                     wrong, stop.
J=(Don't Care)
  ADVANCE NEVER
A=(Don't Care)
  TRACE NEVER
T=(Don't Care)
```

Figure 8-44. Check for Unknown Errors in Real Time (Sheet 3 of 3).

PURPOSE: To trace a subroutine each time it occurs while simultaneously checking for EVENT 1 to occur followed by EVENT 2.

BENEFIT: A segment of interest can be continually traced while waiting for a sequence of events that could occur at unknown times.

DESCRIPTION: Every time subroutine S occurs, trace it. While looking for S to be called, simultaneously look for EVENT 1. If EVENT 2 happens only after EVENT 1, then the program is finished and tracing should stop. EVENT 1 and 2 can occur at any time, except during subroutine S.

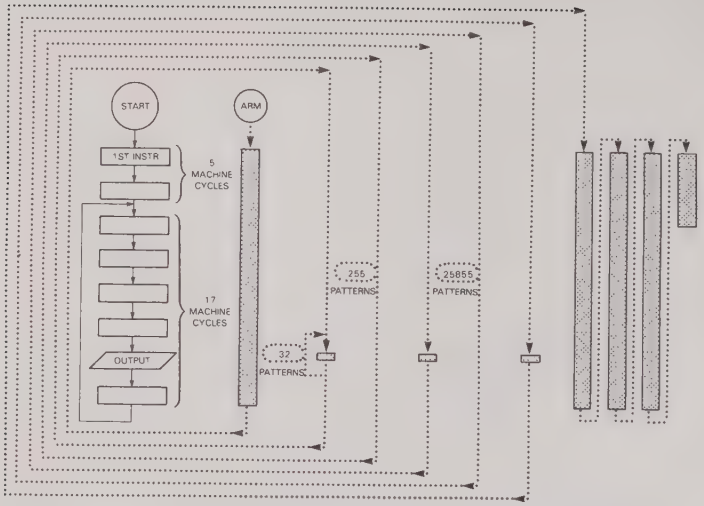
PROCEDURE: Simultaneously check for EVENT 1 and Call S. If S occurs, trace it and start looking for EVENT 1 and Call S again. After EVENT 1 occurs, simultaneously check for EVENT 2 and Call S. Trace 2 if it happens, then continue looking for EVENT 2 and Call S. Stop when EVENT 2 happens after EVENT 1 is found.

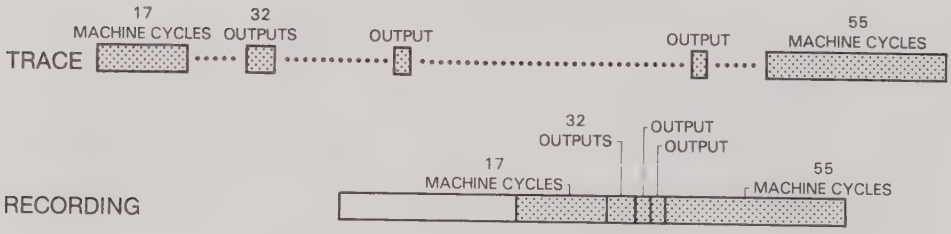
SET UP:

	COMMENTS
LEVEL 0 DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Don't Care)	
JUMP TO 2 IF DATA = J J=(EVENT 1)	Look for EVENT 1 and Call S.
ADVANCE IF DATA = A A=(Call S)	
TRACE IF DATA = T T=(Call S)	
LEVEL 1 DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Dont't care)	
JUMP TO 0 IF DATA = J J=(Exit S)	
ADVANCE NEVER A=(Don't Care)	
TRACE ALWAYS T=(Don't Care)	Trace S (neither EVENT 1 nor 2 has happened).
LEVEL 2 DELAY = DEC 515 CLOCKS	
STOP IF DATA = S S=(EVENT 2)	EVENT 1 has has happened. Look for EVENT 2 and Call S. Stop when EVENT 2 is found.
JUMP TO 0 NEVER J=(Don't Care)	
ADVANCE IF DATA = A A=(Call S)	
TRACE IF DATA = T T=(Call S)	
LEVEL 3 DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Don't Care)	
JUMP TO 2 IF DATA = J J=(Exit S)	
ADVANCE NEVER A=(Don't Care)	
TRACE ALWAYS T=(Don't Care)	Trace S (EVENT 1 has happened but EVENT 2 has not.

Notes: Uses building blocks of Figures 7.2-10, 7.2-11, and 7.2-12.

Figure 8-45. Record and Check for Correct Execution.





PURPOSE: To record multiple, non-continuous program segments during a single recording and verify correct operation over a multitude of program executions.

BENEFIT: A single recording captures segments of program execution widely separated in time and will only record correctly if the program is operating correctly.

DESCRIPTION: A short loop program adds 3 to a register and outputs the register value to a port each time the loop is executed. Port values range from CC to FF so program repeats the same port value every 256 cycles as a major loop.

Figure 8-46. Isolate Program Execution Essentials (Sheet 1 of 3).

PROCEDURE: The first level merely waits for the initial program instruction (FIRST INSTR.), traces it, and advances to level 1. At level 1, the next 21 machine cycles are captured so that the entire execution of the first loop pass is recorded and then the unit advances again. At level 2, only the actual port accesses (OUTPUT PORT) are recorded for the next 32 passes (1 word out of 17, captured 32 times). Continuing at level 3, the analyzer is programmed to ignore all execution until the 255th occurrence of output port which should be a complete major loop of over 4000 machine cycles with only the final port value being stored. If, and only if, the loop properly executes all the code between, then the sample traced at level 3 should have the same data value as the last loop traced in level 2. The unit is then programmed to advance to level 4, where the same type of data exclusion is used, only instead of using one major loop, a hundred and one major loops (256 x 101 255 = 25,855 patterns) are checked. The program must properly execute over 400,000 machine cycles and then the port data should be the same as in the preceding two samples. Finally, the trace control is advanced to level 5, where the next 55 samples of each machine cycle are captured, and the recording is stopped.

SET UP:	COMMENTS
LEVEL 0 DELAY = DEC 515 CLOCKS	
STOP NEVER S=(Don't Care)	
JUMP TO 0 NEVER J=(Don't Care)	
ADVANCE IF DATA = A A=(1st. Instr.)	
TRACE IF DATA = T T=(1st. Instr.)	Start recording at the first program.
LEVEL 1 DELAY = DEC 21 CLOCKS	
STOP NEVER S=(Don't Care)	
JUMP TO 0 NEVER J=(Don't Care)	
ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY A=(Don't Care)	Record first pass of the program loop.
TRACE ALWAYS T=(Don't Care)	
LEVEL 2 DELAY = DEC 32 A PATTERNS	
STOP NEVER S=(Don't Care)	
JUMP TO 0 NEVER J=(Don't Care)	
ADVANCE IF DATA = A A=(OUTPUT PORT)	Only port accesses are traced for the next 32 passes.
TRACE IF DATA = T T=(OUTPUT PORT)	

Figure 8-46. Isolate Program Execution Essentials (Sheet 2 of 3).

```
LEVEL 3 DELAY = DEC 255 A PATTERNS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A=(OUTPUT PORT)
  TRACE IF DATA = A AND SAMPLE COUNT = DELAY
T=(OUTPUT PORT)
```

After 1 major loop record only the value being output to the port. (It should be the same as the last value in trace level 2.)

```
LEVEL 4 DELAY = DEC 25855 A PATTERNS

  STOP NEVER
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A=(OUTPUT PORT)
  TRACE IF DATA = A AND SAMPLE COUNT = DELAY
T=(OUTPUT PORT)
```

Wait 101 major loops before recording output values. (Value should still be the same as in level 3.)

```
LEVEL 5 DELAY = DEC 55 CLOCKS

  STOP IF DATA = S AND SAMPLE COUNT = DELAY
S=(Don't Care)
  JUMP TO 0 NEVER
J=(Don't Care)
  ADVANCE NEVER
A=(Don't Care)
  TRACE ALWAYS
T=(Don't Care)
```

All of the next 55 cycles are recorded and tracing stopped.

Figure 8-46. Isolate Program Execution Essentials (Sheet 3 of 3).

Section 9

COMMUNICATIONS

9.1 OVERVIEW

Communication links can be set up between the K101-D and other devices. This section describes two user-programmable communication interfaces, the IEEE STD 488-1978 and the EIA-RS-232-C. The IEEE STD 488-1978 is an eight-bit, parallel interface, commonly referred to as the General Purpose Interface Bus (GPIB). The EIA-RS-232-C (RS-232) is an asynchronous bit serial interface that involves the use of modems for telephone line links or direct connection to printers, terminals or other peripherals.

Operation of the two interfaces is described in paragraph 9.2. Additional technical descriptions of the two interfaces are contained in paragraphs 9.5 (GPIB) and 9.6 (RS-232).

The basic procedure to establish a communication link is straightforward:

a. Connect either the GPIB cable or the RS-232 cable to the proper connection on the rear panel of the K101-D.

b. Set up matching link parameters on the K101-D and the device at the other end of the communication link.

c. Initiate communication as described in paragraph 9.2.

9.2 OPERATION

9.2.1 GPIB INTERFACE OPERATION

a. Connect the GPIB connector (IEEE 488) on the rear panel of the K101-D to a GPIB controller or peripheral.

b. Press INTERFACE to display the interface setup menu.

As shown in Figure 9-1, the setup menu is divided into two sections. The left side is for the GPIB interface. Three parameters need to be programmed: interface mode, termination character, and command field.

9.2.1.1 Interface Mode

The first field in the GPIB interface section is used for selection of one of three interface modes: Talk and Listen, Talk Only, or Listen Only (the default mode -- so you can remotely send a command to the K101-D giving it an address and changing to Talk and Listen mode).

a. **Talk and Listen Mode.** In this mode, the K101-D will accept information from, or transfer information to, a controller. Talk and Listen mode is used in most applications. For example, it is best suited to control the instrument from a controller. To use Talk and Listen mode, assign to the instrument an address between 0 and 30 (in decimal) to the instrument. Press CHOICE NEXT until ADDRESS = nn (nn = 0 to 30) is selected at the blinking cursor. Enter a number between 0 and 30 from the keyboard, e.g., 14 by pressing Hx3 1 H and PAGE 4 K . The instrument can now be addressed by a

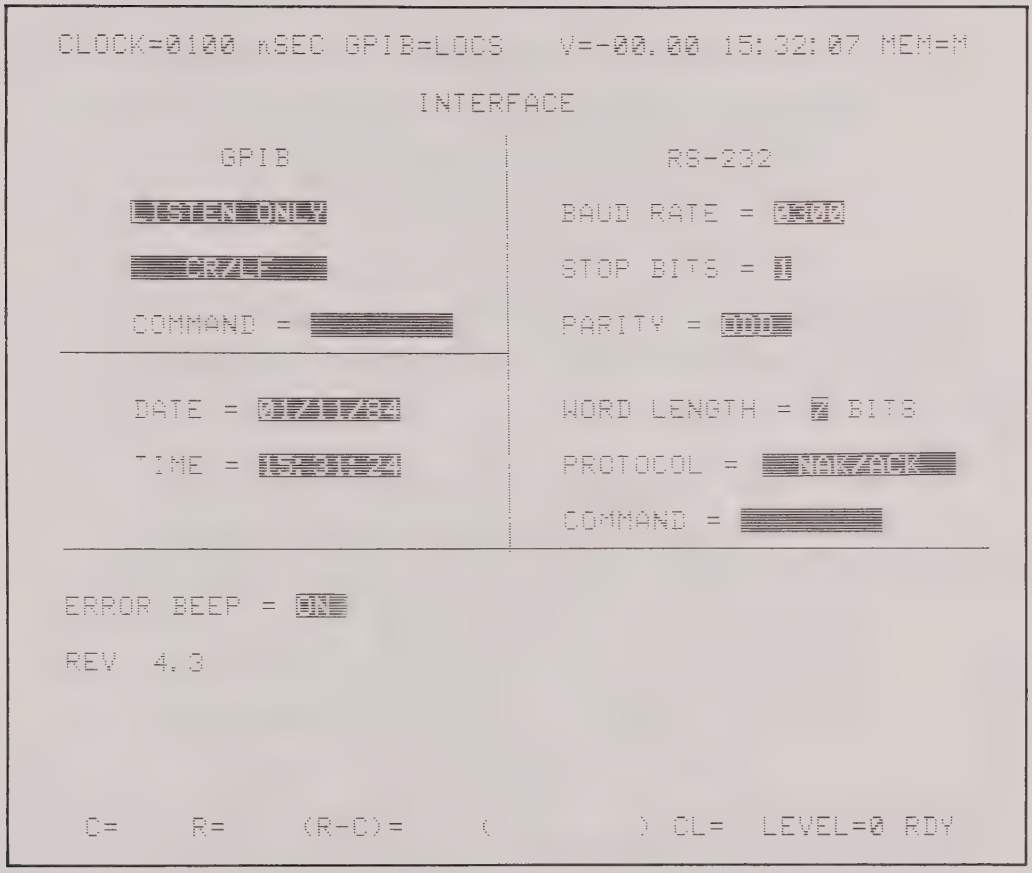


Figure 9-1. GPIB Interface Setup Menu.

controller as location 14. The K101-D will process records sent on the GPIB when commanded to listen. For example, the instrument will listen to controller commands to address 14 such as move a cursor on the screen, select setup menus, perform timing analysis, and arm the instrument.

The K101-D can be commanded to talk as address 14. In this case, the instrument will process records and send the necessary information back to the controller.

Note

Users should be careful when talk commands are used because the GPIB, and hence the instrument, can lock up. The three most common problems are

a. The instrument is commanded to talk but has not been commanded to send data. Therefore it will wait for further instructions from the controller.

b. All requested data has been transferred by the instrument.

c. The instrument did not understand the command.

b. **Talk Only mode.** The foremost application of Talk Only mode is to transfer information from the screen to a dedicated GPIB printer. Producing hard copy with Talk Only mode is straightforward. For example, display the desired setup screen and press

. The screen will be printed as displayed.

Display data with DATA and A, and again press SERVICE.

The data will be printed as shown on the screen.

Note

The printer should be set to Listen Only mode.

Talk Only mode can also be used to transfer the contents of memory A or B to another K101-D. The Command field is used to enter the command to transfer the contents of memory A or the contents of B (CMA or CMB, respectively). Press SHIFT and DON'T CARE * SPACE to initiate data transmission. The records entered in the command field must conform to the specified formats (see paragraph 9.2.1.3).

Note

GPIB listener capability is not available in Talk Only mode.

c. **Listen Only mode.** Like Talk Only mode, the Listen Only mode has limited use; for example, it is used to receive information from another K101-D. GPIB talking capabilities are not available in this mode. The default condition for the K101-D is Listen Only mode. This mode permits users to change the K101-D mode. For example, the user can change the instrument

to the Talk and Listen mode or assign a new address by sending keystroke records. While in Listen Only mode, the instrument will not transmit information to another device as GPIB Talking capabilities are not available in this mode. The instrument will, however, process all messages received over the GPIB.

9.2.1.2 **Termination Characters**

The K101-D can be configured to accept any one of four termination characters or character strings. This gives the K101-D the flexibility to adapt to any controller. For example, some controllers must receive carriage return only. Others may require both carriage return and line feed to terminate a record. The four termination strings are as follows:

a. CR and LF
b. CR/LF + EOI
c. CR
d. CR + EOI

where:

CR = carriage return
LF = line feed
EOI = end of information

To program the instrument proceed as follows:

a. Press

to display the Interface setup menu.

b. Press

to move the cursor to the termination character field.

c. Press CHOICE NEXT to select a character string which matches with the termination character required by the controller on the other side of the GPIB interface.

9.2.1.3 Command Field

The command field is used only in conjunction with Talk Only mode and is not usable in the other two modes. The command field is provided to enter records from the keyboard in Talk Only mode.

a. Display the Interface setup menu with INTERFACE .

b. Select Talk Only mode with CHOICE NEXT .

c. Press ◁▷ SET two times to move the cursor to the Command field.

d. Change the mode from Talk Only to Listen Only or Talk and Listen.

e. Move the cursor downward with ◁▷ SET.

Note

The cursor bypasses the command field, which indicates that the field is not usable with Talk and Listen or Listen Only mode.

The record entered in the command field must conform to specified formats. The keys entered in the command field are processed as if they came over the GPIB from an external controller. The field can contain a maximum of eight characters. If more than eight characters are entered, the first entered character will be deleted, then the next, and so on.

Enter a space character, i.e., press **SHIFT** and **SPACE**, to process all records. The space character is interpreted as a "carriage return" terminator. Enter a new record and the previous record will be automatically deleted by the instrument. Use **DELETE** to delete the last entered character. Continue pressing **DELETE** and the subsequent characters will be deleted in turn.

9.2.1.4 **Saving Interface Setup Menus**

The K101-D will automatically save the most recently selected interface parameters, the user need not select them every time power is turned on. The **SHIFT** and **RECALL** keys do not restore the interface parameters to default. It does not matter if the keys were pressed at the keyboard or the keycodes came over the GPIB. (The K101-D will, however, change the Interface setup menu to default conditions if a CMOS memory error is detected during power up diagnosis.)

9.2.2 RS-232-C INTERFACE OPERATION

Connect the RS-232-C connector on the rear panel of the K101-D to a modem or other device.

Press

to display the Interface menu.

As shown in Figure 9-2, the right side of the setup menu is for RS-232-C. Select the six parameters as described below to configure the K101-D:

a. Baud rate
b. Stop bits
c. Parity
d. Word length
e. Protocol
f. Command

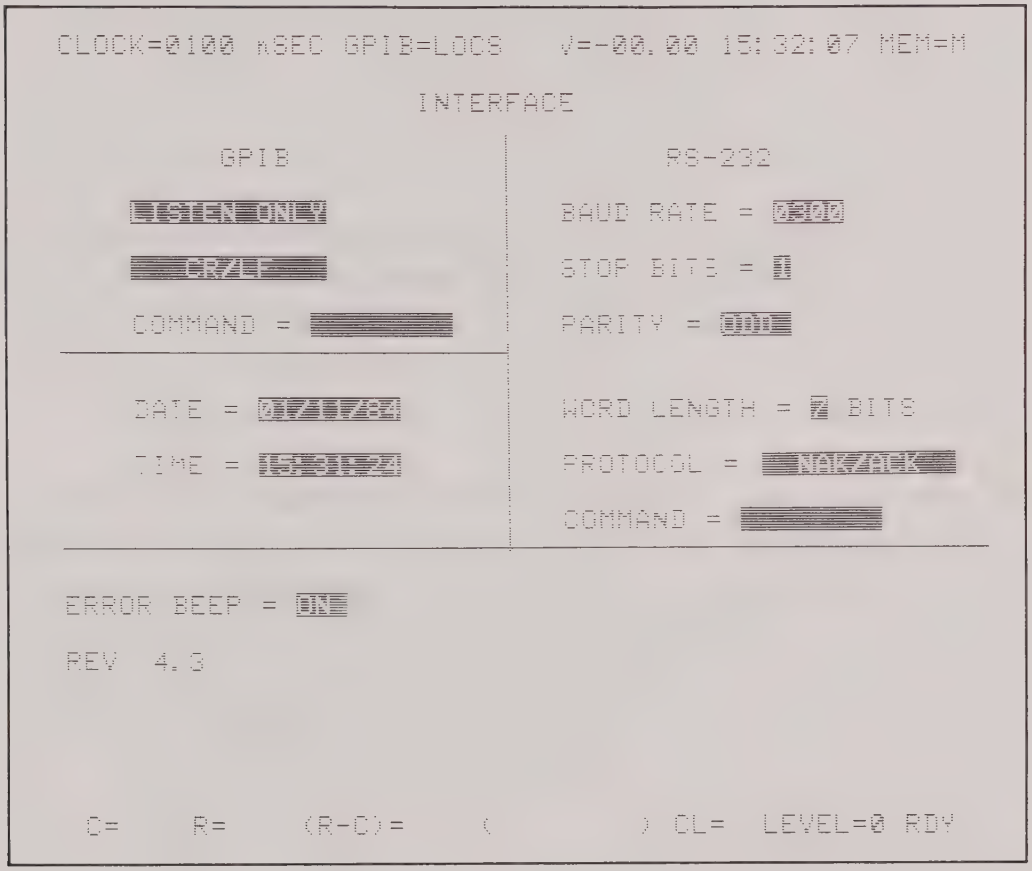


Figure 9-2. RS-232-C Interface Setup Menu.

9.2.2.1 **Baud Rate**

Select the K101-D communication speed to match the speed of the device at the other end; the communication speed must be the same. Use the FIELD keys to select the baud rate. The available values are 110, 150, 300, 600, 1200, 1800, 2400, 4800, and 9600 bps. [Default Value = 300 BPS]

9.2.2.2 **Stop Bit**

The stop bit can be one bit or two bits; its value should match the other device. If you do not know the stop bit for the other device, select one bit for the K101-D. [Default = one bit]

9.2.2.3 **Parity**

The K101-D transmits and checks parity of odd, even, or none. Check the parity of the other device and set the K101-D accordingly. Alternately, you can change another device's parity to match the K101-D selected parity. If your terminal receives square blocks, or some characters are not identifiable, the probable cause is wrong parity. Change parity and try again. If you are not sure about the parity of the other device, start with none parity for the K101-D. [Default = odd]

9.2.2.4 **Word Length**

Word length can be seven or eight bits. Start with eight bits. [Default = seven bits]

9.2.2.5 **Protocol**

Most computers and computer peripherals recognize XON/XOFF (CTRLQ/CTRLS). Select CTS/RTS. The K101-D will then send XON/XOFF as well as accept XON/XOFF from another device. The ACK/NAK and CTS/RTS

have some limitations for the software versions 4.0 and 4.2 (see paragraph 9.3.2.1). [Default = ACK/NAK]

9.2.2.6 **Command**

The command field is provided to transmit the contents of memory A or B, or setup screens to a printer or to another K101-D. The field is a maximum of eight characters wide. The **DELETE** key could be used to delete the most recently entered character. Enter CMA or CMB to transfer contents of memory A or B, respectively. Any other command record can also be entered in the command field to perform corresponding activity. Press **SHIFT** and **DON'T CARE** to initiate communication. The records entered in the command field must conform to the specified formats. They are processed by the instrument as if they were received via the RS-232 interface from an external controller.

9.2.2.7 **Saving RS-232-C Interface Setup Menu**

The RS-232-C Interface menu can be saved either by keyboard entry or transmitted code (see paragraph 9.2.1.4 for details).

9.3 **CODES AND COMMANDS**

9.3.1 DESCRIPTION

Records are provided to allow the K101-D to interact with other devices. Each record is a predefined string of characters which has a specific format and predefined purpose. The same records are used for both the GPIB and RS-232-C interface. Five types of records (keystroke, command, memory modification, message display, and status) can be used with the K101-D. Their formats are summarized in Figure 9-3.

All these records are terminated by the same termination character. Each record is discussed below.

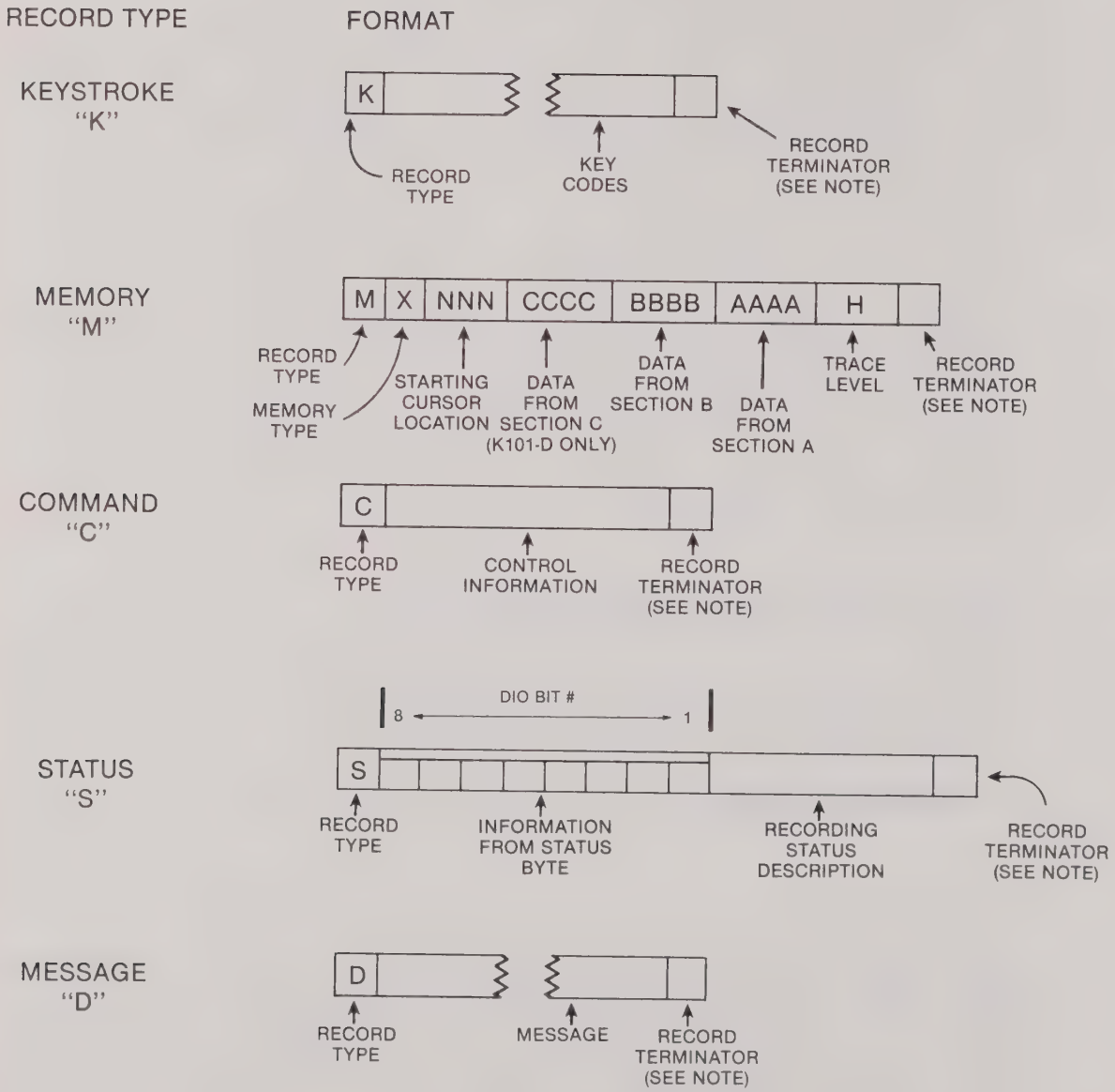


Figure 9-3. The K101-D Records.

Record types D, C, K, and M may be sent to the K101-D when it is a listener. Record types K, M, and S may be sent by the K101-D when it is a talker.

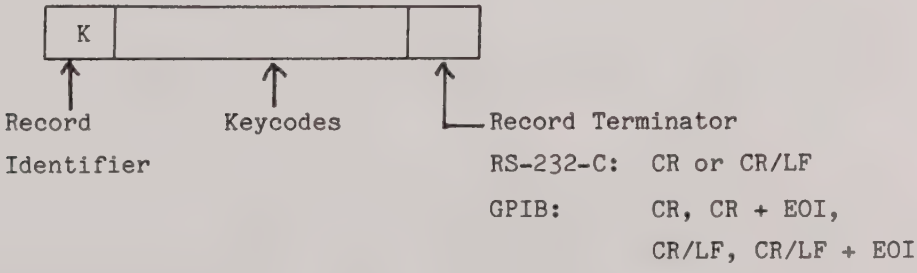
Note

The record terminator may be either a two-ASCII-character "carriage return" (hex OD)/ "line feed" (hex OA) combination or a single-ASCII "carriage return." Either form will be accepted by the K101-D when it is a listener. The form used by the K101-D when it is a talker can be selected by the GPIB controller. See the explanation of the CR and LF commands under the descrip-

9.3.2 KEYSTROKE RECORD

The five keystroke records are used to reconfigure the six setup menus and perform DISPLAY key functions. The keystroke records are equivalent to the user pressing the keyboard keys. For example, with a keystroke record, the user can select the Clock setup menu, change it, arm the instrument, and display data. The keystroke record can be used for editing.

The record has the following format:



All keystroke records start with an ASCII K (capital K) followed by the keycodes which are the ASCII letters as defined in Table 9-1. The record is terminated by a carriage return or carriage return and line feed when using RS-232-C. For the GPIB, the termination string could be CR, CR + EOI, CR/LF, or CR/LF + EOI.

Several keycodes can be grouped together to form one record. In a group, however, only one identifier is required. For example, send **K $C %] 100 CR.** The **K** informs the K101-D that it is a keystroke record. The **$C** displays Clock setup menu. The **%** activates the **NEXT** key, i.e., advances mode selection one step. For example, if Internal mode was selected before sending the record, the **%** will advance it to external single-phase. The **]** moves the cursor one step down. The **100** sets the current cursor location, i.e., internal clock speed, to 100. Finally, **CR** terminates the record.

Note

Spaces may be entered anywhere in the record to enhance legibility. The K101-D will ignore the space characters.

In software versions 4.0 and 4.1, the K101-D will process the record before receiving the termination character. The users, however, must send the termination character to terminate the record. Otherwise, the K101-D will wait for a termination character, and any new record sent by the user will be interpreted as an illegal command even if it is a legal record. Any time you are in the middle of a record and want to start again, press the **ENTER (RETURN)** key to terminate the record.

Note

In software versions 4.0 and 4.2, the users should avoid overflowing the K101-D buffer. The K101-D may be busy executing keystroke records and may not interrupt the communi-

Table 9-1. Keycode Selection Table
(Keystroke Record Only)

Description of Key on the Keyboard	Keycode	Description of Key on the Keyboard	Keycode
0	0	**SPECIFY Keys**	
1	1	Interface	$Z
2	2	Clock Select	$C
3	3	Input Mode	$I
4	4	Trace Control	$S
5	5	Logic Polarity	$P
6	6	Data Format	F
7	7		
8	8	**FIELD Keys**	
9	9	Cursor left	<
A	A	Cursor right	>
B	B	Cursor up	(
C	C	Cursor down	)
D	D	Next	%
E	E	Previous	#
F	F		
G (shift 0)	G	**DISPLAY Keys**	
H (shift 1)	H	Select A	!3
I (shift 2)	I	Select B	!4
J (shift 3)	J	Compare A/B	!6
K (shift 4)	K	Search On/Off	!7
L (shift 5)	L	Graph	$G
M (shift 6)	M	A - B	!1
N (shift 7)	N	Data	$D
O (shift 8)	O	Timing	$T
P (shift 9)	P		
Q (shift A)	Q	**ACQUIRE Keys**	
R (shift B)	R	Arm	!8
S (shift C)	S	Advance	!5
T (shift D)	T	M - A	!2
U (shift E)	U	Stop	!0
V (shift F)	V		
W (shift <)	W	**ACTION Keys**	
X (shift =)	X	Edit	/0
Y (shift >)	Y	Insert	/1
Z (shift .)	Z	Delete	/2
		Save	/3
*	*	Recall	/4
-	-		
		VIRTUAL Keys	
Period	&.	Blank Display	.0
Less than	&<	Set Cursor	/6
Greater than	&>	Set Reference	/7
Equal to	&=	Shift Recall	/5
Space	$;	Shift Delete	/8

cation once the buffer is filled. The number of keystroke records which can be sent in a group to the K101-D will depend upon the type of records.

9.3.2.1 QUICK Keys and DIRECT Keys

The **NEXT** and **PREV** keys help select the desired value of a parameter in the setup menus (see Table 9-2). In some cases, this requires pressing the keys several times to select a specific value.

Example

Select mixed multiphase inputs with **NEXT** key.

SET UP: a. Press CLOCK SELECT to display Clock setup menu.

b. Press CHOICE NEXT four times to select mixed multiphase inputs.

RESULT: User presses CHOICE NEXT four times to select the desired inputs.

End Example

The QUICK keys are provided to select a specific function in which the user presses only one key instead of repeatedly pressing the **NEXT** or **PREV** key. The QUICK keys are identified by numeric keys, i.e., keys **0** through **9** (see Section 4).

Table 9-2. DIRECT Keys and QUICK Keys (Keystroke Record Only)

Interface Setup Menu	Keycode
GPIB INTERFACE	
Interface Mode	
Address	0 thru 30 (direct keys)
Talk Only	B
Listen Only	C
Termination Characters	
CR	0
CR or EOI	1
CR·LF	2
CR·LF or EOI	3
Error Beep	
Off	0
On	1
RS-232-C INTERFACE	
Baud Rate (bps)	
110	0
150	1
300	2
600	3
1200	4
1800	5
2400	6
4800	7
9600	8
Stop Bits	
1 bit	0
2 bits	1
Word Length	
7 bits	0
8 bits	1
Protocol	
XONXOFF	0
RTS/CTS	1

Clock Select Setup Menu	Keycode
Clock Mode	
Internal	0
External Single-Phase	1
External Multiphase	2
External Mixed Single-Phase	3
External Mixed Multiphase	4
Internal Extended	5
Internal Clock Period	
milliseconds	0
microseconds	1
nanoseconds	2
Clocks	
xy (x = A, B, C) (y = J, K, R, S)	0
xy as above	1
xy as above	2
Sample Clocks	
Int	0
Ext	1
10 ns	2

Input Setup Menu	Keycode
Mode	
Sample	C
Glitch	D
Latch	E
Demux	F
Threshold	
TTL	8
ECL	9
VAR A	A
VAR B	B

Table 9-2. DIRECT Keys and QUICK Keys (Keystroke Record Only) (Cont'd)

Input Setup Menu (Cont'd)	Keycode
Arm Mode	
Manual	0
Auto	1
Auto Stop if A = B	2
Auto Stop if A ≠ B	3
Auto Stop if A = B within limits	4
Auto Stop if A ≠ B within limits	5

Trace Control Setup Menu	Keycode
Delay	
DEC	D
HEX	F
Clocks	0
A Pattern	1
Command Conditions (see note)	
If data = D	0
Always	1
Never	2
If data = D and sample count => Delay	3
If data = D and sample count =< Delay	4

Trace Control Setup Menu	Keycode
Command Conditions (Cont'd)	
If data = D and sample count = delay	5
If data = D and sample count >= delay	6
If data = D and sample count <= delay	7
If data = D and sample count <> delay	8

Logic Polarity Setup Menu	Keycode
True	+
False	-

Data Format Setup Menu	Keycode
Hex	0
Octal	1
Binary	2
Mixed user sequence	3
Mixed CF-A0 sequence	4
Device mnemonics	5

Note: D = S, J, A, or T as determined by command type.

Note

In the following examples, CR means that the user terminates the record by pressing **RETURN/ENTER** key.

Example

Select mixed multiphase inputs with QUICK keys

SET UP: a. Press CLOCK SELECT to display Clock setup menu.

b. Press PAGE 4 K to enter 4. mixed multiphase inputs are selected.

RESULTS: User presses a single key to select the desired inputs.

End Example

Like QUICK keys, the DIRECT keys also select the specific functions. The DIRECT keys can be identified by functions labelled on the keys, e.g., the **SAMPLE** key.

Example

Demux inputs BF-B8 and B7-B0 with **NEXT** key.

SET UP: a. Press CLOCK SELECT to display Input setup menu.

b. For K101-D: move cursor to BF-B8 with ▽ SET.

Then press **NEXT** three times to Demux BF-B8 and B7-B0.

RESULT: User presses **NEXT** three times to select the desired input mode.

With DIRECT keys, user does not repeat entries.

End Example

Example

Demux inputs CF-C8 and C7-C0 with DIRECT keys.

SET UP: a. Press CLOCK SELECT to display Input setup menu.

b. Press DEMUX F HEX. The CF-C8 and C7-C0 inputs are now in Demux mode.

RESULT: User presses one key to select the desired input mode.

End Example

The DIRECT and QUICK keys can be transmitted over the GPIB or the RS-232-C interface. These keys select a specific function and the user or a controller need not know the current state of the setup menus. If the DIRECT and QUICK keys are not available, a user or controller has to receive the current setup menu to check it. In such a case, the user moves the cursor to the desired field by transmitting the code for the arrow keys. Finally, the **NEXT** or **PREV** key is sent repeatedly in many situations to select the specific function. With DIRECT and QUICK keys, the user sends one keystroke record to the same parameter.

Example

Current state unknown. Select mixed multiphase inputs with **NEXT** key.

SET UP:

a. Display Clock setup menu on the K101-D screen: send K $C CR (CR = return key).

b. Bring Clock setup menu to your terminal: send CPS CR.

c. Check the Clock setup menu for the current state (say, Internal mode).

d. Change Internal mode to mixed multiphase: press the **NEXT** key four times. Send K%%%%CR.

e. Bring the Clock setup menu to confirm the changes: send CPS CR. Review and ensure that mixed multiphase mode has been selected.

RESULT: Five steps are required to select and confirm the mixed multiphase inputs.

End Example

With QUICK keys the above process will take only two steps as shown below.

Example

Current state unknown. Select mixed multiphase inputs with QUICK keys.

SET UP: a. Select mixed multiphase mode. Send K $C 4 CR.

b. Bring the Clock setup menu to your terminal and confirm the selection: send CPS CR. Review and ensure that mixed multiphase inputs have been selected.

RESULT: Two steps are needed to select and confirm the mixed multiphase inputs.

End Example

Like QUICK keys, DIRECT keys also reduce steps to select a specific parameter.

Example

Current state unknown. Demux inputs AF-A8 and A7-A0 with **NEXT** key.

SET UP: a. Display Input Mode menu on the K101-D screen: send K $I CR.

b. Bring Input Mode menu to your terminal to find the current state: send CPS CR.

c. Change current state to Demux AF-A8.

d. Assume that AF-A8 are set to Sample mode.

e. Move the cursor four steps down, press the **NEXT** key three times to Demux AF-A8 inputs: send K))))%%%CR.

f. Bring Input setup menu to confirm the change: send CPS CR. Review and ensure that AF-A8 and A7-A0 inputs have been set to Demux.

RESULT: Five steps are required to change AF-A8 and A7-A0 inputs to Demux from Sample mode.

End Example

With DIRECT keys, the above selection requires only two steps (see example below).

Example

Current state known. Demux inputs AF-A8 and A7-A0 with DIRECT keys.

SET UP: Display and demux AF-A8 inputs. Move cursor four steps down to select AF-A8 inputs. Send K$I))))FCR.

End Example

9.3.2.2 **Keycode Error**

The K101-D may receive records with illegal keycodes. In that case, the instrument will cause a service request for GPIB or transmit a NAK (15 hex) character on the RS-232-C interface. A GPIB controller can be programmed to interrupt and display any message whenever a service is requested by the instrument. In case of RS-232-C, NAK is not a displayable character. A CRT terminal that can display control characters should be able to display NAK on its screen. Also, an application program can retrieve NAK character from the instrument buffer.

9.3.3 COMMAND RECORDS

The command records transmit information from the K101-D to another instrument, peripheral, or computer. For example, command records are used to transmit contents of memory A or B or setup screens to an external memory. The command record is also used to interrogate the K101-D status. All command records are summarized in Table 9-3. The command records format is shown in Figure 9-4a.

The record identifier is an ASCII C, followed by control information, and a termination character. The command records, like keystroke records, cannot be grouped. All command records, and the actions initiated by them, are described in detail in the following paragraphs.

9.3.3.1 **Memory Transfer: CMA, CMB**

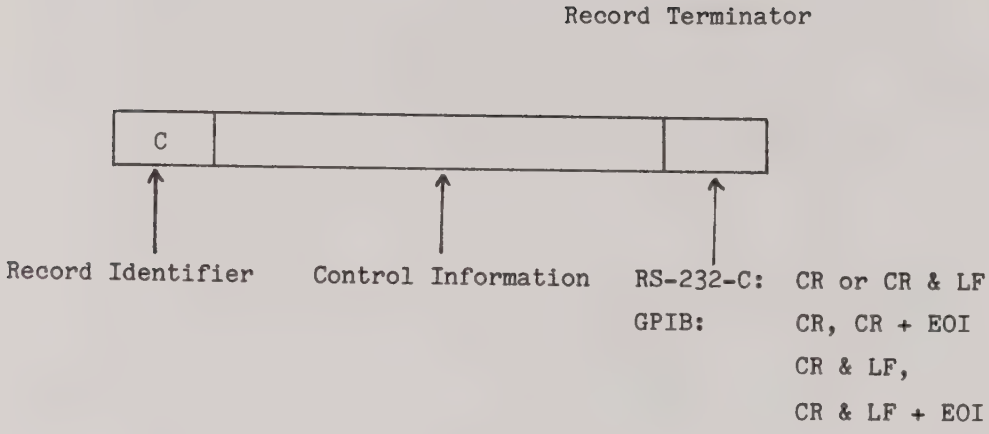
In several situations, the user may need to review, analyze, or edit the information in memory A or B. The memory transfer records CMA and CMB (Figure 9-4b) transfer the contents of memories A and B respectively, to an external storage device, a computer, or to a computer terminal. Thus, information can be reviewed by the user. The data between cursor locations C and R will only be transmitted by the K101-D. In case C is greater than R, the data between C and the memory location 514 will be

transferred. The data are transmitted in 70-character blocks, which have the format shown in Figure 9-4b. The K101-D inserts CR/LF at the end of each block for the RS-232-C interface. For the GPIB, the termination character is the same as that selected in the Interface setup menu.

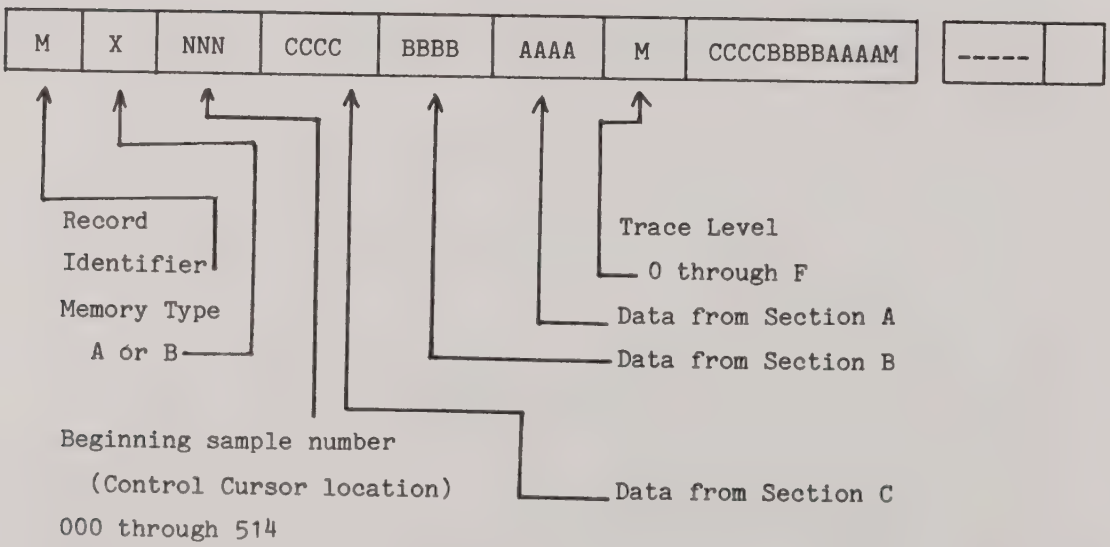
As shown in Figure 9-4b, a sample is represented by 13, ASCII-encoded hex characters for the K101-D. Characters 1 through 4 represent section C; 5 through 8, section B; and 9 through 12, section A. The thirteenth character indicates trace level. In case of the K102-D, section C is not displayed, and nine characters represent a sample. The K101-D

Table 9-3. Summary of K101-D Command Records

Acquisition Parameters	
Send memory A, B within C and R cursor locations:	CMA, CMB
Send device status:	CSR
Sent time, date, and trace time of recording in A, B:	CTA, CTB
Send voltmeter reading:	CVM
Send current displayed image in ASCII (limited):	CPS
Setup Information	
Send keystrokes to setup Interface screen:	CZM
Clock select screen A, B, M:	CCA, CCB, CCM
Input mode screen A, B, M:	CIA, CIB, CIM
Trace control screen A, B, M:	CSA, CSB, CSM
Logic polarity screen A, B, M:	CPA, CPB, CPM
Data format screen:	CFM
Cursors C and R positions:	CCU



a. The Command Record Format.



b. The Memory Transfer Record Format.

Figure 9-4. Record Formats.

transmits five samples in a block of data appearing as one line on a computer terminal. The maximum block length is 70 characters.

The K101-D always transmits all samples between the Control and Reference Cursors on all 48 inputs. It transmits zeros for the unselected inputs. For example, plug probe AF through A8 in the PROBE TEST connector, set AF through A8 clock inputs to ECL, select AF through A8 in the data format, arm the instrument by pressing **ARM**, and display data by pressing the **DATA** key. On the instrument screen, the memory contents of channels AF through A8 are displayed. When sending CMA from a terminal, the K101-D transmits lines, each 70 characters wide. The data for sections C, B, and A0 through A7 are all zeros in all the samples (as indicated by characters 1 through 8, 11, and 12). The ninth and tenth characters display data from inputs AF through A8.

9.3.3.2 **Device Status: CSR**

For controllers with no serial poll capabilities, and for the RS-232-C interface, an ASCII code representative of the serial poll status byte and record status is implemented. Sending the command CSR has the same effect (i.e., clearing certain bits in the device status byte) as performing a serial poll. Upon receiving CSR, the K101-D sends its status as a character string. The string is encoded in ASCII and defined as a status record (see paragraph 9.3.6).

Example

Receive the K101-D current status.

SEND: CSR

RECEIVE: S01000000,0 RDY

End Example

9.3.3.3 **Acquisition Time: CTA, CTB**

The time, date, and total trace time of each recording are stored along with the recording, and can be reviewed by sending the CTA or CTB command to the K101-D.

Example

Receive date and time of the last tracing
in memory A (Talk record only).

SEND: CTA

RECEIVE: TA09:03:4208/27/8210.0uS

Variable length string

End Example

The first character of an acquisition time record is a T, the record type. All characters in this record are ASCII. The next character indicates which memory the data represent, either A or B. The next eight characters indicate the time at which the acquisition was taken (normally formatted HH:MM:SS). The next eight characters indicate the date (MM/DD/YY). The last ten characters indicate the trace time.

9.3.3.4 **Voltmeter Reading CVM**

The K101-D has a built-in, real-time voltmeter which can be read by sending a CVM command.

Example

Receive current voltmeter reading from
the K101-D (talk record only).

SEND: CVM

RECEIVE: V-00.01 The current voltmeter reading is 0.01 V

Length of string is nine characters, including the CR/LF terminator

End Example

9.3.3.5 **Transmit Screen CPS**

The CPS command allows the user to obtain a hard copy of the current screen display. This command will have limited value in some situations because certain K101-D display characters have no equivalent ASCII code (e.g., timing diagrams).

Example

Receive clock select setup currently displayed on the screen.

```
SEND:     CPS

RECEIVE:  Clock = 0020 nsec GPIB = REMD V = 00.01 09:0956 MEM = M

                        CLOCK SELECT
                      MODE = INTERNAL
              INTERNAL CLOCK PERIOD = 0020 NANOSECONDS
            MASTER CLOCK = INTERNAL
            SAMPLE CLOCK

                C = INT 0020 NANOSECONDS
                B = INT 0020 NANOSECONDS
                A = INT 0020 NANOSECONDS

            ENABLE -- (used only in Latch and Demux)

                C = EXT ( __ X___X___)+(____+____+____)
                B = EXT ( __ X___X___)+(____+____+____)
                A = EXT ( __ X___X___)+(____+____+____)
                C = R = (R-C) = (     ) CL = LEVEL RDY
```

End Example

The K101-D will send one record for each row of characters displayed on the screen.

9.3.3.6 **Save Setup Information in External Memory**

The K101-D can be shared by several users. Since each user probably selects a different setup configuration, the instrument may often require reconfiguration. This process requires considerable time. The K101-D converts all setup screens into keystroke records and transmits them to an external memory, e.g., to a computer file. The transmitted information is actually several keycodes grouped together to form a keystroke record.

The examples given below all start with K, indicating that the received data could be used as a keystroke record. In fact, the key codes transmitted by the K101-D are QUICK and DIRECT keys as given in Table 9-3. The K101-D converts the setup screen into QUICK and DIRECT keys, groups them together to form a keystroke record, and transmits the record to an external memory. Later on, the record can be transmitted back to the K101-D, which will interpret it as a keystroke record and reconfigure the setup screen accordingly.

In the following command records, A, B, and M refer to memory A, B, and M, respectively.

Note

The following screen codes apply:

CZM -- Interface
CCA, CCB, CCM -- Clock select
CIA, CIB, CIM -- Input mode
CSA, CSB, CSM -- Trace control
CPA, CPB, CPM -- Logic polarity
CFM -- Data format
CCU -- Cursor location

Example

Receive interface setup menu (talk/listen record).

SEND: CZM

RECEIVE: K$ZA09)2)082682)1736)10>8)0)2)1)1

Length of string is 35 characters, including the CR/LF terminators.

End Example

Example

Receive Clock Select setup menu of
memory A (talk/listen record).

SEND: CCA

RECEIVE: K$CO)0020>2)0>2>2>2>2>2<<<)0>2>2>2>2>2<<<)0>2>2>2>2>2<<<)

Length of string is 61 characters, including the CR/LF terminators.

End Example

Example

Receive Input Mode setup menu of
memory B (talk/listen record).

SEND: CIB

RECEIVE: K$IC>8<)C>8<)C>8<)C>8<)C>8<)00000!2!1

Length of string is 44 characters, including the CR/LF terminators.

End Example

Example

Receive Trace Control setup menu of memory M (talk/listen record).

SEND: CSM

RECEIVE:

K$F2$SO>F>0203>0F)3)**********)
K0)>2
K2)**********)
K1)**********)
etc.

Length of string is about 2133 characters including the CR/LF terminators

End Example

Note

Whenever the Trace Control setup menu is formatted with keystroke records, the user should also format the Data Format setup menu. The K101-D changes the Data Format setup menu to binary every time the Trace Control setup menu is formatted with keystroke records. This is because a few characters in the Trace Control and Data Format menus are interrelated. In addition these characters cannot be represented by ASCII characters. For example, the DON'T CARE and SEMI-CARE characters have no equivalent simple ASCII characters. Whenever formatting the Trace Control menu, the user should also format the Data Format menu.

The CSA, CSB,and CSM commands have no effect on Data Format menu. These commands fetch the corresponding Trace Control menu as formatted by the user.

Example

Receive Logic Polarity setup menu of memory A (talk/listen record).

SEND: CPA

RECEIVE:

K$P++++++++++++++++)++++++++++++++++)++++++++++++++++)!2

Length of string is 58 characters, including the CR/LF terminators.

End Example

Example

Receive Data Format setup menu of memory M (talk/listen record).

SEND: CFM

RECEIVE:

K$F3)FCFCECDCCFCBCAC9C8C7C6C5C4C3C2C1C0*FBFBEBDBFBBBAB9B8FB7B6B5B4
KFB3B2B1B0*FAFAEADACFABAAA9A8FA7A6A5A4FA3A2A1A0/8((((((****)****)****
K)****)****)****)****)****)****)****)****

Length of string varies, depending on format selection.

End Example

Example

Receive locations of Control and Reference Cursors (talk/listen record).

SEND: CCU

RECEIVE: K$D/6000/7514

The Control Cursor C is located at 000 and the Reference Cursor at 514.

In the above example the received record starts with K, and can be set as a keystroke record. Also, 16 sets the Control Cursor and 17 sets the Reference Cursor. If the above record is transmitted back to the K101-D, the Control and Reference Cursors will be set to CRT locations 000 and 514, respectively. Thus, users can change 000 and 514 to the desired locations in the above record and send them back to the K101-D. The instrument will set the two cursors accordingly.

Length of string is 15 characters, including the CR/LF terminators.

End Example

9.3.4 MEMORY MODIFICATION RECORDS

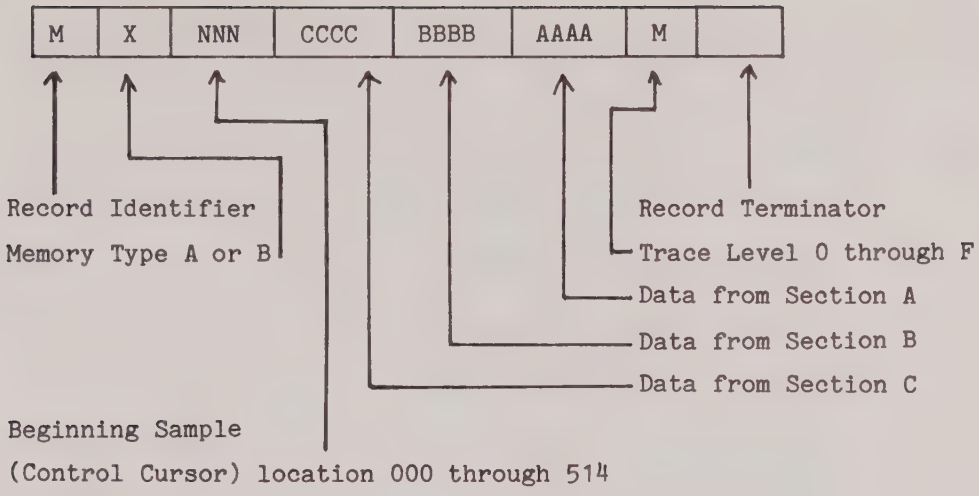
The memory modification records are used to send information from an external storage device to the K101-D memory. The information can be saved in memory A or B.

In several situations, the user may elect to change data in memory A or B. Initially, data should be transferred from memory A or B to an external storage device (e.g., a computer file). The data transfer can be accomplished by command records CMA or CMB.

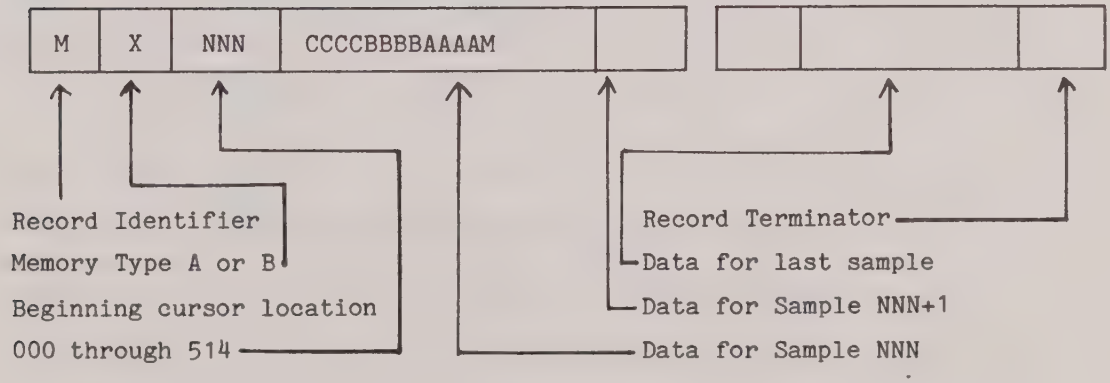
Once the data are transferred to a computer file, they can be edited with the help of the editor provided with the K101-D. The new data can then be transmitted back to the K101-D memory. This step is accomplished with memory modification records, which send data to locations 000 through 514 in memory A or B. The user must specify the beginning location of the record.

The data transfer to the K101-D memory must conform to the format shown below. The format should begin with character M to indicate that it is a memory modification record (see Figure 9-5).

The second character specifies the type of memory, either A or B. The following three characters define the location of the beginning of the record, which can be selected from 000 through 514. The next 12 characters are the hex-coded data. The first four are for section C; the next four, for section B; and the final four, for section A. The eighteenth character specifies trace level, and the last character is the termination character. The user can group samples in one record, in which case the format should be as shown below. When grouping records, data and trace level for each sample should be specified. The user should specify one record identifier, one memory type, and one beginning sample location for a group of records.



a. Memory Modification Record Format (One Sample Only)



b. Memory Modification Record Format (Group Samples)

Figure 9-5. Memory Modification Records.

Example

Change data in sample locations 006 and 007 in memory A (talk/listen record).

SET UP: Type data on your terminal as follows:

MA006020202020202F0101010101001CR

RESULT: Sample locations 006 and 007 in memory A are changed to 020202020202 and 010101010101, respectively. Also, the trace levels are changed to F and E for samples 006 and 007, respectively.

End Example

If the data are received from the K101-D using a CMA or CMB command record, the K101-D formats the transmitted data to conform to the memory modification record format. In this case, the user changes the sample data and sends the data back with no additional formatting.

Note

As shown in paragraph 9.3.3.1, the format of data received with the CMA or CMB command record is the same as the format of the memory modification record.

For block transmission mode terminals, the K101-D can receive up to 240 characters in a block. It can also receive 72 characters, including the termination character, in a line.

9.3.5 DISPLAY MESSAGE RECORD

As an extension of the instrument commands, a message record allows user messages to be sent to the K101-D screen. This is especially useful in automatic test equipment (ATE) applications.

This record displays a string of characters, starting at a desired location on the K101-D screen. The position of the message is given as row and column of numbers. There are 29 rows down the screen and 52 columns across the screen. The topmost and bottommost rows (rows 1 and 29, respectively) are used for the two lines of status information. These two lines are not accessible to the GPIB or the user. The message record format is shown in Figure 9-6a.

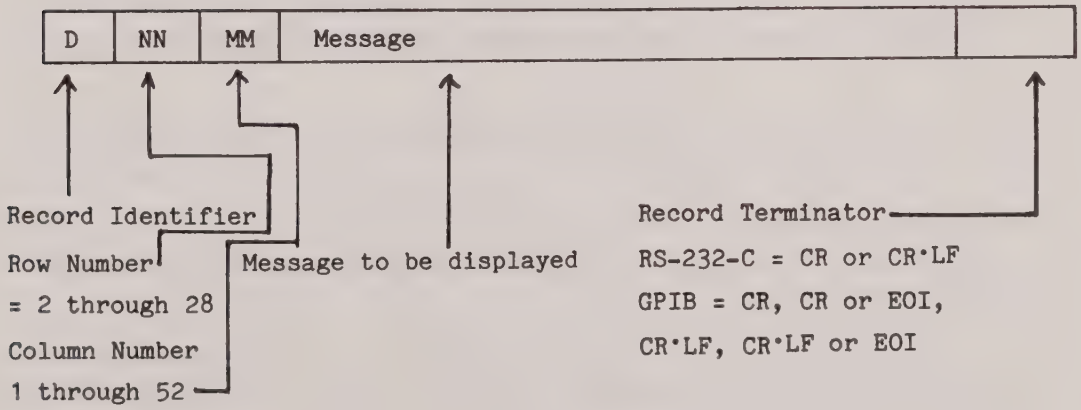


Figure 9-6a. Display Record Format.

The first character of a display record must be a D, the record type. The next two pairs of characters are the row and column positions, respectively. Two ASCII-encoded decimal digits are used for the row, and two for the column. The range of row values is 2 through 28; the range for column values is 1 through 52. If the specified row is out of range, row position 2 is used. If the specified column is out of range, column position 1 is used. The remaining characters constitute the message to be displayed. The row and column positions will be automatically incremented until row 28, column 52 has been displayed. If there are still more characters to display, the remainder of the message will be printed starting at row 2, column 1.

Example

Send a message to the K101-D.

```
SEND:     D0502 This is a message in row 5, column 2.
```

End Example

9.3.6 STATUS RECORD

The status record is transmitted by the K101-D in response to the CSR command record. The status record gives status of the K101-D. Its format is shown in Figure 9-6b.

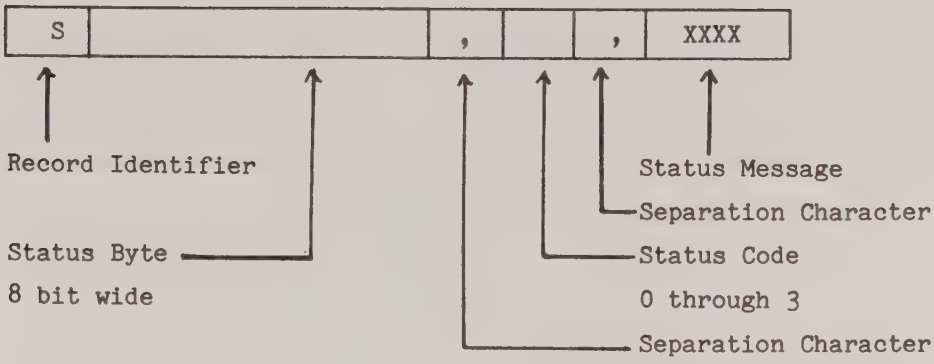


Figure 9-6b. Status Record Format.

The first character of a status record is an S. The next eight characters represents the status byte value. The value of each bit of the status byte is encoded as an ASCII 0 or ASCII 1. The value of the MSB (bit 8) is given first, down through the LSB (bit 1). The meaning of these bits can be found in Tables 9-4 and 9-5.

A comma starts the next field, "K101-D Recording Status." The recording status describes the current status of the K101-D recording cycle. The character in this field is the recording status Code, a number between 0 and 3. The status code meanings are given in Table 9-6. This character is followed by a comma. The next four characters comprise the recording status message, which is displayed in the lower right corner of the K101-D display.

Table 9-4. K101-D Status Byte Messages: GPIB Interface

Item No.	Bit Status[1]	Message
1	All 8 bits = zero	No error
2	Bits 1,7 = 1	Received illegal character[2]
3	Bits 1,3,7 = 1	Keycode error (local or remote source)[3]
4	Bits 1,2,3,7, = 1	Received unrecognized character[4]
5	Bits 5,7 = 1	Error in power up diagnostics
6	Bits 6,7 = 1	**SRQ** key pressed on the K101-D keyboard
7	Bit 7=1	Recording is complete and service is requested by the K101-D
8	Bit 8=1	Recording in progress

Notes:

1. All bits that are not specified are set to zero.

2. Illegal character means that the first letter of the character string received is an illegal record identifier, i.e., it is not K, C, M, or S.

3. Keycode error means that an illegal keycode within the keystroke record has been received by the K101-D.

4. Unrecognized character means that at least one character within a record (except a keystroke record) is illegal. For example, CMX will generate this error.

Table 9-5. K101-D Status Byte Message: RS-232-C Interface

Item No.	Bit Status	Message
1	All 8 bits = zeros	No error
2	Bits 1,3,7 = 1	Keycode error (local or remote source)
3	Bit 7=1	Recording is complete and service is requested by the K101-D
4	Bit 8=1	Recording In progress

Note: The keycode error means that an illegal keycode within the keystroke record has been received by the K101-D.

Table 9-6. Recording Status Codes

Status Code	Message
0	RDY
1	BUSY
2	CLK?
3	xxxx (Pass Count)

9.4 USING A PRINTER WITH THE K101-D

The user can transmit the setup screens, the displayed data and the memory contents of memories A and B to a printer terminal, via the GPIB or RS-232-C interface.

9.4.1 PRINTER TERMINAL WITH A KEYBOARD

A printer terminal with a keyboard can send a CMA or CMB command record to receive the contents of memory A or B, respectively. Send CPS to receive the currently displayed screen. The information on the screen is received as it is displayed on the instrument's screen. The information can be one of the setup menus or the data displayed using **DATA FORMAT** key. The user cannot transmit timing diagrams, graphs, or memory M contents. The graphic characters transmitted by the K101-D may not match the printer terminal in use and therefore could be meaningless.

9.4.2 PRINTING BY USING THE K101-D KEYBOARD

The user can print information from the K101-D by using the instrument's keyboard. This method is helpful when the printer does not have a keyboard (it may be used for a printer with a keyboard).

9.4.3 SUMMARY -- USE OF GPIB INTERFACE AND PRINTER

Proceed as follows:

a. Connect the printer to the K101-D with a GPIB cable. A connector labelled IEEE-488 is provided in the back of the instrument. The K101-D conforms to the IEEE-488 GPIB protocols.

b. Set the K101-D to Talk Only mode. Press **INTERFACE** to display the Interface setup menu. Press **NEXT** to set the instrument to Talk Only mode.

c. Display a setup screen of your choice by using one of the SPECIFY keys. Display data with **DATA** and

or

and

keys.

d. Press **SERVICE** to transmit the current screen to the printer. The printer should print the screen information as it is currently displayed on the screen.

To transmit memory contents, move the cursor to the command field, using the **REFERENCE SET** key. Enter CMA or CMB to transmit contents of memory A or B, respectively. The user can also enter any other command record to perform a desired activity.

Press **SHIFT** and **SPACE** to initiate information transmission to the printer.

Note

The printer must be on and configured to accept data.

9.4.4 SUMMARY -- USE OF RS-232-C INTERFACE AND PRINTER

a. Connect the printer to the K101-D with a RS-232-C cable. A female connector, labelled "RS-232-C", is provided in the back of the instrument.

b. Display the Interface setup menu by pressing the **INTERFACE** key.

c. Select a communication speed to match the speed of the printer. The speed can be 110, 150, 300, 600, 1200, 1800, 2400, 4800, or 5600 bps.

d. Select the stop bit.

e. Select parity (ODD, EVEN, or NONE) to match the printer.

f. Select word size: 7 bits or 8 bits wide.

The instrument is now configured to communicate with the printer.

g. Display on the screen the information to be printed.

h. Press **SHIFT** **SERVICE** to initiate information transmission to the printer. To print memory contents, see paragraph 9.3.4.

i. Move the cursor to the command field.

j. Enter CMA or CMB from the keyboard to print contents of memory A or B, respectively. Users can also enter any other command record to perform an activity of their choice.

k. Press **SHIFT** and **SPACE** to initiate information transmission to the printer.

Note

The printer must be on and configured to accept data.

9.5 GENERAL PURPOSE INTERFACE BUS (GPIB)

9.5.1 DESCRIPTION

The K101-D GPIB communication interface is an implementation of IEEE 488-1978, published 30 November 1978, under the title "IEEE Standard Digital Interface for Programmable Instrumentation." The implementation supports the capabilities and electrical interface as defined by that standard. The GPIB Interface capabilities are listed in Table 9-7.

9.5.2 GPIB INTERFACE CONNECTION

A female connector labeled IEEE-488, is provided in the back of the K101-D, for connection to one end of the GPIB cable. Connect the other end of the GPIB cable to a controller or to another K101-D. The instrument can be operated locally or from a remote station.

9.5.3 GPIB INTERFACE MESSAGES

a. **Interface Clear (IFC).** The IFC message clears the GPIB interface (talker, listener, and serial poll states are set to idle). If the instrument is transmitting a talk record when an IFC occurs, the remainder of the record is output when the instrument is next addressed to talk.

b. **Group Execute Trigger (GET).** A pulse is available on the rear panel GET BNC connector when this message is received during DAV = true. The K101-D does not respond internally to this signal.

c. **Device Clear or Selected Device Clear (DCL or SCD).** This command has the same effect as pressing STOP .

Table 9-7. GPIB Interface Capabilities

Function	K101-D Capability
Source handshake (SH1)	Complete capability
Acceptor handshake (AH1)	Complete capability
Talker function (T5)	Basic talker Talk only Unaddress if "MLA"
Talker function with address extension (TE0)	No capability
Listener function (L3)	Basic listener Listen only Unaddress if "MLA"
Listener function with address extension (LE0)	No capability
Service request (SR1)	Complete capability
Remote local function (RL1)	Complete capability
Parallel poll function (PP1)	Remote configuration
Device clear function (DC1)	Complete capability
Device trigger function (DT1)	Complete capability
Controller function (C0)	No capability

Note

The GPIB is inactive in Self-Test mode;
Self-Test cannot be operated via the GPIB.

9.5.4 GPIB STATUS INFORMATION PARALLEL POLL

The K101-D supports parallel polling. This feature checks the K101-D status rapidly when multiple devices are attached to the bus. When parallel poll is used, a device requiring attention is identified by a controller. Then the controller conducts a serial poll with that device. Parallel polling expedites communication between the K101-D and the controller.

The K101-D must be configured for parallel polling by a controller, using the following sequences:

```
ATN  =  TRUE
LDA       Listener address
PPC       Parallel poll configuration
PPE       Parallel poll enable
UNL       Unlisten
ATN  =  FALSE
```

When the controller conducts a parallel poll, it asserts ATN and EOI to read the parallel poll response bits.

The parallel poll response (PPR) state depends upon the sense bit (bit 4) of the parallel poll enable message (PPE) and the current request to service (RQS) state. The RQS is indicated by bit 7 of the status byte. The possible combinations of sense bit and RQS bit and the resulting PPR states are given in Figure 9-7.

RQS PPE	Status Byte Bit 7 = 0	Status Byte Bit 7 = 1
Sense Bit = 0	0	1
Sense Bit = 1	1	0

Figure 9-7. PPR States.

Example

The K101-D receives the following:

PPE = 01101000

The sense bit (bit 4) = 1.

If RQS is true (service requested), i.e., bit 7 of the status byte is set to 0, then from the above figure PPR = 00000001.

If RQS is false (service not requested), i.e., bit 7 of the status byte is set to 1, then from the above figure PPR = 00000000.

End Example

9.5.5 GPIB STATUS INFORMATION SERIAL POLL

A parallel poll will not clear the service request of the K101-D. A serial poll should be conducted to identify the reason for the service request. When the serial poll is conducted, the K101-D will drop its service request.

To conduct a serial poll, the controller uses the following sequence:

```
ATN  =  TRUE
UNL       Unlisten for all addressed devices
SPE       Serial poll enable
TAD       Talker address
ATN  =  FALSE
SBN       Status byte of device
ATN  =  TRUE
SPD       Serial poll disabled
ATN  =  FALSE
```

The above sequences are performed automatically by many GPIB controllers (e.g., HP85) whenever a serial poll is requested by the user program. These sequences are transparent to the users. Thus, users need not include the above sequences in their program. Below is an example of serial polling by the HP85.

9.5.6 GPIB STATUS BYTE

Whenever the K101-D requests service from a controller, the RQS bit (bit 7) of the status byte is set to one (1), as defined by the TPIB standards. The RQS bit remains set until the controller has performed a serial poll. Other bits of the status byte identify the reason for the service requested by the K101-D.

Example

User types.

```
I = SPOLL (730)
```

Note

The K101-D address = 30

The HP85 will serial poll the K101-D at address 30. It will go through the sequences outlined above. Display I to see the status byte in hex. (The status byte is explained in detail in the following section.)

End Example

The K101-D service request can also be cleared by using the CSR command record. The following example is for the HP85. Note that the second step must be successfully executed and the status byte must be received by the controller to clear the status byte.

Example

```
OUTPUT 730; "CSR."
```

```
OUTPUT 730; "CSR"
ENTER 730; A$
A$
```

Note

The K101-D address = 30

End Example

The above steps clear the K101-D service request, fetch the status byte, and display the status byte on the screen. The screen may display the following:

S00000101,0,RDY

The status byte indicates a keycode error.

If the above three steps are repeated, the screen displays the following:

S00000000,0,RDY

This indicates that the service request has been dropped by the K101-D.

The K101-D requests service under the following conditions:

a. **End of K101-D record cycle.** It is indicated by bit 7 of the status byte (bit 7 = 1).

b. **SRQ pressed (Talk/Listen mode).** The bit 6 of the status byte set to 1 indicates that the GPIB **SERVICE** key has been pressed on the K101-D keyboard.

c. **Error in power up diagnostics.** Bit 5 of the status byte set to 1 indicates that an error has been found during power up diagnostics.

d. **GPIB listen record error.** See Table 9-4 for complete details.

9.5.7 GPIB REFERENCES

a. "IEEE Standard Digital Interface for Programmable Instrumentation," (IEEE STD 488-1978). Osborne/McGraw-Hill

b. Pet and the IEEE-488 Bus, E. Fisher & C. Jensen, Osborne/McGraw-Hill, 1980.

c. Articles in Microcomputing, July 1980: Electronic Test, April, 1981.

d. "IEEE-488: Its Impact on the Design, Building and Programming of Automatic Test and Measurement Systems," by David W. Ricci, Hewlett-Packard. Presented at ELECTRO '80, Session 3: IEEE-488 User Fundamentals, May 13-15, 1980, Boston, MA.

9.6 THE RS-232-C INTERFACE

This interface is provided for applications in which the K101-D is remotely controlled via modems and a telephone line or connected to a local peripheral. The transmission characteristics can be selected in the Interface setup menu. The K101-D is configured as data terminal equipment (DTE).

9.6.1 PROTOCOLS

The modem control lines are used to control an asynchronous modem. The RTS/CTS handshake is used to synchronize two devices with different processing speeds. This feature protects the internal buffer from overflowing with received characters. The K101-D uses the DTR (data terminal ready) signal to indicate imminent buffer overflow. When this signal occurs, the user must stop sending data until this signal is released. The K101-D will cease transmission if the CTS (clear to send) signal goes false.

Many computers and peripheral equipment use XOFF/XON (DC3/DC1, control S/control Q in ASCII table) protocol to synchronize their data exchange. The K101-D/RS-232-C interface incorporates this software protocol. When the K101-D can only accept a few more characters, it will send an XOFF

character (control S) to signal that it needs some time to empty and process the input buffer. The XON character in turn indicates that the K101-D is ready to accept more data. If the K101-D receives an XOFF character, it will not transmit any information until it has received an XON character.

Note

The NAK/ACK protocol as used in software versions 4.0 and 4.2 does not work. transmit blocks no more than 250 characters long and include at least a 0.5 second wait between consecutive transmissions. The software versions also do not drop DTR during the imminent input buffer overflow. Since DTR controls the user's CTS signal, the hardware handshake cannot be used to secure proper data transmission.

9.6.2 RS-232-C INTERFACE CONNECTION

9.6.2.1 **Connector**

A rear panel female connector, labeled RS-232, is provided. To access the K101-D from a remote location, connect it to a modem or an acoustic coupler with an RS-232-C cable. The cable should have male connectors on both ends. The instrument can also be connected to various computers and computer peripherals. Most computer peripherals operate as DTE, indicated by a female connector in the back. To connect the K101-D to the peripherals, the user needs an RS-232-C cable with male connectors on both ends. In addition, pins 2 and 3 have to be interchanged on one end to transfer proper signals. This is essentially an implementation of the null modem.

9.6.2.2 The Null Modem

One way to connect a terminal is to use the simple circuit shown in Figure 9-8a. This circuit does not provide handshake capabilities.

An alternate configuration is shown in Figure 9-8b. This circuit allows logic handshaking using the DTR/DSR lines.

The interconnection shown in Figure 9-9 is a complete arrangement for interconnecting the K101-D to any computer, using the earlier described hardware handshake.

9.6.3 RS-232 REFERENCES

a. EIA Standard, "Interface between DTE and DCE, RS-232-C, Electronic Industries Association, August 1969.

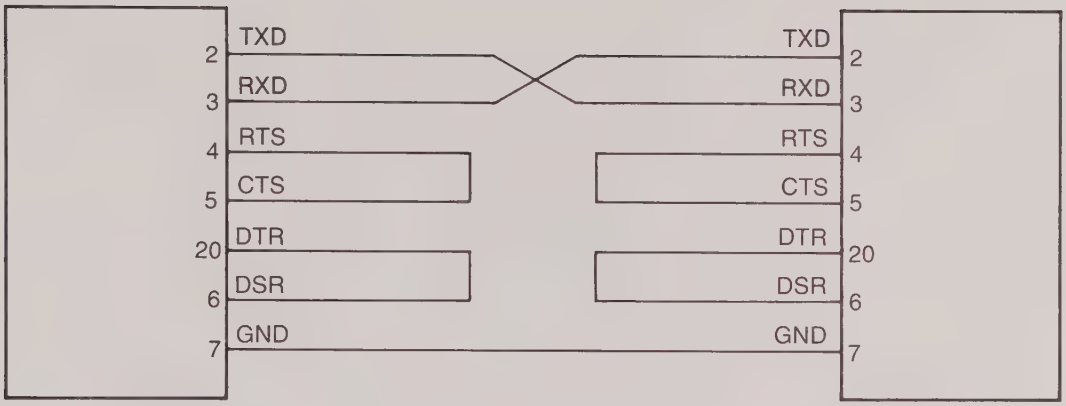
b. EIA, Application Notes for RS-232-C Standard (Bulletins 9 and 12), Electronic Industries Association, May 1971 (Bulletin 9), and November 1977 (Bulletin 12).

c. CCITT Series V Recommendations, International Telecommunications Union, 1978.

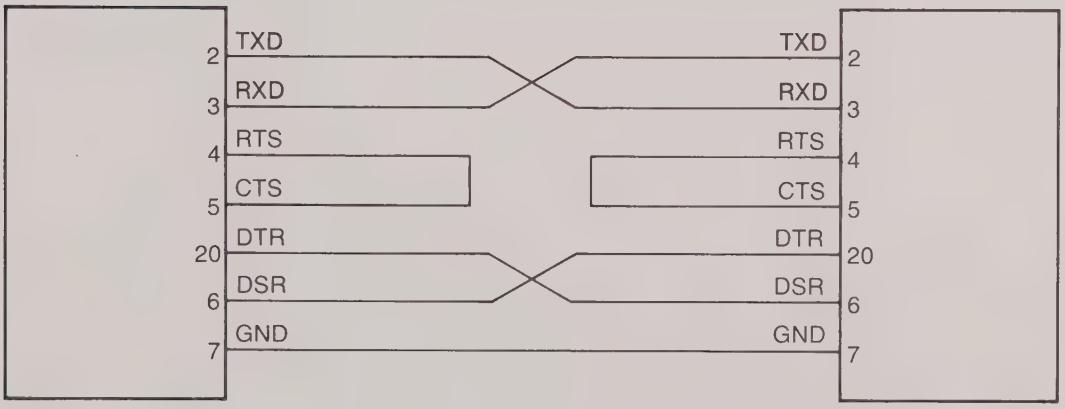
d. 8251 PCI data sheets and application notes of various Data Communications chips.

e. Digital, Technical Aspects of Data Communication, J. McNamara, Digital Press, July 1979 (Original printing 1977).

f. Data Communication Handbook, A. Weissberger, 1978.



a. Simple Null Modem Wiring Diagram.



b. Null Modem Wiring Diagram with DTR/DSR.

Figure 9-8. Null Modem Wiring Diagrams.

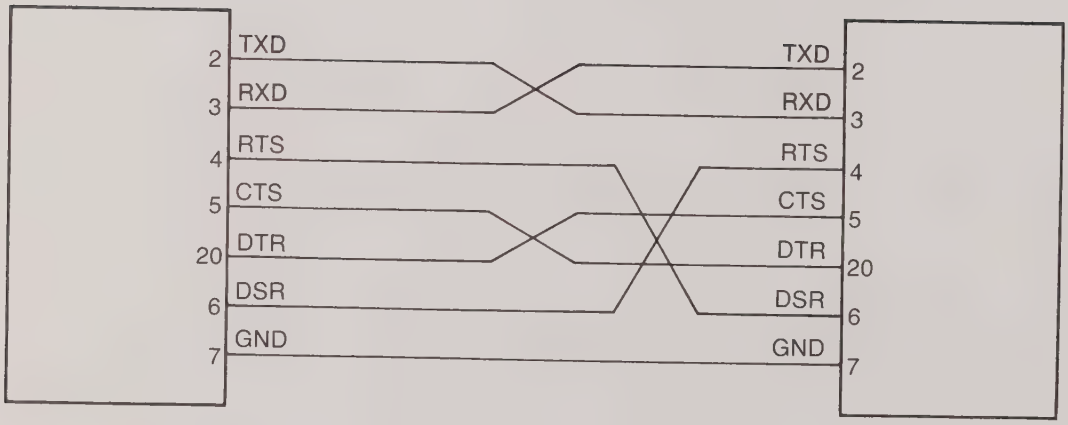


Figure 9-9. Complete Null Modem.

Section 10

MEASUREMENT CONFIDENCE

10.1 INTRODUCTION

The K101-D has three self-diagnostic routines to give you confidence that it is operating correctly: Probe Test, Power Up Test, and Self-Test. Successful completion of these tests ensures that your K101-D is operating correctly and that the measurements it makes are valid. If there is a problem in the analyzer, these tests help you to quickly identify the problem.

a. **Probe Test:** The two clock and eight sample inputs of each probe can be quickly tested for correct detection of signal inputs by a built-in Probe Test socket which generates a known ring-counter pattern and clocking signals. Besides physically checking a probe's inputs, Probe Test can be used to explore and understand the operation of the K101-D itself.

b. **Power Up Test:** When the K101-D is turned on, a series of tests is automatically performed. The unit's ROM, RAM, power supply, CMOS RAM, USARTs, and keyboard are checked for correct operation.

c. **Self-Test:** For maximum confidence in the K101-D's operation, any of a series of detailed diagnostic tests may be performed. There are also troubleshooting test routines to help you debug any instrument error that may appear. Running Self-Test before calling the factory or shipping your instrument back for repair could save you a lot of time, trouble, and money.

10.2 **PROBE TEST**

The Probe Test discussion is intended to familiarize you with the operation of the K101-D, and verify that the equipment is working properly. The examples in this section are related to the A section inputs, and are summarized in Table 10-1. These examples are designed to be performed sequentially. The directions for creating a specific setup assume you will only need to make changes from the preceeding setup. Where appropriate, setup guides and illustrations of the desired setup screens are included to help you check that your setup is correct.

Turn the power on. Once the power up test sequence is complete, press **SHIFT, RECALL** to initialize all setups to their default values.

> Note
>
> If you make a mistake on a particular example you can start over by using the **SHIFT/RECALL** keys.

10.2.1 PROBE CONNECTION

Plug the SECTION A INPUTS CLK J, K, F . . . 8 probe cable into its front panel input and the pod into the Probe Test socket. The probe PC board key slot should be on your left and the pod labels facing up. To avoid getting noise on the other inputs, plug all the other probe cables into their appropriate front panel section inputs.

Table 10-1. Probe Test Exercises

Topic	Paragraph Number
Probe Connection	10.2.1
Polarity and Threshold:	
a. Fixed TTL	10.2.2.1
b. Fixed ECL	10.2.2.2
c. Stabilize pattern	10.2.2.3
d. Variable threshold	10.2.2.4
e. Negative polarity	10.2.2.5
Data Format:	
a. Delete inputs	10.2.3.1
b. Repeat inputs	10.2.3.2
c. Fixed format	10.2.3.3
Clock and Input:	
a. Sample internally	10.2.4.1
b. Sample -- single external clock	10.2.4.2
c. Sample -- multiple external clocks	10.2.4.3
d. Latch (Enable) -- combination	10.2.4.4
e. Demux -- single enable input	10.2.4.5
f. Demux -- combination enable inputs	10.2.4.6
Basic Trace Control:	
a. Fill MEM from anywhere	10.2.5.1
b. Record immediately after event	10.2.5.2
c. Record immediately before event	10.2.5.3
d. Record around an event	10.2.5.4
e. Record long after event	10.2.5.5
f. Record from here to there	10.2.5.6
g. Don't record from here to there	10.2.5.7

Table 10-1. Probe Test Exercises (Cont'd)

Topic	Paragraph Number
h. Selectively record -- n times	10.2.5.8
i. Follow a path -- then record	10.2.5.9
j. Record -- then follow a path	10.2.5.10
k. Check for event 1 or 2	10.2.5.11
l. Take same path -- ignore events	10.2.5.12
m. Check timing between two events	10.2.5.13
n. Monitor for correct operation	10.2.5.14
Advanced Trace Control:	
a. Continuous check -- path and timing	10.2.6.1
b. Trace independent of execution path	10.2.6.2
c. End level break point	10.2.6.3
d. Segments, patterns, and total trace time	10.2.6.4
Record:	
a. Manual arm	10.2.7.1
b. Auto arm	10.2.7.2
c. Limiting the count	10.2.7.3
d. Stop if A $\neq$ B	10.2.7.4
e. Auto Stop if A = B	10.2.7.5
f. Auto Stop if A $\neq$ B within limits	10.2.7.6
g. Auto Stop if A = B within limits	10.2.7.7

10.2.2 POLARITY AND THRESHOLD

10.2.2.1 **Fixed TTL Threshold**

SET UP: None required. Uses the default values.

RECORD: Press ARM . This will arm (enable) recording of data.

REVIEW: Display timing data page 4. Press TIMING , PAGE 4 K four times to reach page 4.

You should see all zeros on all inputs (see Figure 10-1). This is because the Probe Test signals are generated by ECL logic, which typically uses a threshold of -1.30 volts (well below the default TTL value of +1.4 volts).

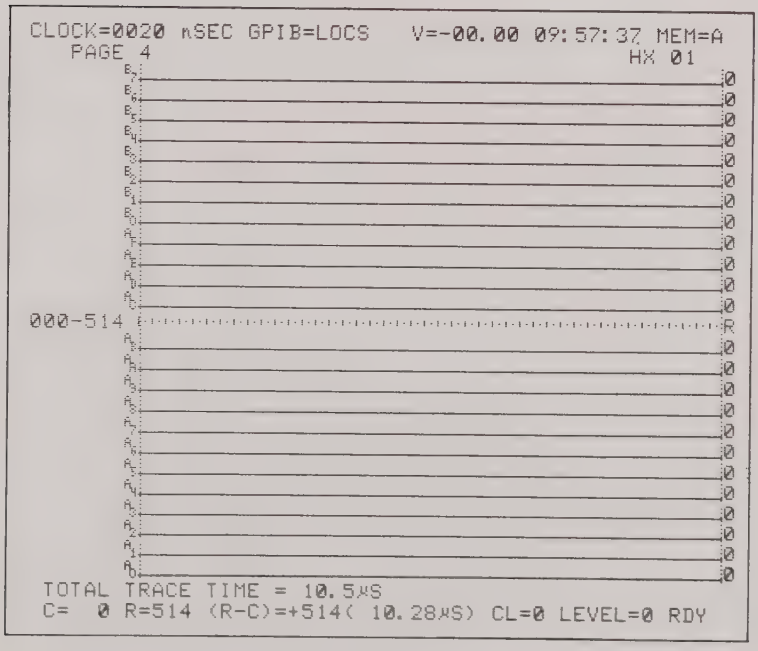


Figure 10-1. Resulting Probe Test Recording Using a TTL Threshold.

10.2.2.2 **Fixed ECL Threshold**

SET UP: Press INPUT MODE.

Change the threshold for inputs AF through A8 to ECL by moving the blinking cursor to the AF-A8 line of the Input Mode display and change TTL to ECL.

Press △ three times, ▷, 9 (EBCDIC / ECL).

RECORD: Press ARM.

REVIEW: Press TIMING.

A staircase pattern of pulses should be seen (Figure 10-2). This pattern may start anywhere on the screen because of the default trace control program, "Fill Memory with Samples from Anywhere in the Data Stream." Use the Control and Reference Cursors to measure the characteristic total trace time of 10.5 microseconds and pulse width of 0.9 microseconds.

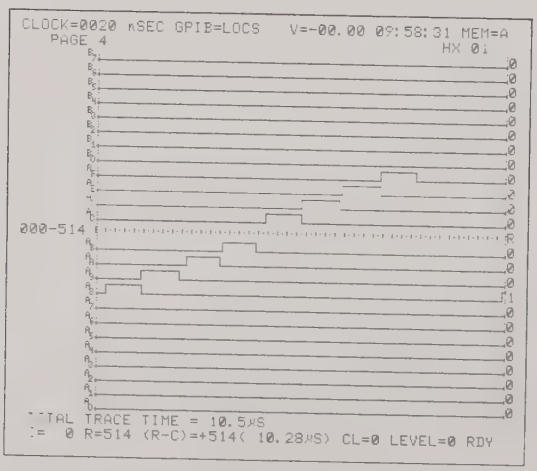


Figure 10-2. Typical Probe Test Recording Using an ECL Threshold.

10.2.2.3 **Stabilize Pattern**

SET UP: Obtain one full pattern that starts in the same location every time. Change the S word recognizer to S = xxxx xxxx 01xx.

Press TRACE CONTROL .

Move the cursor to S. Press ▽ SET twice, ◁ SET eight times, then 0 (Hx1) G, 1 (Hx3) H.

RECORD: Press ARM .

REVIEW: Press TIMING .

The display should look like Figure 10-3. The pattern will begin in the same location every recording through the use of the trace control command STOP IF DATA = S AND SAMPLE COUNT DELAY WHERE S = XXXX XXXX 01XX and DELAY = DEC 515 CLOCKS. Note that the total trace time is greater than 10.5 microseconds because of the extra time spent waiting for the specified trace control STOP condition to come true.

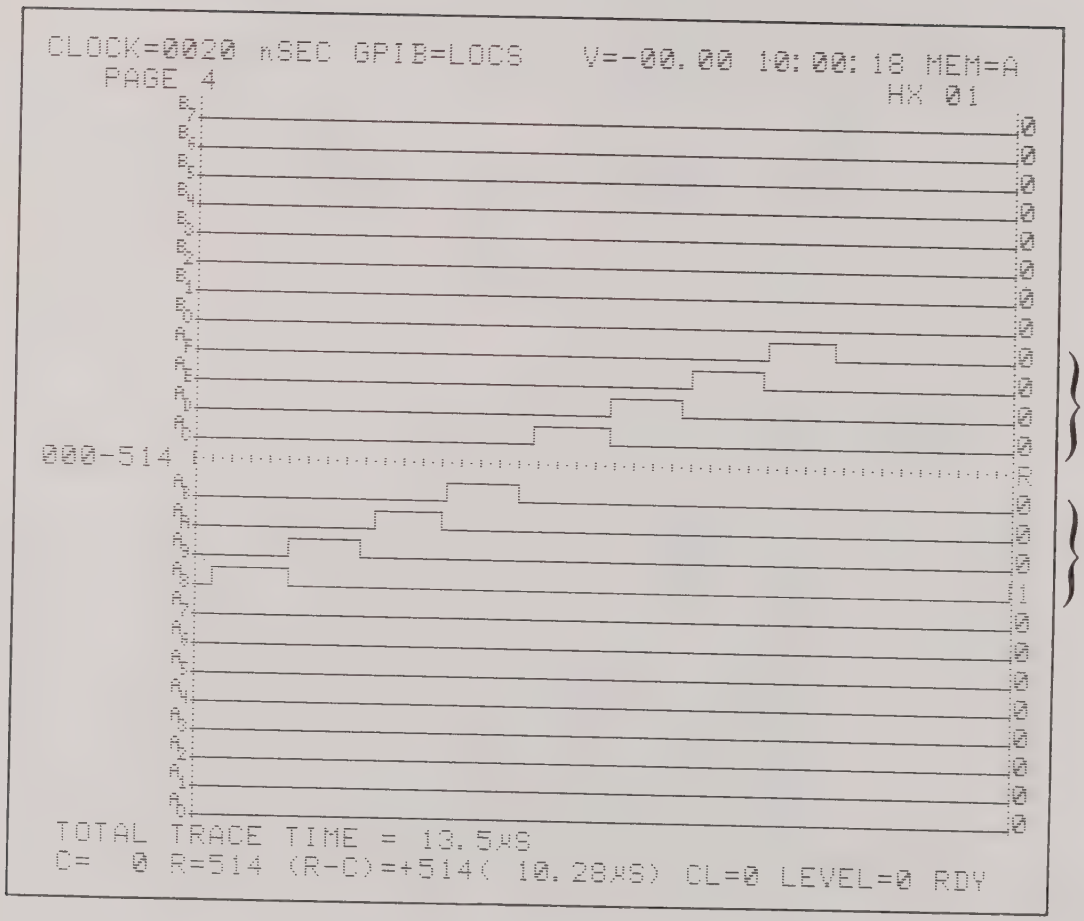


Figure 10-3. Fixed Location Pattern.

10.2.2.4 **Variable Threshold**

SET UP: Display the Input Mode screen.

Press [INPUT MODE] .

Change the threshold for inputs AF through A8 to VARA.

Press [△] three times, [▷] , [ASCII A Q] .

Change the value to something other than -1.30 volts such as -1.00 volts. Move the cursor to the numerical value and enter the digits (which are entered sequentially).

Press [▷] , [FALSE −] , [Hx3 1 H] , [Hx1 0 G] , [Hx1 0 G] .

RECORD: Press [ARM] .

REVIEW: Press [TIMING] .

Look for any difference in the pattern such as missing or shortened (<0.9 microsecond) pulses (check pulse width with the cursors), as shown in Figures 10-4 and 10-5, respectively. In Figure 10-4 note that the pulses that do not exceed the threshold will not be detected (threshold = 0.00 volts). In Figure 10-5 note that slow rise and fall times cause only that portion of the pulse that exceeds the threshold to be detected (threshold = +0.50 volts). If you see no irregularities, go back and change the threshold to some other value, record, and review again. Repeat this process until you perceive a noticeable change.

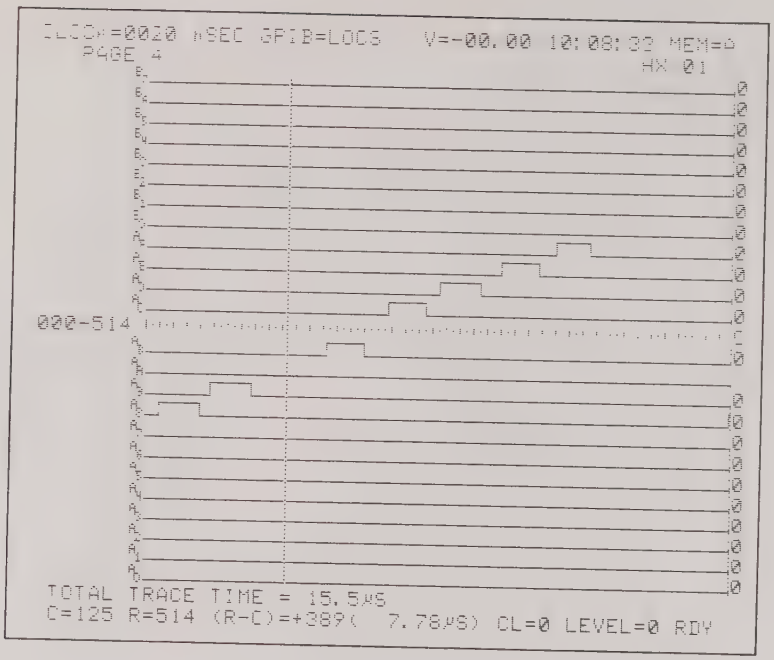


Figure 10-4. Pattern Changes with Threshold Changes.

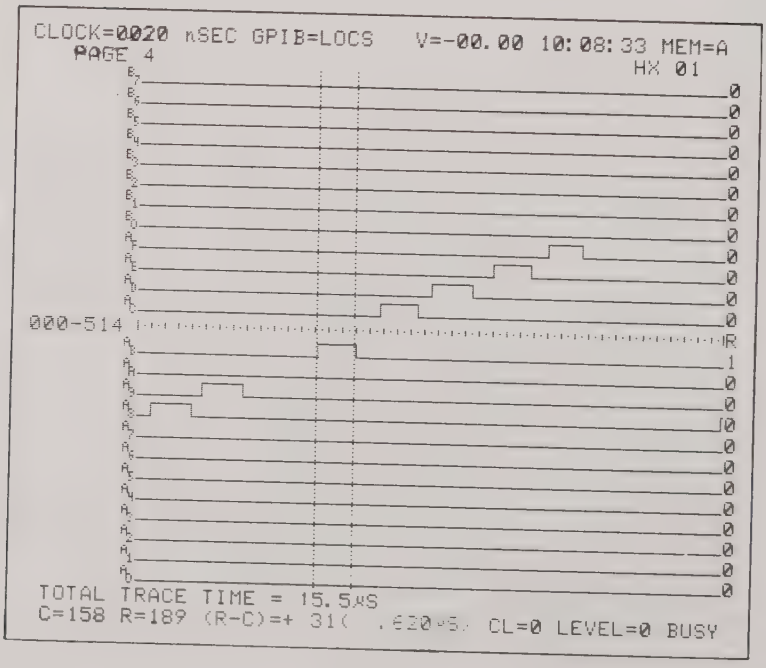

CLOCK=0020 nSEC GPIB=LOCS V=-00.00 10:08:33 MEM=A
PAGE 4
HX 01
000-514
TOTAL TRACE TIME = 15.5µS
C=158 R=189 (R-C)=+ 31(.620µS) CL=0 LEVEL=0 BUSY

Figure 10-5. Effect of Rise and Fall Time.

10.2.2.5 **Negative Polarity**

SET UP: Display logic polarity screen. Press LOGIC POLARITY .

Change the polarity of inputs AF through A8 to negative.

Press ▽ SET twice, FALSE − eight times.

Return threshold to ECL.

Press INPUT MODE , △ three times, ▷ , EBCDIC 9 ECL P.

RECORD: Press ARM .

REVIEW: Press TIMING .

The trace level status will say LEVEL = 0 BUSY. (The displayed timing information is from the previous recording.) Trace control looks for 01 (hex) but never sees it because of the reversed polarity. Check what information is flowing from memory M to memory A.

Press M→A .

The display shows what information was flowing into memory and through trace control (see Figure 10-6). With negative polarity, positive-going pulses are a logical "0." The total trace time reading reflects the time between your pressing of the **ARM** and **M -> A** keys. Move the Control or Reference Cursor through the pulses (by holding down the appropriate cursor keys) while watching the binary cursor readout. Stop when the cursor is at the A8 input pulse. Note that for inputs AF through A8, a positive-going pulse is detected and represented as a logical "0," which is the definition of negative polarity.

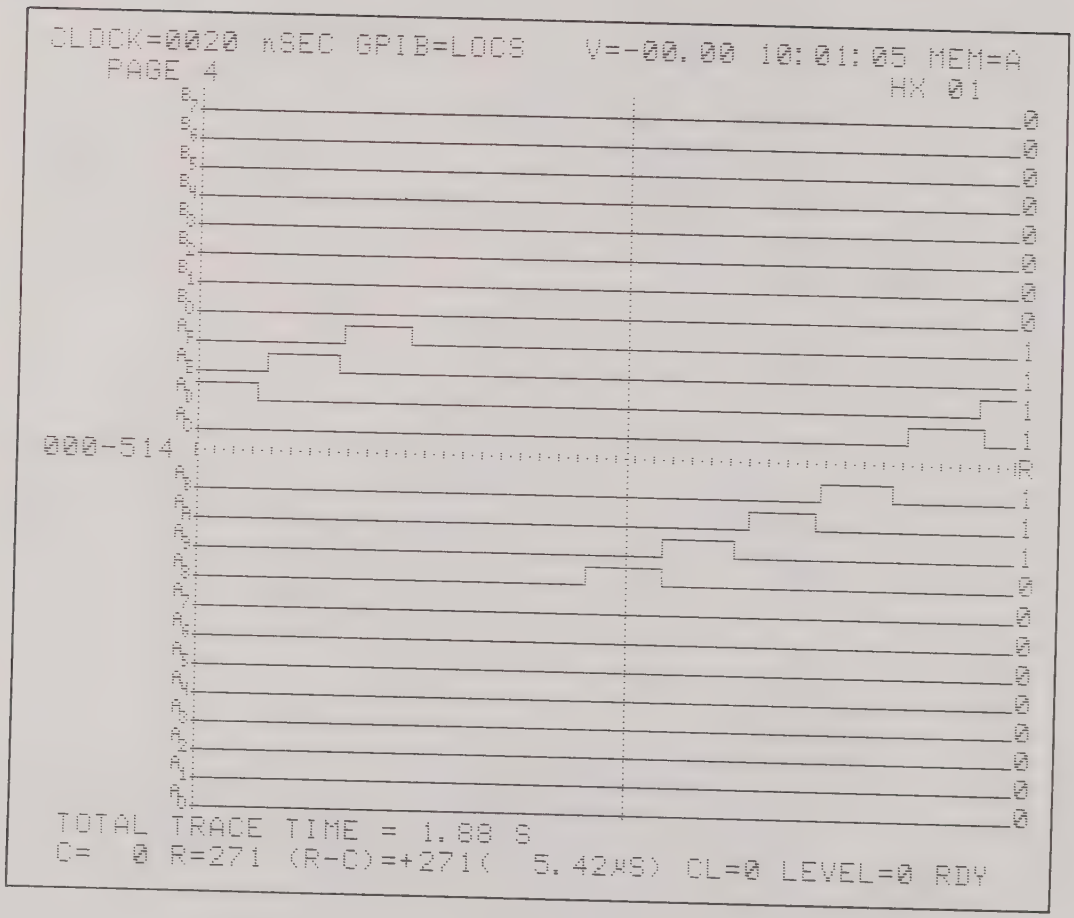


Figure 10-6. Information Flow.

10.2.3 DATA FORMAT

10.2.3.1 **Delete Inputs**

SET UP: See setup guide in Figure 10-7. Display Clock Select screen.

Press CLOCK SELECT .

Select the first option. Press Hx3 1 H .

Move to the master clock line. Press ▽ SET twice.

Select second option and move cursor. Press Hx6 2 ' , ▷ twice.

Select first option. Press Hx3 1 H .

Select Logic Polarity display. Press LOGIC POLARITY .

Move cursor to A section. Press ▽ SET twice.

Enter plus polarity for first eight inputs. Press TRUE + eight times.

The Clock Select and Trace Control displays should now look like Figures 10-8 and 10-9.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 31 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H H H H H H H H H H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	$C_F C_B C_7 C_3$ $B_F B_B B_7 B_3$ $A_F A_B A_7 A_3$
A T 2	$C_E C_A C_6 C_2$ $B_E B_A B_6 B_2$ $A_E A_A A_6 A_2$
S 1	$C_D C_9 C_5 C_1$ $B_D B_9 B_5 B_1$ $A_D A_9 A_5 A_1$
LSB	$C_C C_8 C_4 C_0$ $B_C B_8 B_4 B_0$ $A_C A_8 A_4 A_0$

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
At most five commands in each level can be true on any of nine consecutive

Quick Key	Command Condition
0	If DATA ≠ D
1	Always
2	Never
3	If DATA = D and Sample Count ... Delay
4	If DATA = D and Sample Count ... Delay
5	If DATA = D and Sample Count ... Delay
6	If DATA = D and Sample Count ... Delay
7	If DATA = D and Sample Count ... Delay
8	If DATA = D and Sample Count ... Delay

(D, S, J, A, or T, which are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = DEC 515 (DEC/HEX, 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F) — COMMENTS

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY

S = X X X X X X X X X X X X X X X X

(2) JUMP TO 0 (O-F) NEVER

J = X X X X X X X X X X X X X X X X

(2) ADVANCE NEVER

A = X X X X X X X X X X X X X X X X

(1) TRACE ALWAYS

T = X X X X X X X X X X X X X X X X

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

( ) STOP

S =

( ) JUMP TO ___ (O-F)

J =

( ) ADVANCE

A =

( ) TRACE

T =

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

( ) STOP

S =

( ) JUMP TO ___ (O-F)

J =

( ) ADVANCE

A =

( ) TRACE

T =

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

( ) STOP

S =

( ) JUMP TO ___ (O-F)

J =

( ) ADVANCE

A =

( ) TRACE

T =

Figure 10-7. Setup (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 3.1 OF ___ DATE ___

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (.1.) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

INTERNAL CLOCK PERIOD = _____

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)
SECTION B = (_____●_____●_____) + (_____+_____+_____)
SECTION A = (_____●_____●_____) + (_____+_____+_____)

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ___ 0-9999

QUICK KEY (.0.) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
GROUP B	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
GROUP A	±	±	±	±	±	±	±	±	_	_	_	_	_	_	_	_

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX — Fixed hex format & CF AO sequence
1	OCTAL — Fixed octal format & CF AO sequence
2	BINARY — Fixed binary format & CF AO sequence
3	MIXED USER SEQN — Any radix, any sequence
4	MIXED CF AO SEQN — Any radix, fixed CF AO sequence
5	DEVICE MNEMONICS — Fixed disassembled µP code format, only if RTE-816 attached OR DEVICE NOT AVAILABLE — No RTE-816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL — Allows the internal clock to run the Master, Section A, Section B, and Section C clocks.

1 EXTERNAL SINGLE-PHASED — Allows a single-phased external clock to run the Master, Section A, Section B, and Section C clocks.

2 EXTERNAL MULTI-PHASED — Allows a multi-phased external clock to run the Master, Section A, Section B, and Section C clocks.

3 MASTER EXTERNAL — Master clock is external. Section A, Section B, and Section C clocks are internal.

4 MASTER EXTERNAL — Master clock is external. Section A clock is external. Section B and Section C clocks are internal.

5 MASTER EXTERNAL — Master clock is external. Section A and Section B clocks are external. Section C clock is internal.

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
.	A.I.
,	Auto Store A & B
4	A Store A & B
.	A Store A & B

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 10-7. Setup (Sheet 2 of 2).

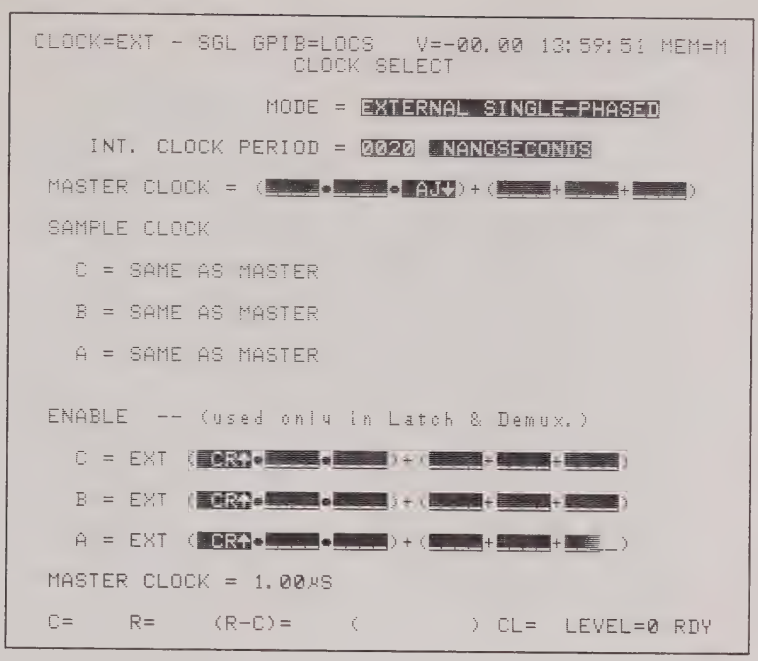

CLOCK=EXT - SGL GPIB=LOCS V=-00.00 13:59:51 MEM=M
CLOCK SELECT
MODE = EXTERNAL SINGLE-PHASED
INT. CLOCK PERIOD = 0020 NANOSECONDS
MASTER CLOCK =
SAMPLE CLOCK
C = SAME AS MASTER
B = SAME AS MASTER
A = SAME AS MASTER
ENABLE -- (used only in Latch & Demux.)
C = EXT
B = EXT
A = EXT
MASTER CLOCK = 1.00µS
C= R= (R-C)= ( ) CL= LEVEL=0 RDY

Figure 10-8. Clock Select for Delete Example.

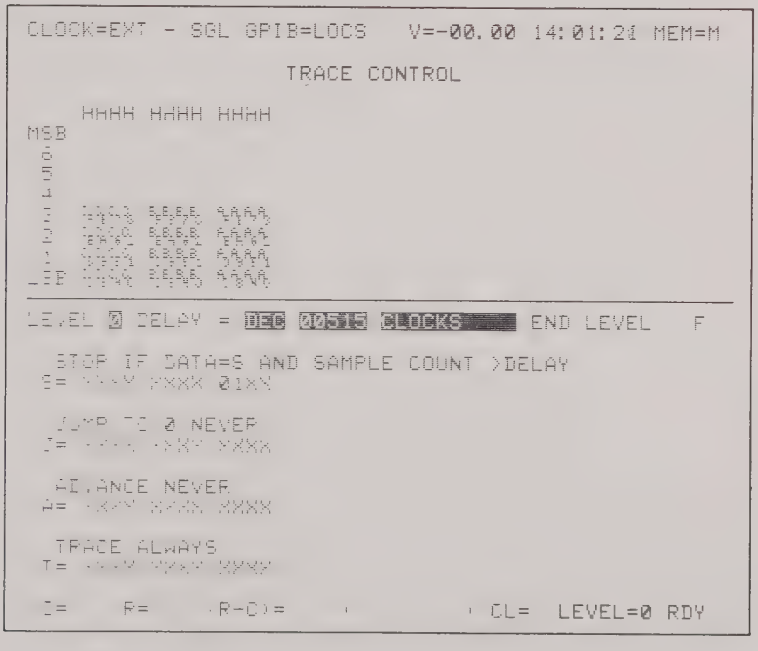

CLOCK=EXT - SGL GPIB=LOCS V=-00.00 14:01:24 MEM=M
TRACE CONTROL
MSB
LEVEL 0 DELAY = DEC 00515 CLOCKS END LEVEL F
STOP IF DATA=S AND SAMPLE COUNT >DELAY
JUMP TO 0 NEVER
ADVANCE NEVER
TRACE ALWAYS
C= R= (R-C)= ( ) CL= LEVEL=0 RDY

Figure 10-9. Trace Control for Delete Example.

RECORD: Press ARM .

REVIEW: Display the synchronously recorded pattern.

Press TIMING , Hx12 3 J .

Display the data. Press DATA .

The display should look like Figure 10-10 which is full data display for inputs AF through A8, probe test recording. . (If any columns are filled with Fs, it means that the probe is not plugged into the front panel.)

Display the corresponding graph (see Figure 10-11) which is based on the original data format. Since the hex value of each 12-character word is close to zero, only a baseline can be seen.

```
CLOCK=EXT - SGL GPIB=LOCS   V=-00.00 10:16:24 MEM=A

     HHHH HHHH HHHH                HHHH HHHH HHHH
000C0000 0000 0000          024 0000 0000 0800
001 0000 0000 0100          025 0000 0000 1000
002 0000 0000 0200          026 0000 0000 2000
003 0000 0000 0400          027 0000 0000 4000
004 0000 0000 0800          028 0000 0000 8000
005 0000 0000 1000          029 0000 0000 0000
006 0000 0000 2000          030 0000 0000 0000
007 0000 0000 4000          031 0000 0000 0100
008 0000 0000 8000          032 0000 0000 0200
009 0000 0000 0000          033 0000 0000 0400
010 0000 0000 0000          034 0000 0000 0800
011 0000 0000 0100          035 0000 0000 1000
012 0000 0000 0200          036 0000 0000 2000
013 0000 0000 0400          037 0000 0000 4000
014 0000 0000 0800          038 0000 0000 8000
015 0000 0000 1000          039 0000 0000 0000
016 0000 0000 2000          040 0000 0000 0000
017 0000 0000 4000          041 0000 0000 0100
018 0000 0000 8000          042 0000 0000 0200
019 0000 0000 0000          043 0000 0000 0400
020 0000 0000 0000          044 0000 0000 0800
021 0000 0000 0100          045 0000 0000 1000
022 0000 0000 0200          046 0000 0000 2000
023 0000 0000 0400          047 0000 0000 4000

 C=  0 R=514 (R-C)=+514(         ) CL=0 LEVEL=0 RDY
```

Figure 10-10. Data Display, Probe Inputs AF through A8.

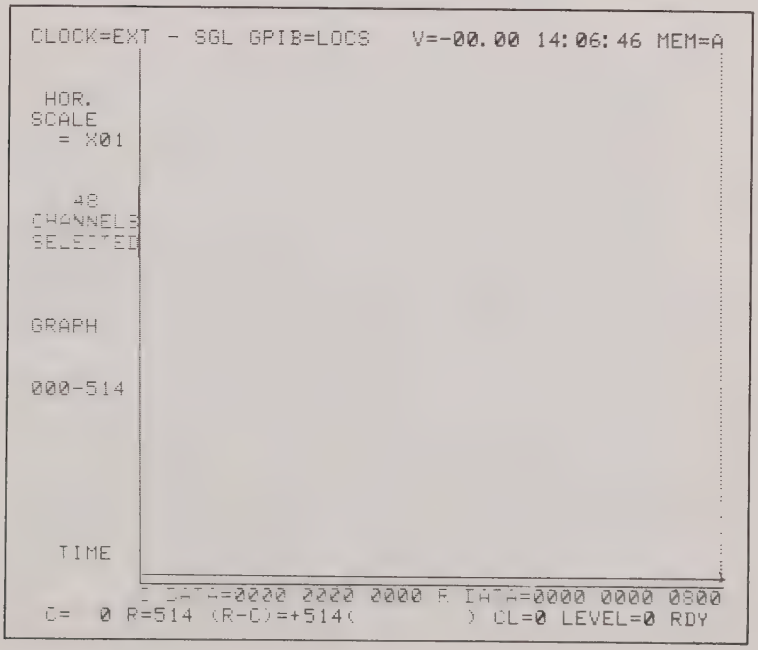


Figure 10-11. Graph of Data of Figure 10-10.

Press GRAPH .

Display the data format. Press DATA FORMAT .

Delete all inputs except AF through A8.

Press ▽ SET , DELETE ten times, ▷ twice, DELETE twice.

Check that the word recognizer formats have correspondingly changed.

Press TRACE CONTROL (see Figure 10-12). Note that changing the data format also changes the trace control's word recognizer format.

Press DATA (see Figure 10-13).

Check the new graph format.

Press GRAPH (see Figure 10-14).

Note the number of channels selected and that changing the data format changes the input channels that are graphed.

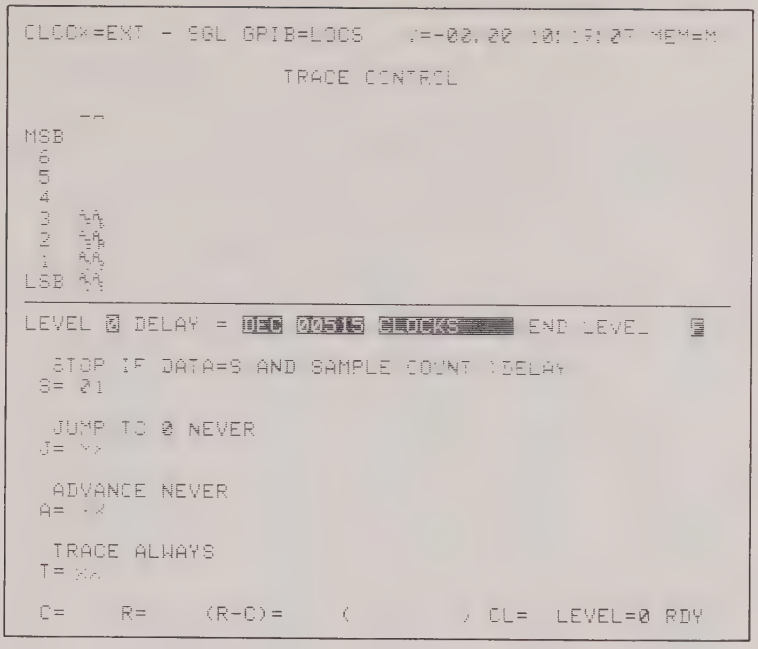


Figure 10-12. Data Format/Word Recognizer Changes.

CLOCK=EXT - SGL GPIB=LOCS V=-00.00 10:16:24 MEM=A

	HH		HH		HH		HH		HH		HH
000	C00	024	08	048	80	072	02	096	20	120	00
001	01	025	10	049	00	073	04	097	40	121	01
002	02	026	20	050	00	074	08	098	80	122	02
003	04	027	40	051	01	075	10	099	00	123	04
004	08	028	80	052	02	076	20	100	00	124	08
005	10	029	00	053	04	077	40	101	01	125	10
006	20	030	00	054	08	078	80	102	02	126	20
007	40	031	01	055	10	079	00	103	04	127	40
008	80	032	02	056	20	080	00	104	08	128	80
009	00	033	04	057	40	081	01	105	10	129	00
010	00	034	08	058	80	082	02	106	20	130	00
011	01	035	10	059	00	083	04	107	40	131	01
012	02	036	20	060	00	084	08	108	80	132	02
013	04	037	40	061	01	085	10	109	00	133	04
014	08	038	80	062	02	086	20	110	00	134	08
015	10	039	00	063	04	087	40	111	01	135	10
016	20	040	00	064	08	088	80	112	02	136	20
017	40	041	01	065	10	089	00	113	04	137	40
018	80	042	02	066	20	090	00	114	08	138	80
019	00	043	04	067	40	091	01	115	10	139	00
020	00	044	08	068	80	092	02	116	20	140	00
021	01	045	10	069	00	093	04	117	40	141	01
022	02	046	20	070	00	094	08	118	80	142	02
023	04	047	40	071	01	095	10	119	00	143	04

C= 0 R=514 (R-C)=+514( ) CL=0 LEVEL=0 RDY

Figure 10-13. New Data Display for Figure 10-12 Data Format.

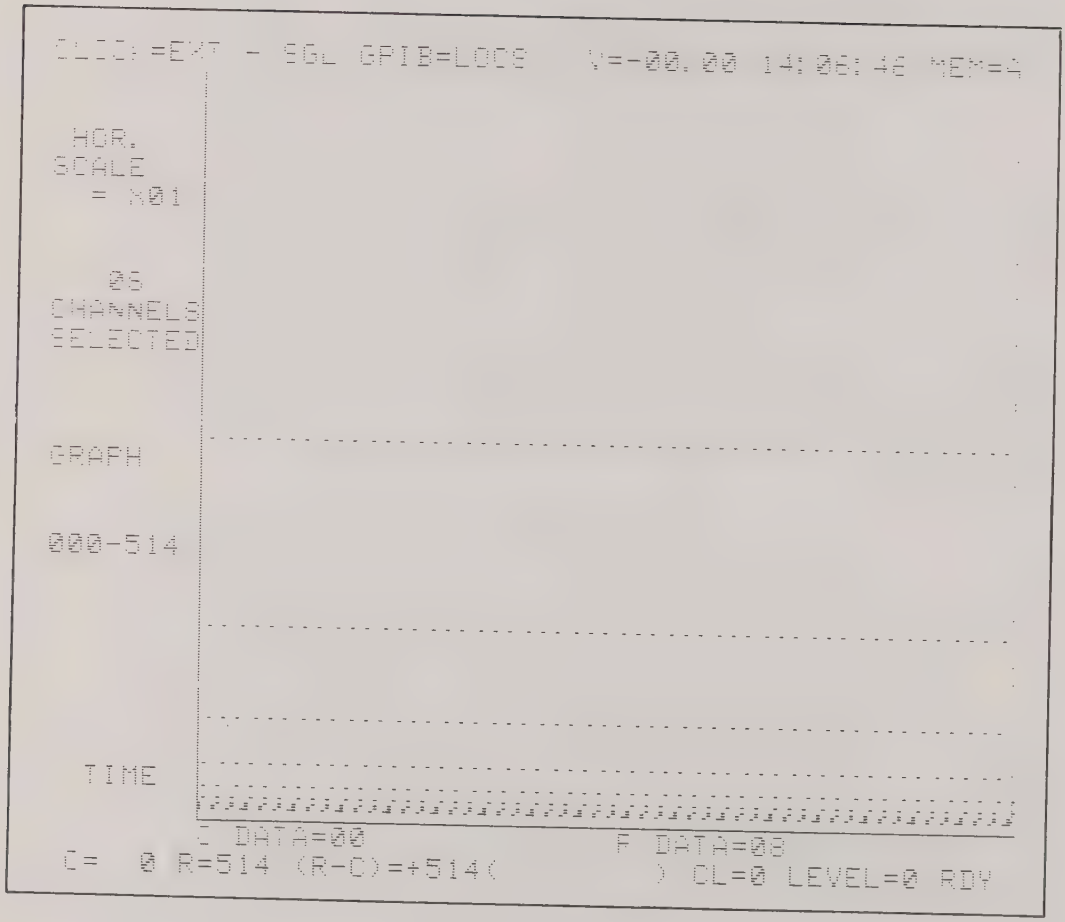


Figure 10-14. Change of Input Channel Graphed.

10.2.3.2 **Repeat Inputs**

REVIEW: Change the data format to look at inputs AF through A8 in binary as well as hex by the following procedure:

Press [DATA FORMAT], [▽ SET], [▷], twice, [INSERT], [▷],

[BINARY B R B], [ASCII A Q A], [DEMUX F V HEX], [BINARY B R B], [ASCII A Q A], [LATCH E U OCTAL],

[BINARY B R B], [ASCII A Q A], [GLITCH D T DECIMAL], [BINARY B R B], [ASCII A Q A], [SAMPLE C S],

[BINARY B R B], [ASCII A Q A], [BINARY B R B], [BINARY B R B], [ASCII A Q A], [ASCII A Q A],

[BINARY B R B], [ASCII A Q A], [EBCDIC 9 P ECL], [BINARY B R B], [ASCII A Q A], [PAGE↑ 8 O TTL].

The new data format should now look like Figure 10-15. The same inputs may be viewed in more than one radix. In Figure 10-15, AF through A8 are displayed in both hex and binary.

Display the reformatted information.

Press [DATA]. See Figure 10-16 which shows the corresponding data display for the data format of Figure 10-15. The binary representation of each hex word is clearly seen.

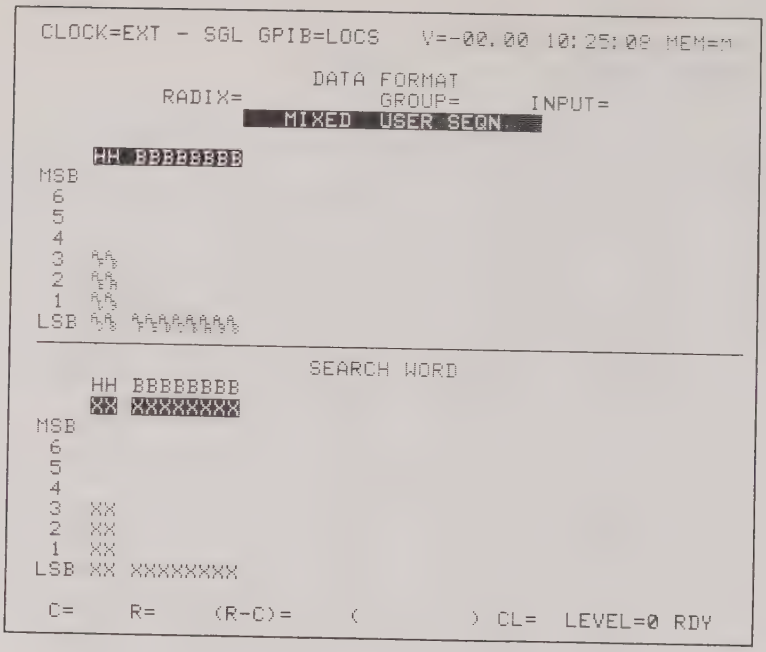


Figure 10-15. AF through A8 Displayed In Both Hex and Binary.

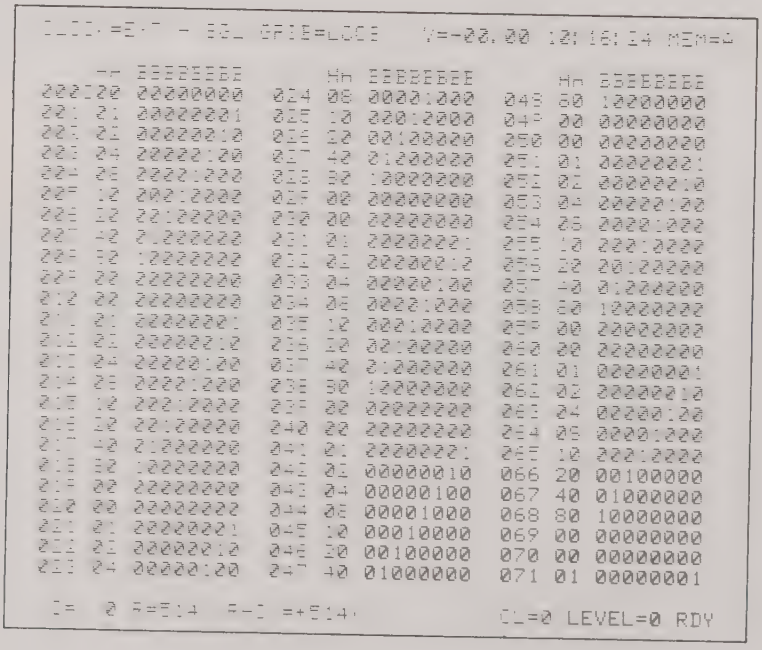


Figure 10-16. Data Display for Figure 10-15.

10.2.3.3 **Fixed Format**

REVIEW: Display the fixed binary format.

Press [DATA FORMAT], [Hx6 2'].

The display data should now look like Figure 10-17 which shows the same information viewed in a fixed binary format of all inputs CF through A0. Verify that only the first 14 binary columns (which are all zeros) are graphed.

Press [GRAPH] (see Figure 10-18) note that the graph of the first 14 columns of the fixed binary data display yields all zeros.

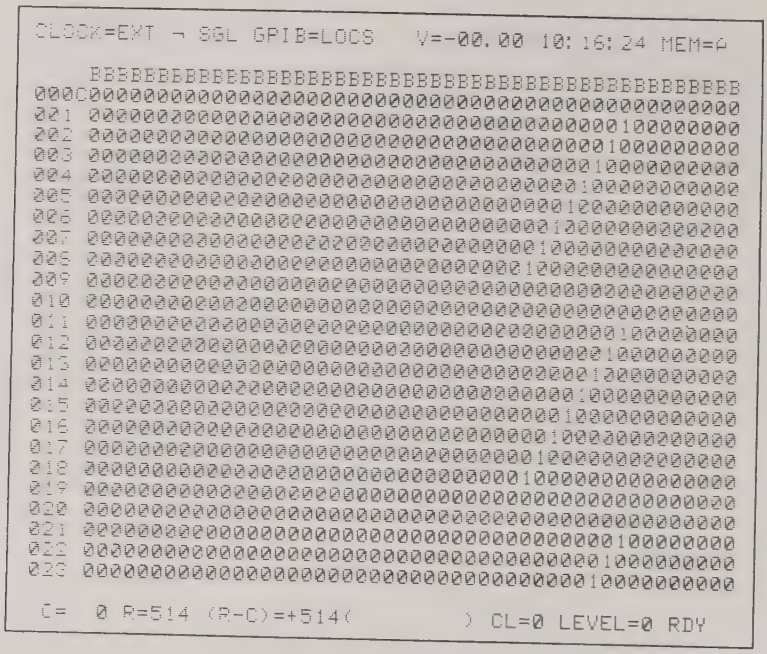


Figure 10-17. Fixed Binary Format, All Inputs CF through A0.

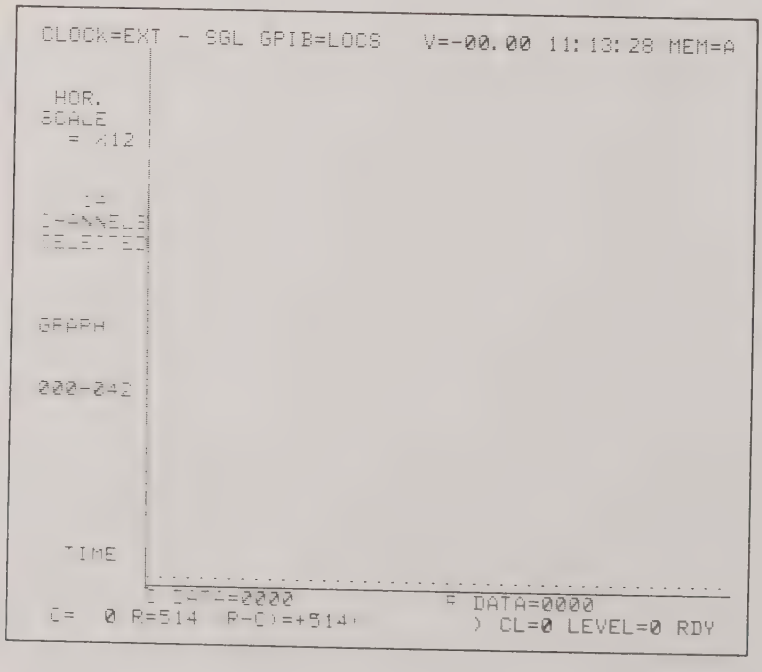


Figure 10-18. Graph First 14 Columns as Fixed Binary Data.

10.2.4 CLOCK AND INPUT

The Probe Test pattern generator produces two clock signals in addition to its eight data signals. The first clock signal is an external J clock input for the high order (F through 8) probe of each section, or an R enable input for the low order (7 through 0) probe of each section. The second clock signal is an external K clock input for the high order probe of each section, or an S enable input for the low order probe of each section. The actual time relationship between the clock and data signals is shown in Figure 10-19.

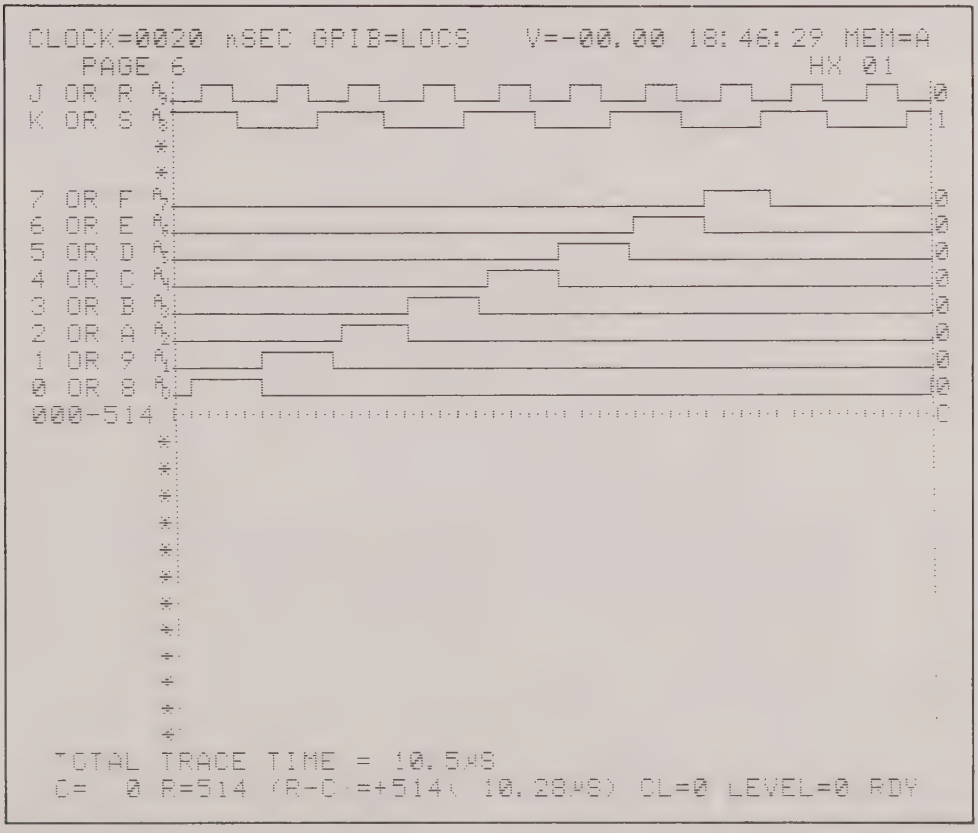


Figure 10-19. Time Relationship of Clock and Data Signals.

10.2.4.1 Sample Internally

SET UP: Take several samples of each pulse. See setup guide in Figure 10-20.

Modify Clock Select screen. Press [CLOCK SELECT] , [Hx1 0 G] ,
[SET ▽] , [Hx3 1 H] , [Hx1 0 G] , [Hx1 0 G] .

Display data format. Press [DATA FORMAT] , [Hx12 3 J] , [SET ▽] ,
[▷] twice, [SHIFT] , [DELETE] .

The Clock Select and Data Format displays should look like Figures 10-21 and 10-22.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 4.1 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AF AB
A T 2	AE AA
S 1	AD A9
LSB	AC A8

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
A. Four maximum commands in each level (one of each type)
Quick Key Commands
0 If DATA = D
1 Always
2 Never
3 If DATA = D and Sample Count > Delay
4 If DATA = D and Sample Count = Delay
5 If DATA = D and Sample Count < Delay
6 If DATA ≠ D and Sample Count > Delay
7 If DATA ≠ D and Sample Count = Delay
8 If DATA ≠ D and Sample Count < Delay
D = S, A = T (all four are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = DEC 515 (DEC/HEX) ___ (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

COMMENTS

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY

S = 0 1

(2) JUMP TO 0 (O-F) NEVER

J = X X

(2) ADVANCE NEVER

A = X X

(1) TRACE ALWAYS

T = X X

LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

COMMENTS

( ) STOP

S =

( ) JUMP TO ___ (O F)

J =

( ) ADVANCE

A =

( ) TRACE

T =

LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

COMMENTS

( ) STOP

S =

( ) JUMP TO ___ (O F)

J =

( ) ADVANCE

A =

( ) TRACE

T =

LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

COMMENTS

( ) STOP

S =

( ) JUMP TO ___ (O F)

J =

( ) ADVANCE

A =

( ) TRACE

T =

Figure 10-20. Set Up Internal Sampling (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 4.1 OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (0) MODE = INTERNAL

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = 100
- ■ NANOSECONDS (20-1600)
- □ MICROSECONDS (1-1600)
- □ MILLISECONDS (1-160)

MASTER = ■ INTERNAL □ EXT (_____●_____●_____) + (_____ + _____ + _____)

SECTION C = INT ■ SAME AS MASTER □ 10 NANOSECONDS; EXT □ SAME AS MASTER □ (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = INT ■ SAME AS MASTER □ 10 NANOSECONDS; EXT □ SAME AS MASTER □ (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = INT ■ SAME AS MASTER □ 10 NANOSECONDS; EXT □ SAME AS MASTER □ (_____●_____●_____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = (_____●_____●_____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence
1	OCTAL Fixed octal format & CF-A0 sequence
2	BINARY Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF-A0 SEQN Any radix fixed CF-A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE-816 attached OR
6	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the Internal clock rate. Section A > Section B > Section C + internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A > Section B > Section C + Master external
2	EXTERNAL MULT PHASED Each section can be sampled at an external rate or Master external rate. Section A, Section B, Section C & Master all can be different external frequencies
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, internal clock period, or 10x. Section A, Section B, and/or Section C = Master external or Internal clock period or 10x
4	MIXED MULT PHASED Master must be external. Each section can be sampled at its own external rate, the Master external rate, internal clock period or 10x. Section A, Section B, and Section C = Master external or Internal or 10x
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10x. Section A, Section B, and/or Section C = Internal clock period or 10x

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ (CURSORS C: 0-512, R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 10-20. Set Up Internal Sampling (Sheet 2 of 2).

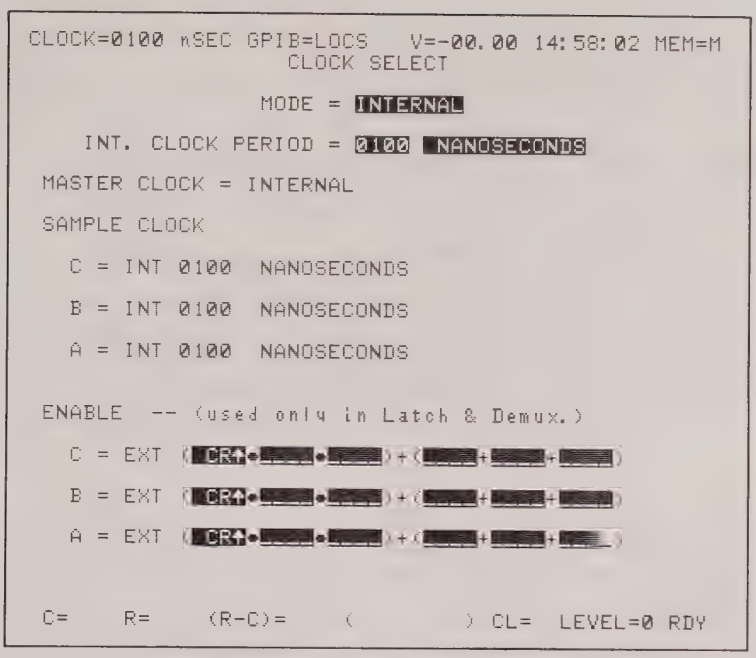

CLOCK=0100 nSEC GPIB=LOCS V=-00.00 14:58:02 MEM=M
CLOCK SELECT
MODE = INTERNAL
INT. CLOCK PERIOD = 0100 NANOSECONDS
MASTER CLOCK = INTERNAL
SAMPLE CLOCK
C = INT 0100 NANOSECONDS
B = INT 0100 NANOSECONDS
A = INT 0100 NANOSECONDS
ENABLE -- (used only in Latch & Demux.)
C = EXT
B = EXT
A = EXT
C= R= (R-C)= ( ) CL= LEVEL=0 RDY

Figure 10-21. Clock Select for Sample Internally.

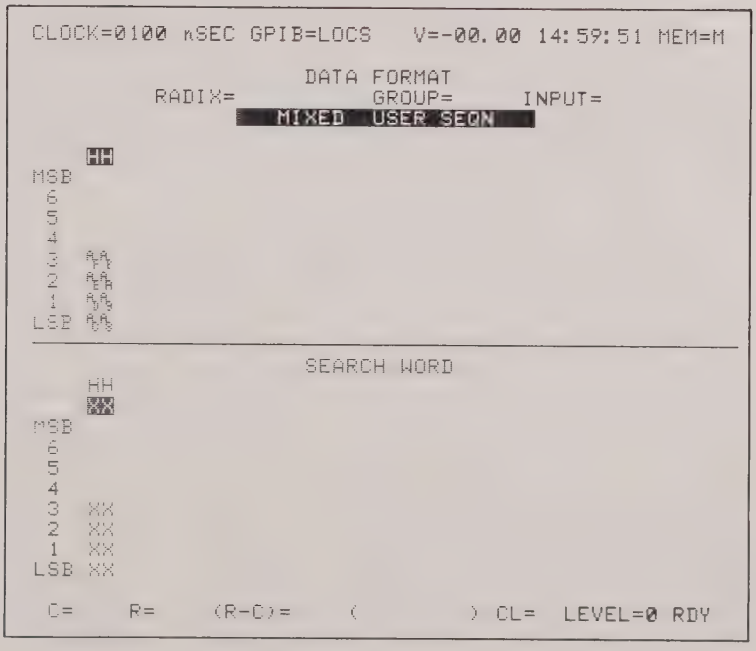


Figure 10-22. Data Format for Sample Internally.

RECORD: Press ARM .

REVIEW: Display the timing screen. Press TIMING , Hx1 0 G ,
PAGE 4 K to page 4.

The display should look like Figure 10-23. Each pulse is 0.9 microseconds (nine samples) wide ±100 nS (one sample). Confirm this with the cursors.

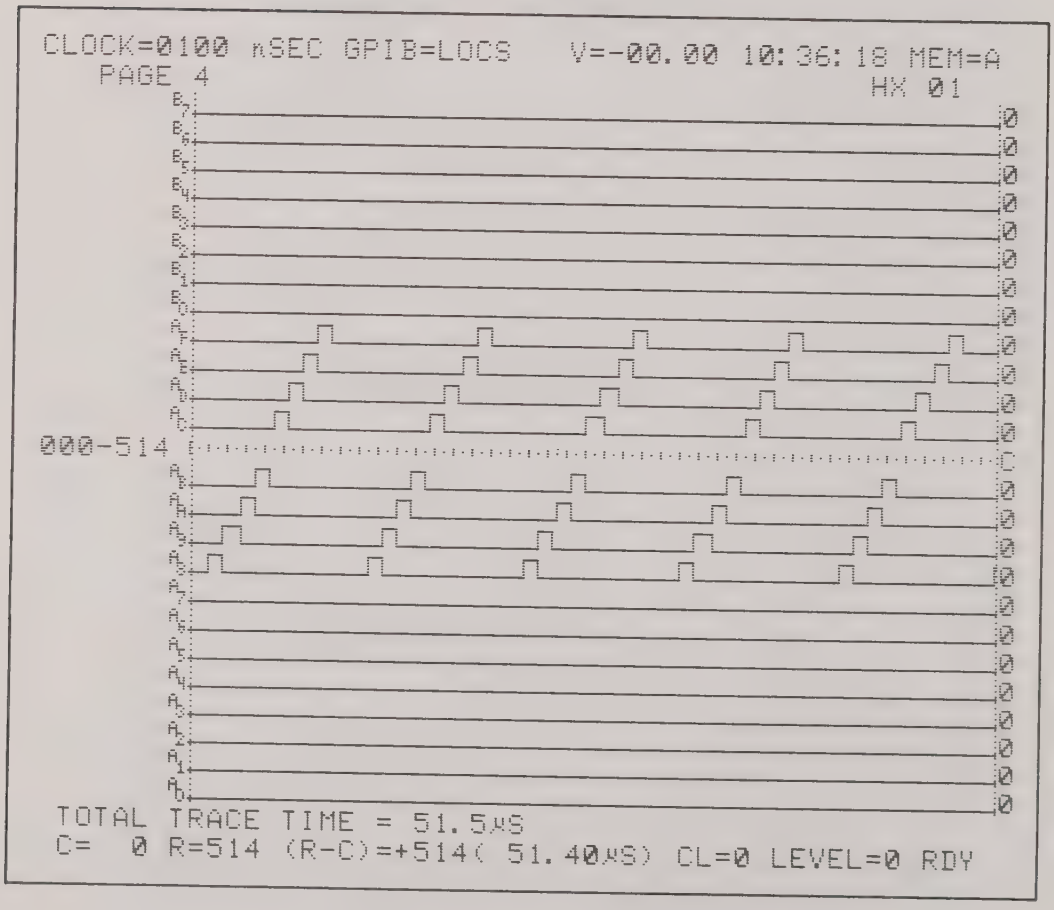


Figure 10-23. Pattern Asynchronously Sampled Every 100 ns.

10.2.4.2 **Sample On A Single External Clock (AJ↑ or AJ↓)**

SET UP: The active sampling edge of AJ can be specified as either rising or falling. Since both edges of each AJ pulse occur well within each input pulse (Figure 24a and 24b), it doesn't matter which edge is selected; the resulting recordings will be identical. In each case, one sample of each pulse will be taken. See the setup guide in Figure 10-25.

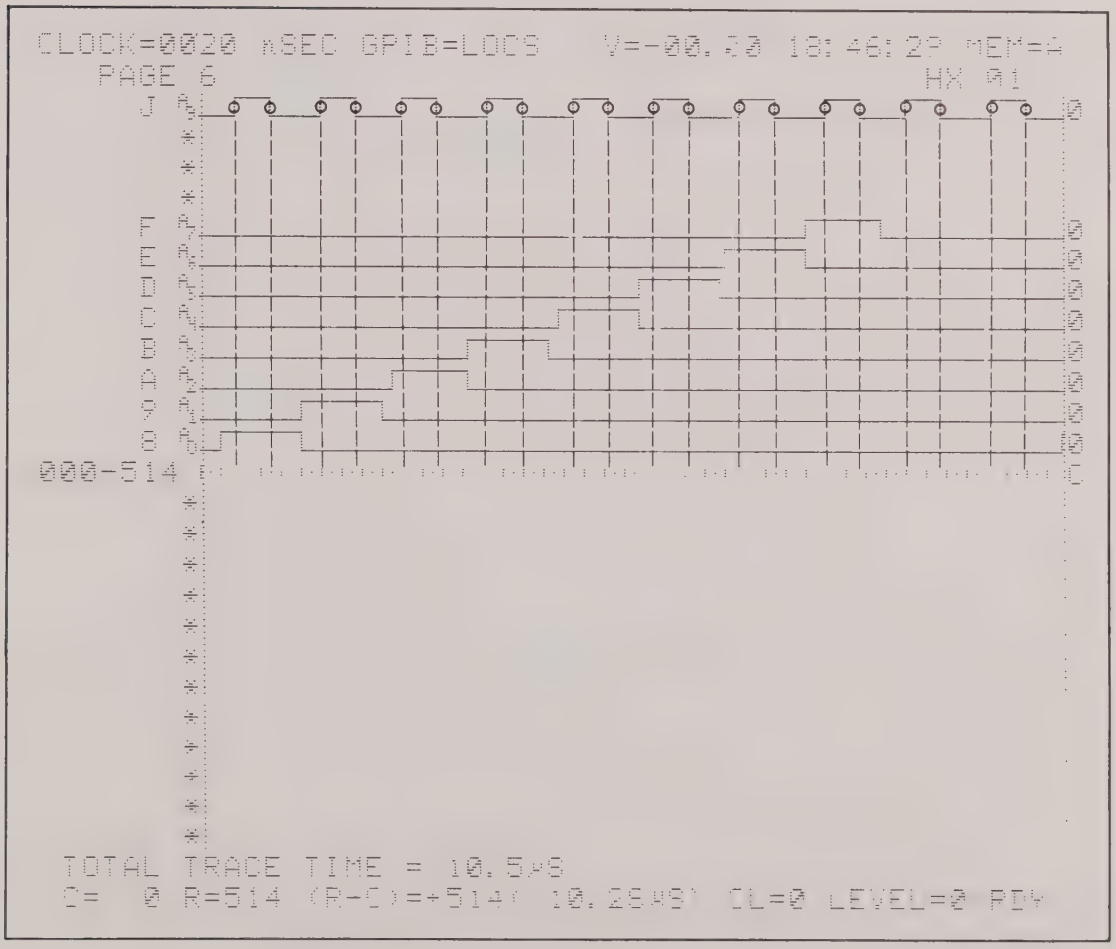


Figure 10-24. Sample Clock = AJ↑.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #4.2a OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AE A8
A T 2	AE AA
S 1	AD A9
LSB	AC A6

RADIX CHOICES. (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four of the commands in each level can come true on any of the preceding lines

Quick Key — Command Condition

0 If DATA = D
1 Always
2 Never
3 If DATA = D and Sample Count = Delay
4 If DATA ≠ D and Sample Count = Delay
5 If DATA = D and Sample Count > Delay
6 If DATA ≠ D and Sample Count > Delay
7 If DATA = D and Sample Count < Delay
8 If DATA ≠ D and Sample Count < Delay

(D = S, J, A, or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (QUICK KEY, O-F) DELAY = DEC 515 (DEC/HEX, 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = 0 1

(2) JUMP TO 0 (O F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

LEVEL ___ (QUICK KEY, O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

LEVEL ___ (QUICK KEY, O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

LEVEL ___ (QUICK KEY, O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

Figure 10-25. Setup Sample, Single External Clock (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 4.2a OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↑) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF - AO sequence
1	OCTAL Fixed octal format & CF AO sequence
2	BINARY Fixed binary format & CF AO sequence
3	MIXED USER SEQN Any radix any sequence
4	MIXED CF AO SEQN Any radix fixed CF AO sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format only if RTE 816 attached OR
6	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— —) NOT USED

QUICK KEY — MODE & DESCRIPTIONS

B INTERNAL

EXTERNAL SINGLE PHASE

EXTERNAL MULTI PHASE

8 MIXED MULTI PHASE

9 MIXED MULTI PHASE

5 INTERNAL EXTENDED

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ (CURSORS C: 0-512 R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP A	±	±	±	±	±	±	±	±	—	—	—	—	—	—	—	—

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 10-25. Setup Sample, Single External Clock (Sheet 2 of 2).

Change Clock Select display to show the following:

MASTER CLOCK = (__•__•__ AJ↑) + (__+__+__)

Press [CLOCK SELECT] , [Hx3 1 H] , [SET ▽] twice, [▷] twice, [Hx1 0 G] .

The Clock Select display should look like Figure 10-26 which shows clock select for setup AJ↑. Each subsequent push of [CLOCK SELECT] measures the external master sample clock frequency. . Note that if you press **CLOCK SELECT** a second time after setting it up, a reading of the external master clock frequency is displayed. Each press of **CLOCK SELECT** takes another frequency measurement.

RECORD: Press [ARM] .

REVIEW: Display the Timing screen.

Press [TIMING] , [Hx12 3 J] .

The display should look like Figure 10-27. Confirm that either active edge will create the same recording.

Press [A→B] , [CLOCK SELECT] , change active edges [SET ▽] twice, [▷] twice, [Hx3 1 H] , [ARM] , [DATA] , [COMPARE A/B] .

There should be no inequalities. Turn off the Comparison mode. Press [COMPARE A/B] .

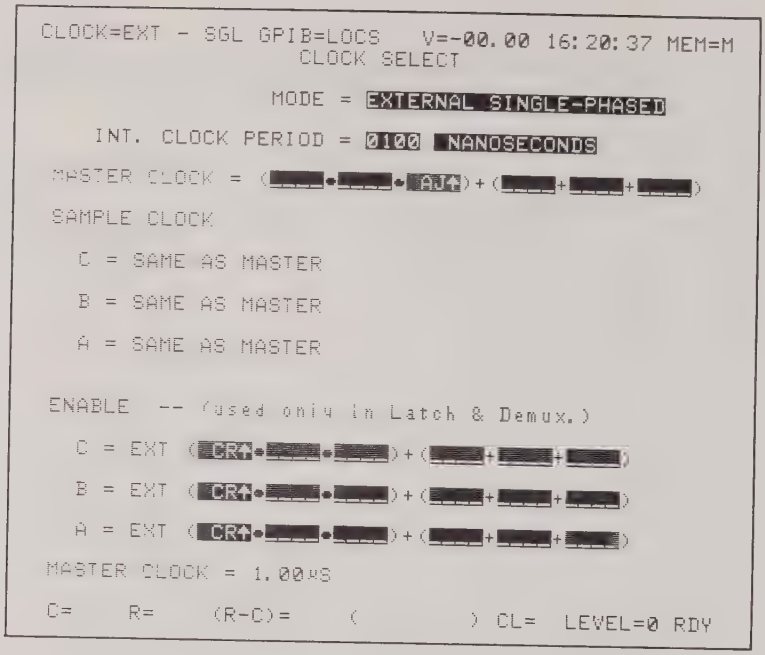

CLOCK=EXT - SGL GPIB=LOCS V=-00.00 16:20:37 MEM=M
CLOCK SELECT
MODE = EXTERNAL SINGLE-PHASED
INT. CLOCK PERIOD = 0100 NANOSECONDS
MASTER CLOCK = (• • AJ↑) + (+ +)
SAMPLE CLOCK
C = SAME AS MASTER
B = SAME AS MASTER
A = SAME AS MASTER
ENABLE -- (used only in Latch & Demux.)
C = EXT (CR↑ • •) + (+ +)
B = EXT (CR↑ • •) + (+ +)
A = EXT (CR↑ • •) + (+ +)
MASTER CLOCK = 1.00µS
C= R= (R-C)= ( ) CL= LEVEL=0 RDY

Figure 10-26. Clock Select for AJ↑.

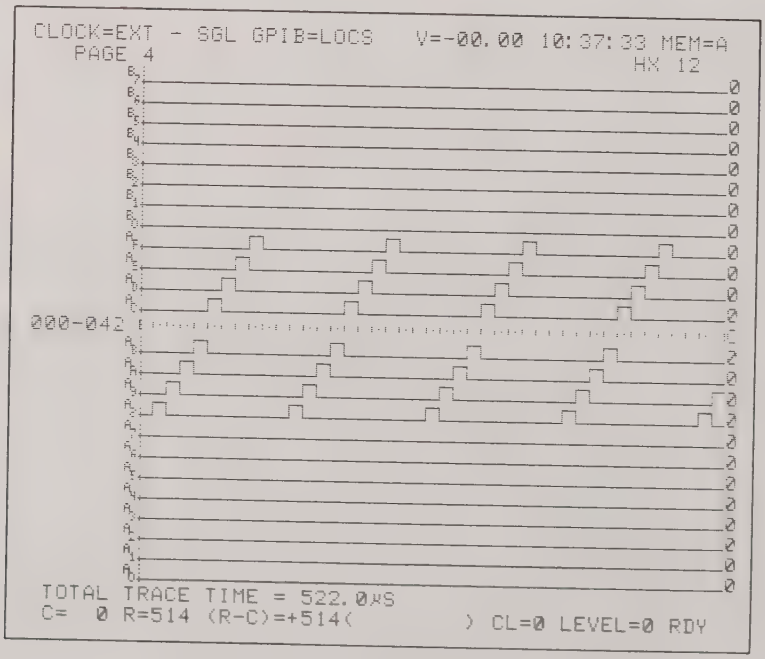


Figure 10-27. Recording for Sample Clock = AJ↑ or AJ↓.

10.2.4.3 **Sample on a Pair of External Clocks (AJ↓ and AK↑)**

SET UP: See setup guide in Figure 10-28.

A sample will be taken at each rising edge of the resultant sample clock which is created by combining AJ| and AK^ into a logical OR expression (Figure 10-29). Each odd-numbered input pulse is sampled once.

Change Clock Select display to the following:

MASTER CLOCK = (___•___• AJ↓) + (__ + __ + AK↑)

Change trace control to S = 02

Press [CLOCK SELECT], [▽ SET] twice, [▷] twice, [Hx3 1 H], [TRACE CONTROL], [▽ SET] twice, [Hx1 0 G], [Hx6 2 I].

RECORD: Press [ARM].

REVIEW: Display timing screen. Press [TIMING].

The display should look like Figure 10-30. See Figures 10-31 and 10-32 for clocking with AJ↑ + AK↓. For Figure 10-31, a sample is taken at each rising edge of the resultant sample clock. Each even numbered input pulse is sampled twice. See Figures 10-33 and 10-34 for clocking with AJ↓ and AK↓. For Figure 10-33, a sample is taken at each rising edge of the resultant sample clock. Each even-numbered input pulse is sampled once.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #436 OF ___ DATE _____

QUICK KEY (See back for notes) (3...) DATA FORMAT MIXED USER SEQN.

TRACE CONTROL NOTES

For each line:
TRACE = enter pattern, A, the "mask" value
STOP = comparison type, MAG
JUMP = enter level, NEVER, F
A = "mask" value, C = count, F
Q = NEVER, C = count, F, Mask

0 DATA D
1 A=A=X
2 N=X
3 = DATA D or Sample Count = Delay
4 = DATA + D or Sample Count = Delay
5 = DATA D and Sample Count = Delay
6 = DATA D and Sample Count = Delay
7 = DATA Q and Sample Count = D or F
8 = DATA Q and Sample Count = D or F
9 = DATA D and Sample Count = Delay

(D, S, J, A, or T which are specified in the type)

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AEAB
A T 2	AEAA
S 1	ADA9
LSB	ACA8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL

LEVEL 0 (O-F) DELAY = DEC 515 (DEC/HEX) CLOCKS (0-65 K) (CLOCKS/A PATTERNS) END LEVEL F (O-F)

COMMENTS

(3...) STOP IF DATA = 5 AND SAMPLE COUNT > DELAY
S = 0 2

(2...) JUMP TO 0 (O-F) NEVER
J = X X

(2...) ADVANCE NEVER
A = X X

(1...) TRACE ALWAYS
T = X X

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

COMMENTS

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

COMMENTS

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

COMMENTS

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

Figure 10-28. Setup Guide Sample on Pair of External Clocks (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF 4.3b DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+AK ↑)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence
1	OCTAL Fixed octal format & CF A0 sequence
2	BINARY Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF-A0 SEQN Any radix, fixed CF A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE-816 attached OR
5	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL
All sections are sampled at the internal clock rate
Section A = Section B = Section C = Internal clock period

1 EXTERNAL SINGLE PHASED
All sections are sampled at the Master external rate
Section A = Section B = Section C = Master external

2 EXTERNAL MULTI PHASED
Each section can be sampled at own external clock
Master = Internal rate, Section A, Section B, Section C
A, Master can be different external expressions

3 MIXED SINGLE PHASED
Master must be external. Each section can be sampled at the Master external rate, internal clock period, or 10ns
Master = external or internal or 10ns
Section A, Section B, and/or Section C: Master external or internal clock period or 10ns

4 MIXED MULTI-PHASED
Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period, or 10ns, Section A, Section B, and/or Section C
Master = external or internal or 10ns

5 INTERNAL EXTENDED
Each section can be sampled at the internal clock rate or 10ns, Section A, Section B, and/or Section C
Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ (CURSORS C: 0-512, R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A < B WITHIN LIMITS
5	AUTO STOP IF A > B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP B	↑	↑	↑	↑	↑	↑	↑	↑	—	—	—	—	—	—	—	—
GROUP A	↑	↑	↑	↑	↑	↑	↑	↑	—	—	—	—	—	—	—	—

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 10-28. Setup Guide Sample on Pair of External Clocks (Sheet 2 of 2).

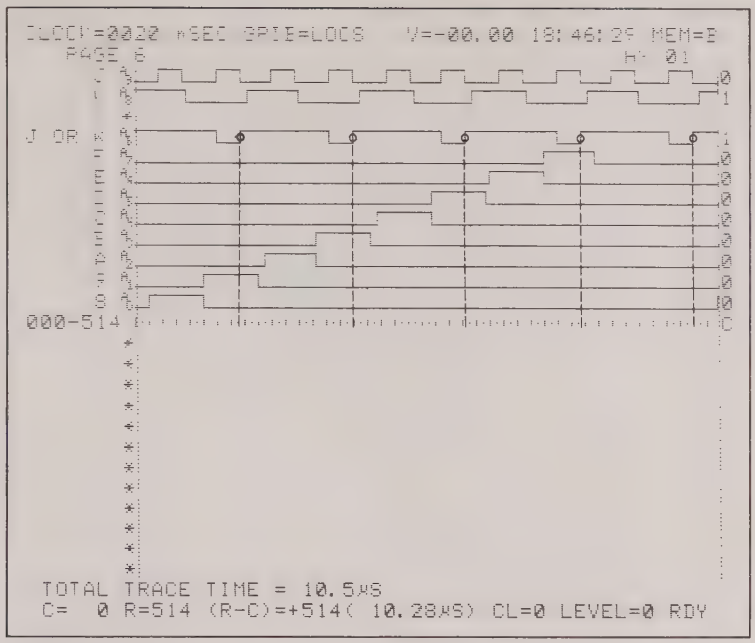


Figure 10-29. Sample Clock = AJ↓ + AK↑.

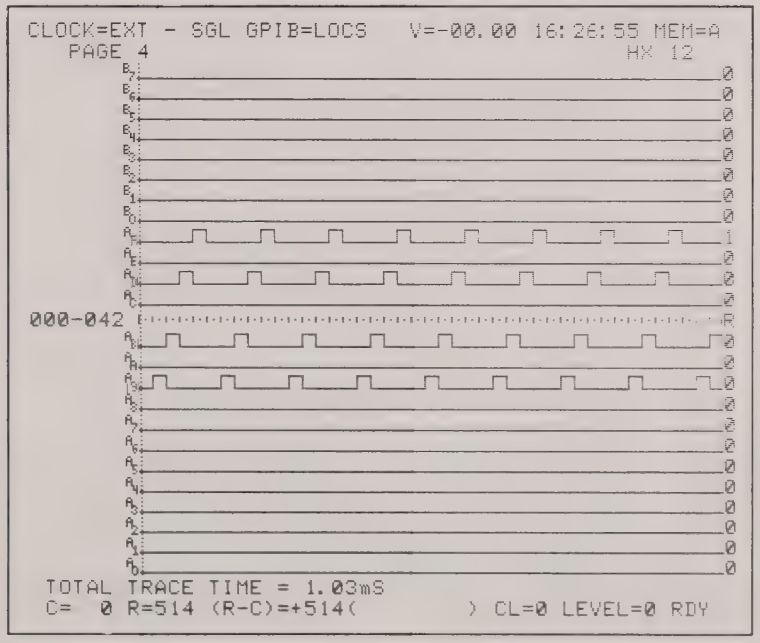


Figure 10-30. Recording for Sample Clock = AJ↓ + AK↑.

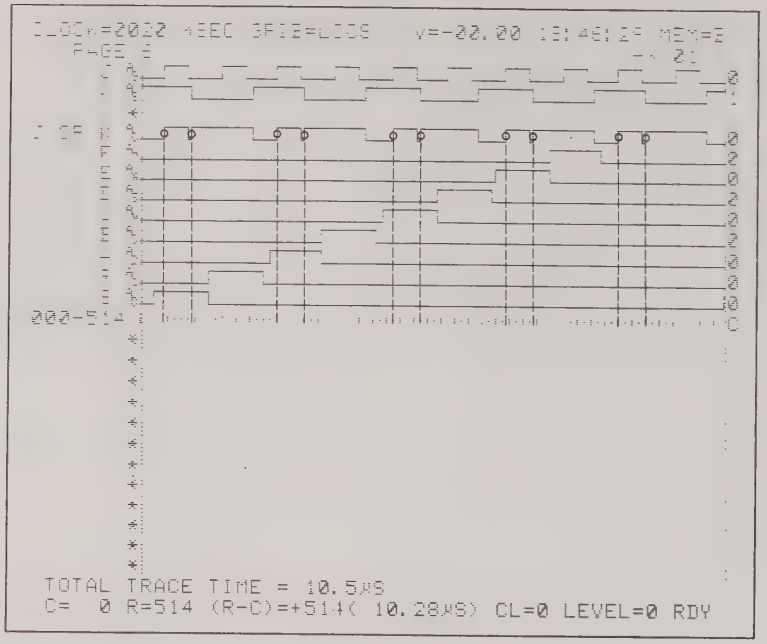


Figure 10-31. Sample Clock = AJ↑ + AK↓.

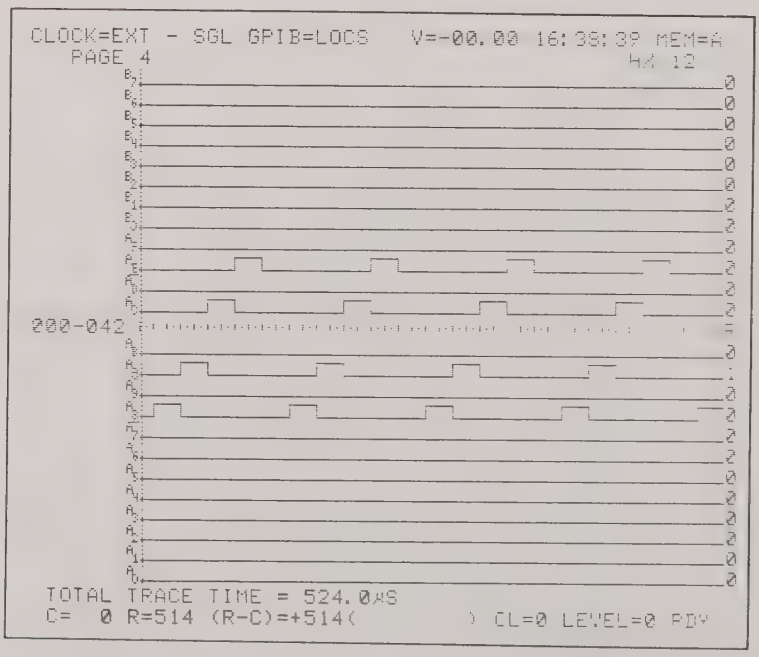


Figure 10-32. Recording for Sample Clock = AJ↑ + AK↓.

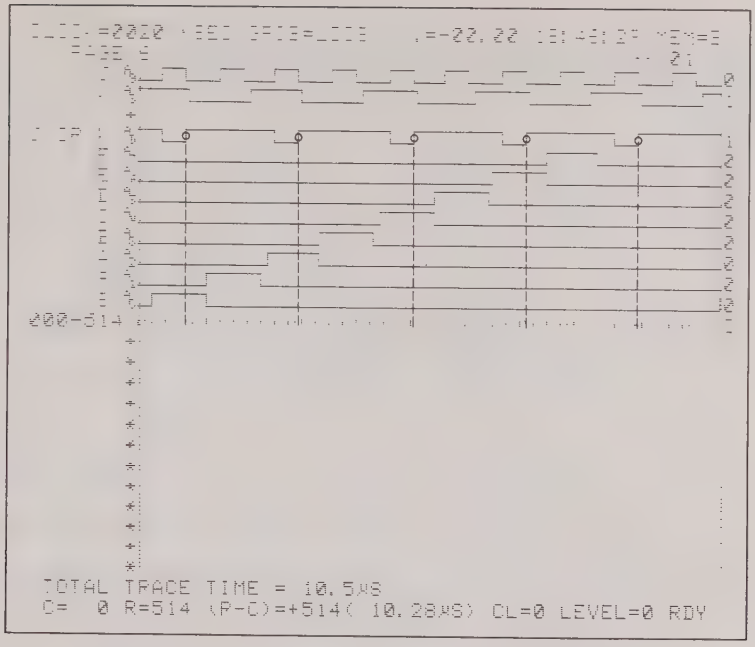


Figure 10-33. Sample Clock = AJ↓ + AK↓.

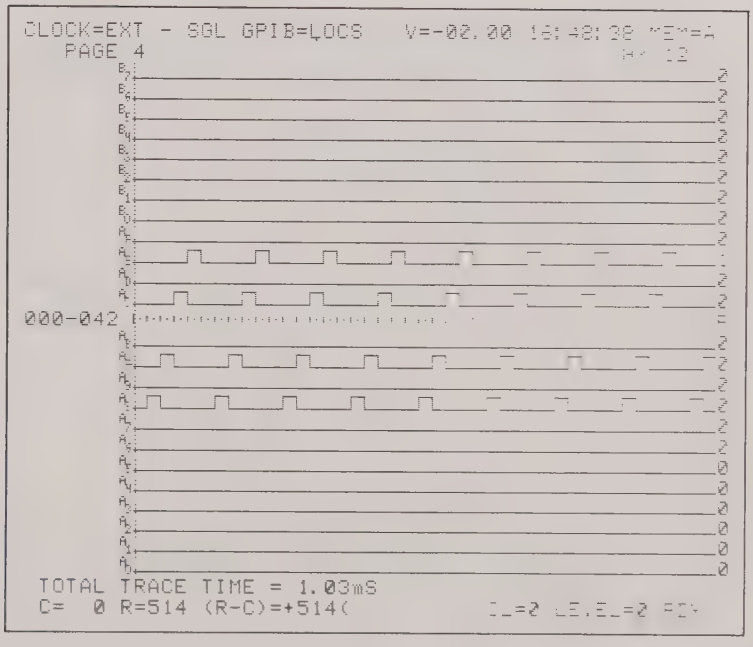


Figure 10-34. Recording for Sample Clock = AJ↓ + AK↓.

10.2.4.4 **Latch (Enable) on a Single Input (AR↑, AR↓)**

SET UP: See setup guide in Figure 10-35. Disconnect the AF through A8 probe from PROBE TEST connector and connect the A7 through A0 probe. Display page 6 of the Timing screen.

Press TIMING , PAGE ↓ 4 K twice.

Inputs are held at the levels that exist when the latch enable signal goes false, then are released to be able to change when the signal is true. All transitions occur while the inputs are latched and, therefore, change synchronously with AR↑ going high. The latched inputs are then asynchronously sampled.

The inputs are latched while AR↑ is false (low) and released while it is true (high). Every transition is latched; therefore, all the inputs change synchronously with the rising edge of AR↑ (see Figure 10-36).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 44a OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3 A7 A3
A T 2 A6 A2
S 1 A5 A1
LSB A4 A0

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions:

Quick Key	Command Condition	
0	If DATA = D	
1	Always	
2	Never	
3	If DATA = D and Sample Count >	Delay
4	If DATA ≠ D and Sample Count >	Delay
5	If DATA = D and Sample Count =	Delay
6	If DATA ≠ D and Sample Count =	Delay
7	If DATA = D and Sample Count <	Delay
8	If DATA ≠ D and Sample Count <	Delay

(D = S, J, A, or T, which are assigned by command type.)

TRACE CONTROL

QUICK KEY — LEVEL 0 (O-F) DELAY = DEC 515 (DEC/HEX, 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F) — COMMENTS

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = 0 1

(2) JUMP TO 0 (O F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX, 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX, 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX, 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F) — COMMENTS

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

Figure 10-35. Setup Latch (Enable) on a Single Input (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #44a OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (0) MODE = INTERNAL

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = 40

■ NANOSECONDS (20-1600)
□ MICROSECONDS (1-1600)
□ MILLISECONDS (1-160)

MASTER = ■ INTERNAL □ EXT (_____●_____●_____) + (_____+_____+_____)

SECTION C = INT ■ SAME AS MASTER □ 10 NANOSECONDS
EXT □ SAME AS MASTER □ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ■ SAME AS MASTER □ 10 NANOSECONDS
EXT □ SAME AS MASTER □ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ■ SAME AS MASTER □ 10 NANOSECONDS
EXT □ SAME AS MASTER □ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●AR ↑) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence
1	OCTAL Fixed octal format & CF A0 sequence
2	BINARY Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF A0 SEQN Any radix, fixed CF A0 sequence
5	DEVICE MNEMONICS Fixed disassembled μP code format, only if RTE-B18 attached OR
6	DEVICE NOT AVAILABLE No RTE B18 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— —) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A = Section B = Section C = Internal clock period
1	EXTERNAL, SINGLE PHASE All sections are sampled at the Master external clock rate Section A = Section B = Section C = Master external
2	EXTERNAL, MULTI-PHASED Each section is independently sampled at the external clock rate Master external = Section A, Section B, or Section C & Master external/internal relative requirements
3	MIXED, SINGLE PHASE Master clock is internal, Section A or B is sampled at the Master internal clock rate Master external = Section A or Section B = Master external & Section B or Section A = Master external/internal relative requirements
4	MIXED, MULTI-PHASE Master clock is internal, Section A or B is sampled at the Master internal clock rate Master external = Section A or Section B = Master external & Section B or Section A = Master external/internal relative requirements
5	INTERNAL, EXTERN Each section is independently sampled at the external clock rate Section A = Section B = Section C = Internal clock period

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	LATCH	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
·	A [illegible]
·	[illegible]
1	AUTO STOP IF A ↑ B
4	AUTO STOP IF A ↑ B WITHIN L M
5	AUTO STOP IF A ↓ B WITHIN L M

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP A	±	±	±	±	±	±	±	±	±	±	±	±	±	±	±	±

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12 5183

Figure 10-35. Setup Latch (Enable) on a Single Input (Sheet 2 of 2).

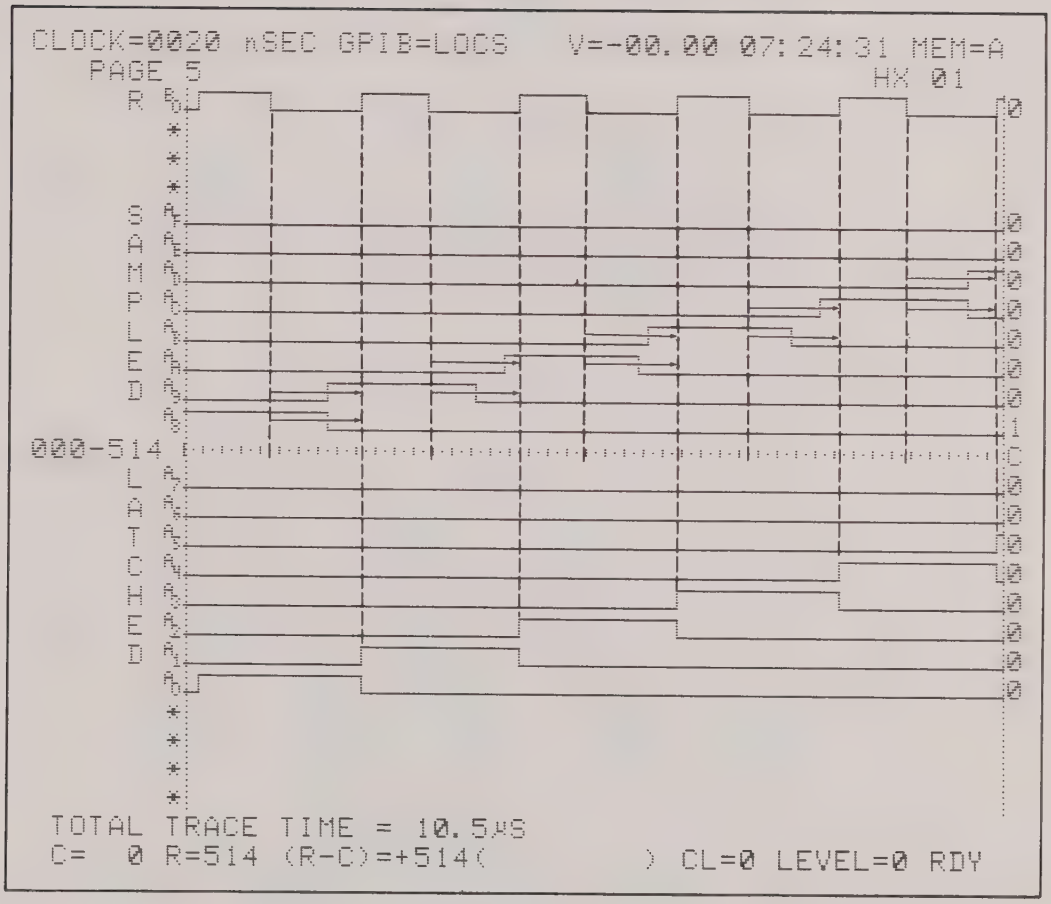


Figure 10-36. Enable = AR↑.

Set up the Clock Select screen.

Press [CLOCK SELECT] , [Hx1 0 G] , [▽ SET] , [PAGE 4 K] , [Hx1 0 G] , [▽ SET] three times, [Hx6 2 I] , [▷] twice, [Hx1 0 G] .

Display the Input Mode screen.

Press [INPUT MODE] , [△] twice, [LATCH E OCTAL U] , [▷] , [EBCDIC 9 ECL P] .

Display the Data Format screen.

Press [DATA FORMAT] , [▽ SET] twice, [ASCII A A Q] , [V6 7 N] , [ASCII A A Q] , [V12 6 M] , [ASCII A A Q] , [V24 5 L] , [ASCII A A Q] , [PAGE 4 K] , [▽ SET] , [ASCII A A Q] , [Hx12 3 J] , [ASCII A A Q] , [Hx6 2 I] , [ASCII A A Q] , [Hx3 1 H] , [ASCII A A Q] , [Hx1 0 G] .

Display Trace Control screen.

Press [TRACE CONTROL] , [▽ SET] twice, [Hx1 0 G] , [Hx3 1 H] .

Clock Select and Input Mode screens should look like Figures 10-37 and 10-38.

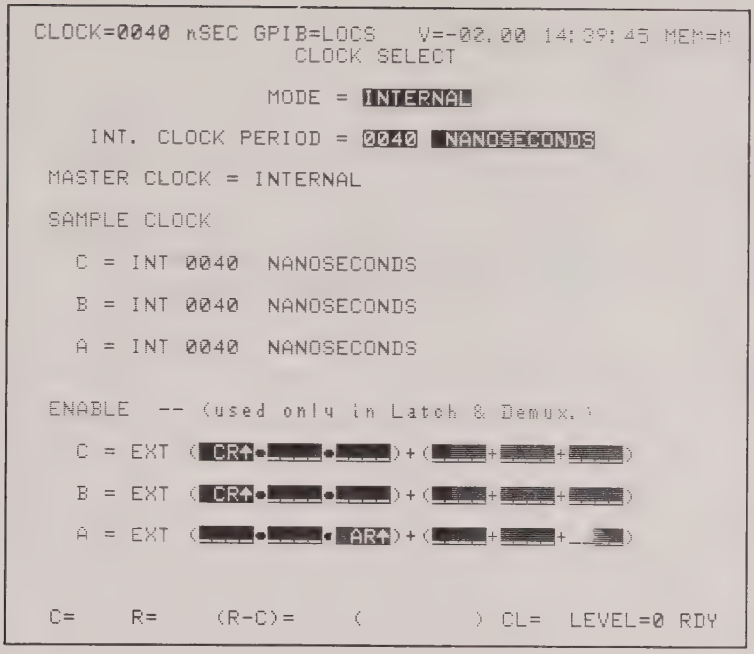

CLOCK=0040 nSEC GPIB=LOCS V=-00.00 14:39:45 MEM=M
CLOCK SELECT
MODE = INTERNAL
INT. CLOCK PERIOD = 0040 NANOSECONDS
MASTER CLOCK = INTERNAL
SAMPLE CLOCK
C = INT 0040 NANOSECONDS
B = INT 0040 NANOSECONDS
A = INT 0040 NANOSECONDS
ENABLE -- (used only in Latch & Demux.)
C = EXT (CR↑ • ____ • ____) + (____ + ____ + ____)
B = EXT (CR↑ • ____ • ____) + (____ + ____ + ____)
A = EXT (____ • ____ • AR↑) + (____ + ____ + ____)
C= R= (R-C)= ( ) CL= LEVEL=0 RDY

Figure 10-37. Clock Select for Enable = AR↑.

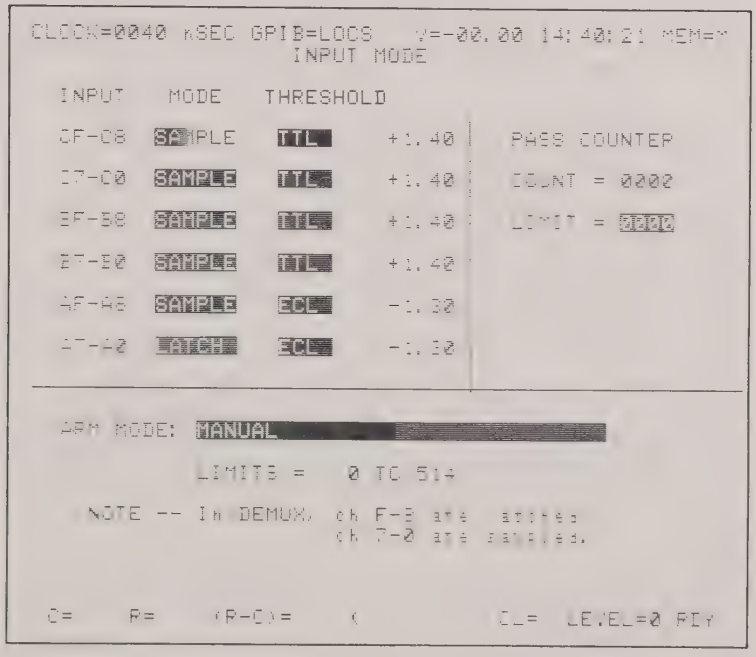

CLOCK=0040 nSEC GPIB=LOCS V=-00.00 14:40:21 MEM=M
INPUT MODE
INPUT MODE THRESHOLD
CF-C8 SAMPLE TTL +1.40
C7-C0 SAMPLE TTL +1.40
BF-B8 SAMPLE TTL +1.40
B7-B0 SAMPLE TTL +1.40
AF-A8 SAMPLE ECL -1.30
A7-A0 LATCH ECL -1.30
PASS COUNTER
COUNT = 0002
LIMIT = 0000
ARM MODE: MANUAL
LIMITS = 0 TO 514
NOTE -- In DEMUX, ch F-8 are strobes
ch 7-0 are samples.
C= R= (R-C)= (CL= LEVEL=0 RDY

Figure 10-38. Input Mode for Latch on Single Input.

RECORD: Press [ARM] .

REVIEW: Display the Timing screen. Press [TIMING] .

The display should look like Figure 10-39. Note that all transitions now occur synchronously.

SET UP: When AR↓ is used, the inputs are latched while AR↓ is false (high) and released while it is true (low). Since the latching occurs totally within each pulse (i.e., no input signal transitions occur during the latch period), the latch signal has no effect on the inputs (see Figure 10-40).

Change the Clock Select display to the following:

ENABLE A = EXT (__·__· AR↓) + (__+__+__)

Press [CLOCK SELECT] , [▽ SET] four times, [▷] twice, [Hx3 1 H] .

RECORD: Press [ARM] .

REVIEW: Press [TIMING] .

When AR↓ is used this display should look like Figure 10-41. Note that the transitions are asynchronous.

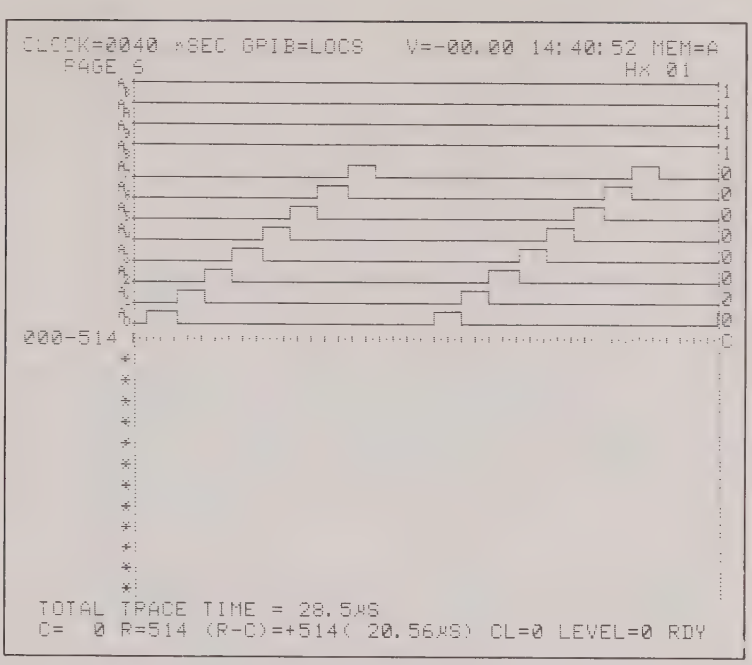


Figure 10-39. Recording of Asynchronously Sampled Latched Inputs for Enable = AR↑.

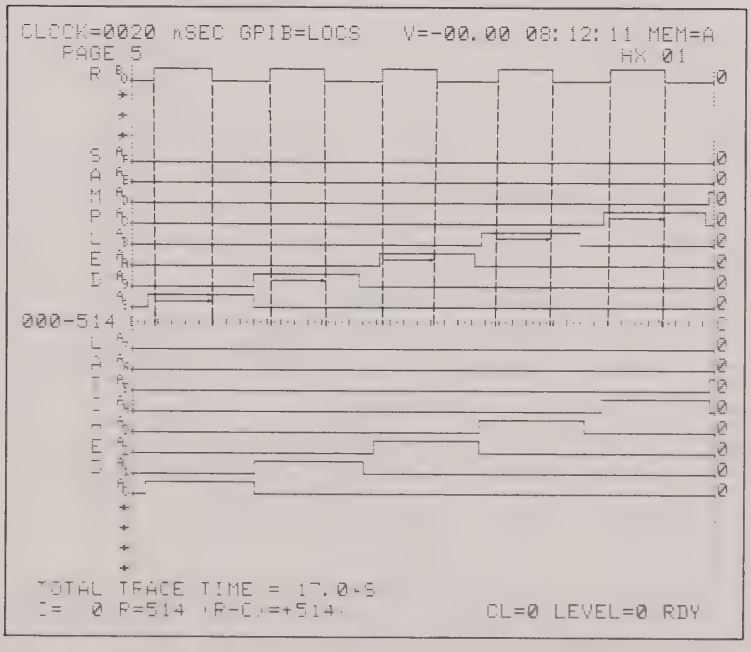


Figure 10-40. Function of Input Signal Transitions Latch Enable Signal.

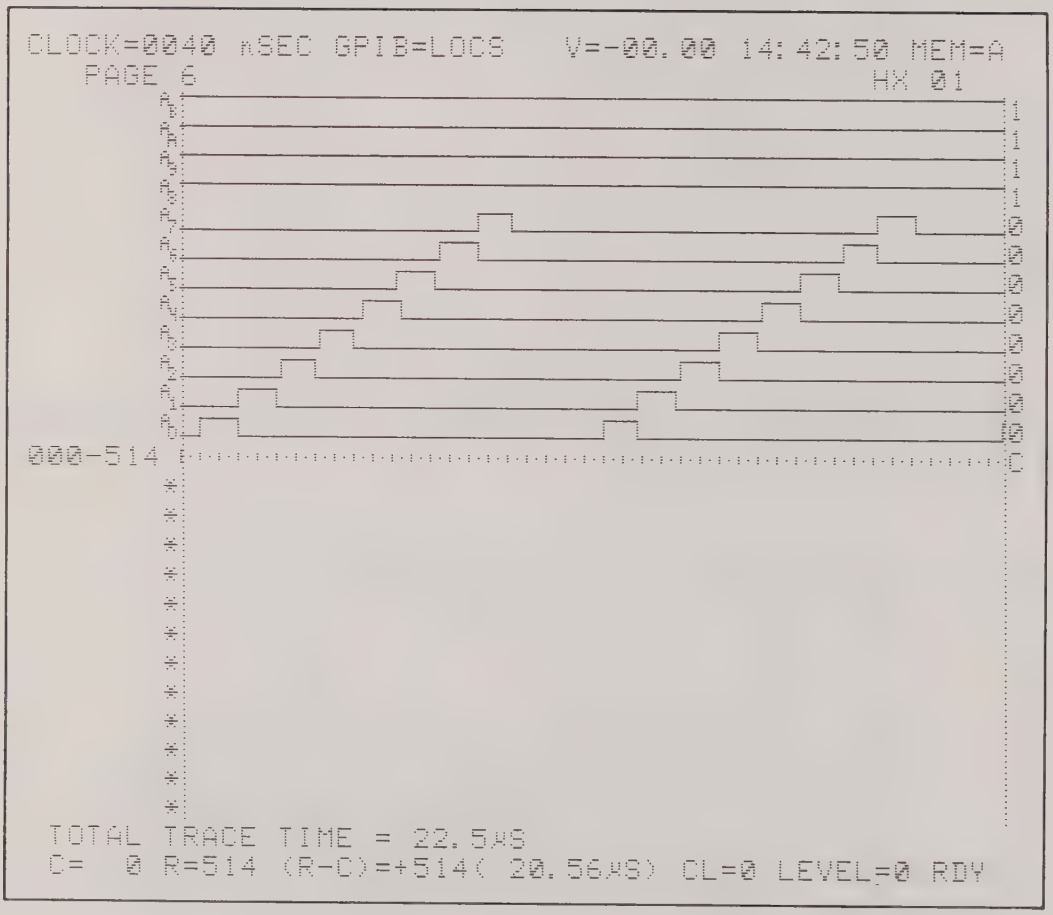


Figure 10-41. Recording for Enable = AR↓.

SET UP: When AS↑ is used the inputs are latched while AS↑ is false (low) and released while it is true (high). Every other transition is latched (see Figure 10-42). Note that every other input transition occurs during a latched period and, therefore, cannot change until enable returns to true.

When AS↑ is used the Timing display should look like Figure 10-43. Note that every other transition is synchronous.

SET UP: When AS↓ is used the inputs are latched while AS↓ is false (high) and released while it is true (low). Every other transition is latched (see Figure 10-44) or every other input transition AS↓ occurs during a latched period and, therefore, cannot change until enable returns to true.

When AS↓ is used the Timing display should look like Figure 10-45.

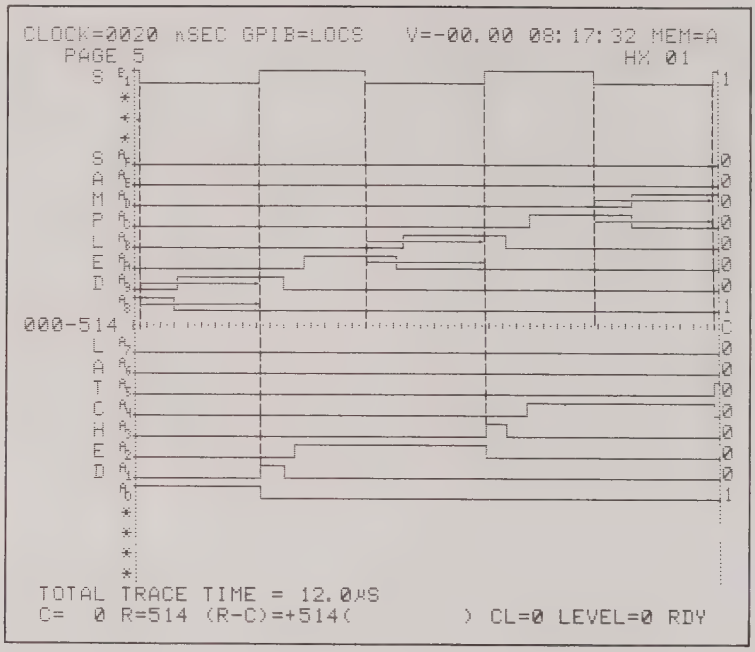


Figure 10-42. Enable = AS↑ Every Other Transition Latched.

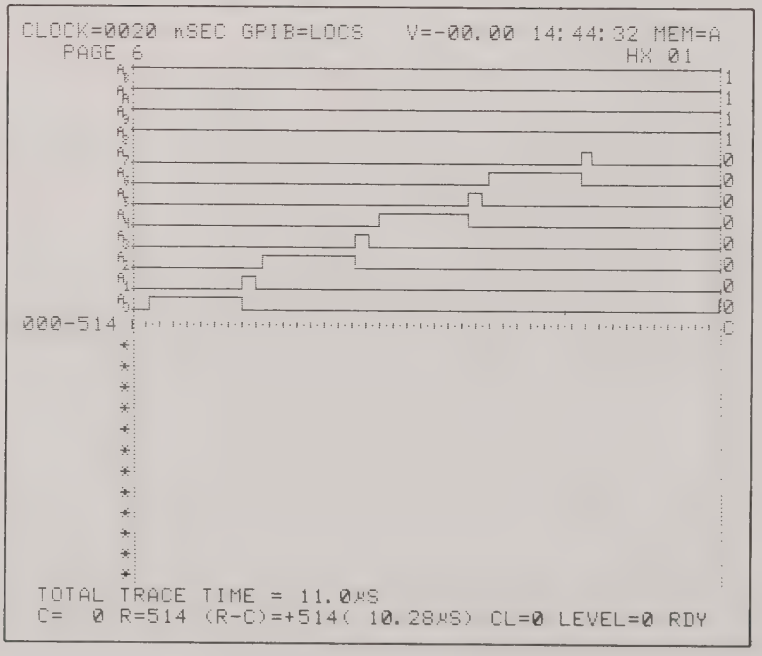


Figure 10-43. Time Recording for Enable = AS↑.

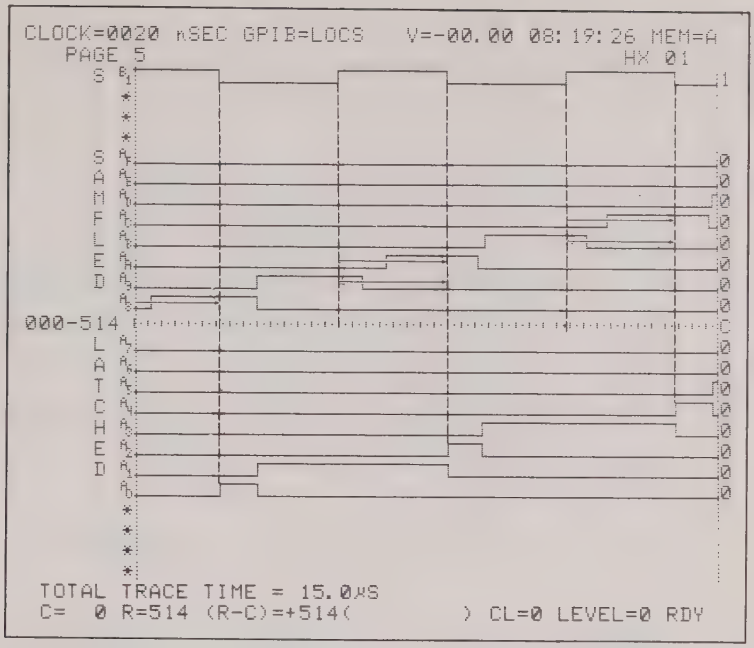


Figure 10-44. Enable = AS↓, Inputs Latched When AS↓ True.

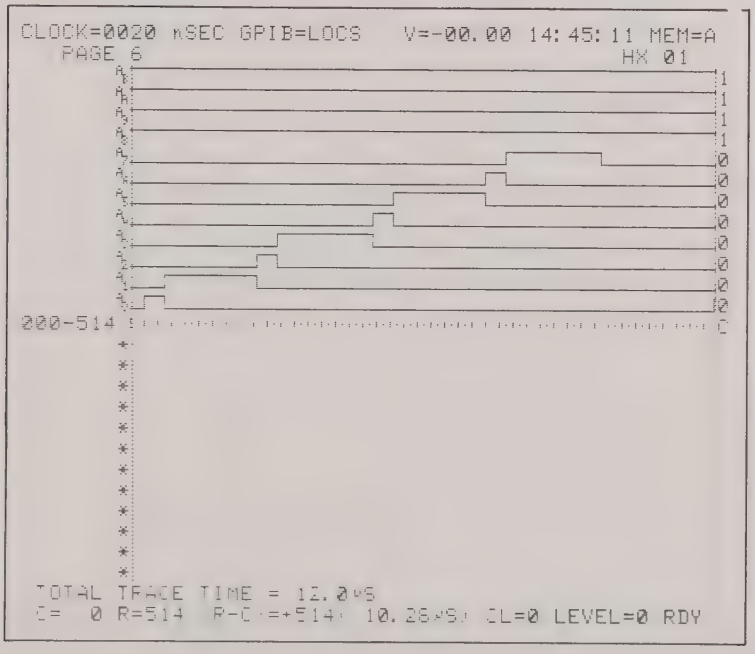


Figure 10-45. Recording for Enable = AS↓.

10.2.4.5 Latch (Enable) on a Combination of Inputs (AR↑ + AS↑, AR↓ + AS↑, AR↑ + AJ↓, AR↓ + AJ↓)

SET UP: The latch enable signal is created by combining AR^ and AS| into a logical OR expression. The inputs are latched while the resultant signal is false and released while it is true. Every other transition is latched (see Figure 10-46). Every other input transition occurs during a latched period and, therefore, cannot change until the enable expression becomes true.

Change Clock Select display to the following:

ENABLE A = EXT (__•__• AR↑) + (__+__+ AS↑)

Press CLOCK SELECT, ▽ SET four times, ▷ twice, Hx1 0 G, ▷ three times, Hx1 0 G.

RECORD: Press ARM.

REVIEW: Display the Timing screen. Press TIMING.

The display should look like Figure 10-47.

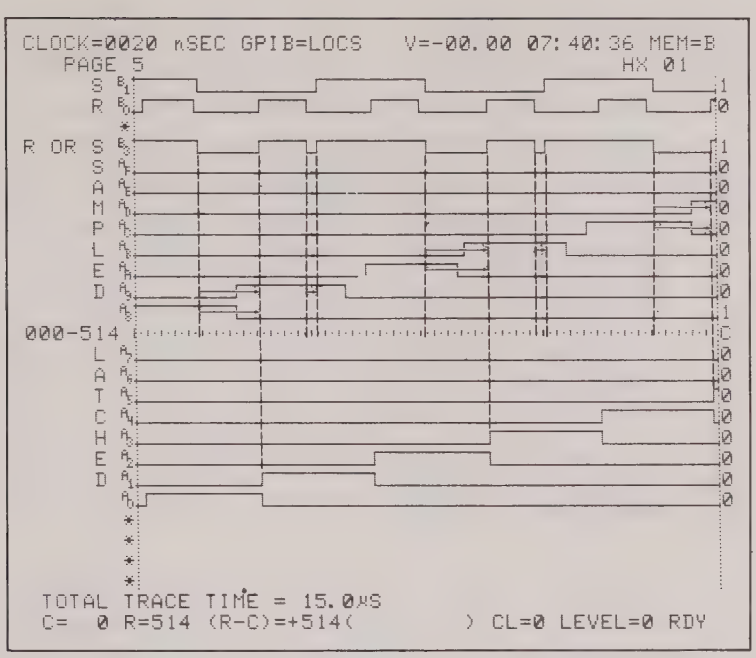


Figure 10-46. Enable = AR↑ + AS↑.

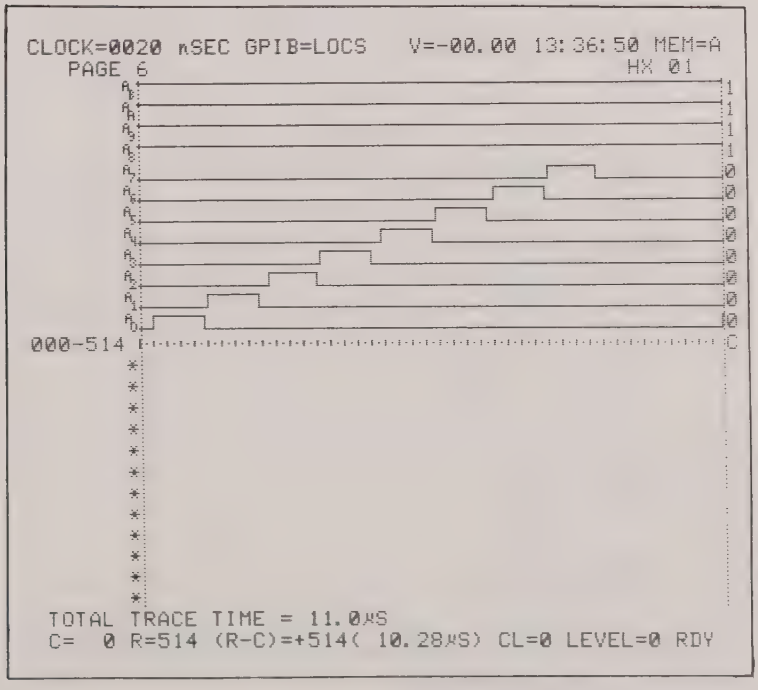


Figure 10-47. Recording for Enable = AR↑ + AS↑.

SET UP: When AR↓ + AS↑ is used, the latch enable signal is created by combining AR↓ and AS↓ into a logical OR expression. The inputs are latched while the resultant enable signal is false and released while it is true. Since latching occurs totally within every other pulse, the latch signal has no affect on the inputs (see Figure 10-48). No input transitions occur during a latched period; therefore, the Enable expression has no affect on the inputs.

When AR↓ + AS↑ is used, the Timing display should look like Figure 10-49.

SET UP: When AR↑ + AS↓ is used the latch enable signal is created by combining AR↑ and AS↓ into a logical OR expression. The inputs are latched while the resultant signal is false and released while it is true. Latching occurs at every other transition (see Figure 10-50). Note that every other input transition occurs during a latched period and, therefore, cannot change until enable becomes true.

Change Clock Select display to the following:

ENABLE A = EXT (__ • __ • AR↑) + (__ + __ + AS↓)

Press [CLOCK SELECT], [▽ SET] four times, [▷] twice, [Hx1 0 G], [▷] three times, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Press [TIMING].

When AR↑ + AS↓ is used, the Timing display should look like Figure 10-51.

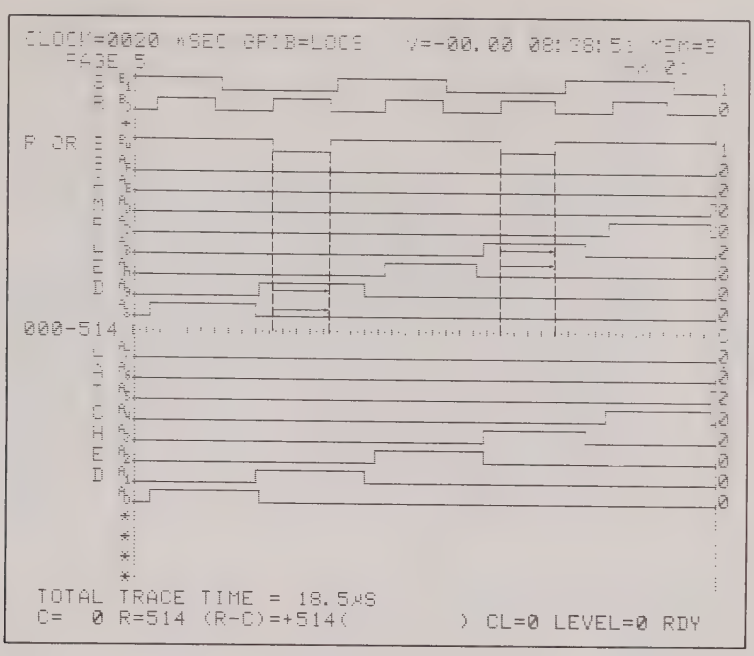


Figure 10-48. Enable = AR↓ + AJ↑.

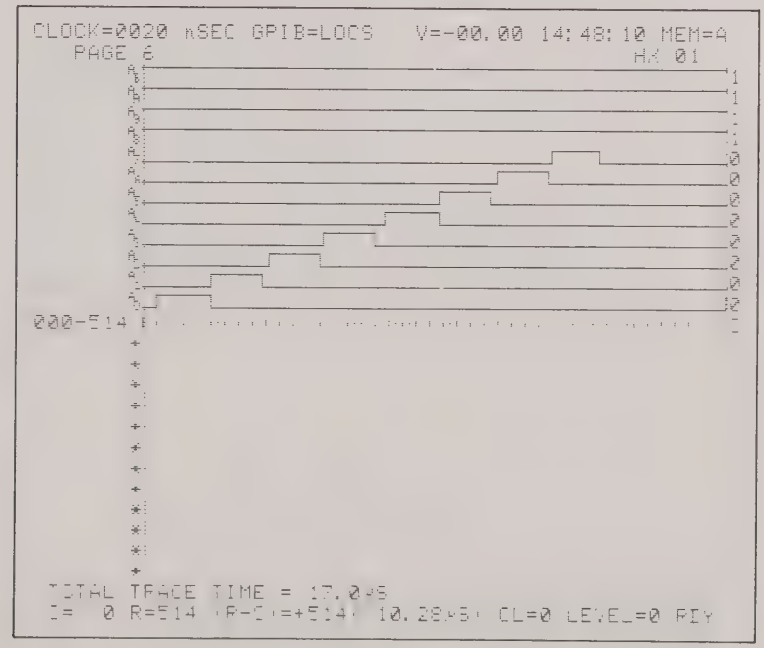


Figure 10-49. Recording for Enable = AR↓ + AS↑.

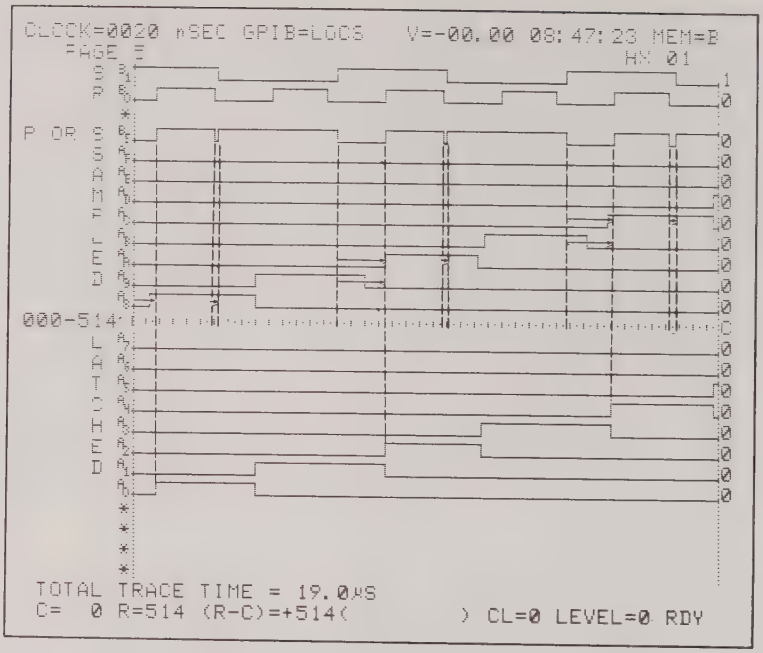


Figure 10-50. Enable = AR↑ + AS↓.

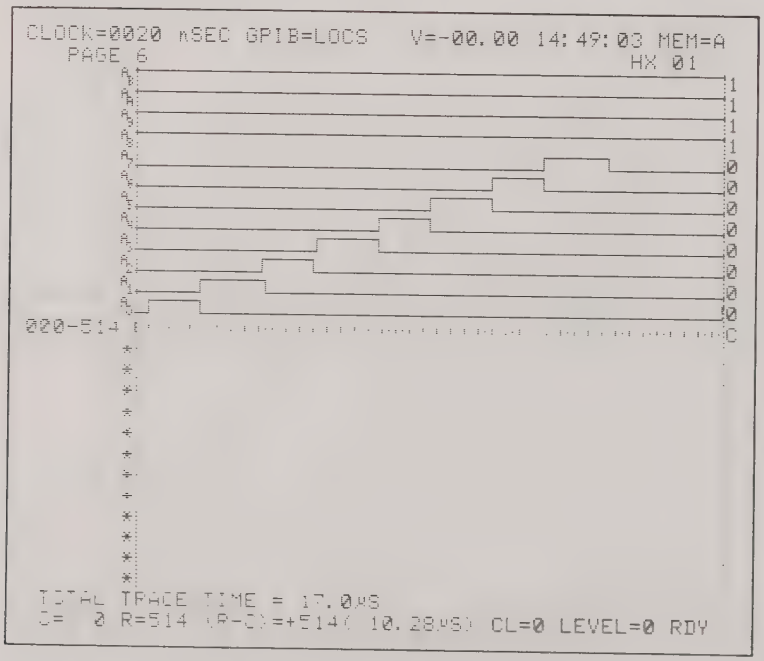


Figure 10-51. Recording for Enable = AR↑ + AS↓.

SET UP: When AR↓ + AS↓ is used the latch enable signal is created by combining AR↓ and AS↓ into a logical OR expression. The inputs are latched while the resultant signal is false and released while it is true. Since the latching occurs totally within every other pulse, the latch signal has no affect on the inputs (see Figure 10-52). Note that no input transitions occur during a latched period; therefore, latch enable has no affect on the inputs.

Change Clock Select display to the following:

ENABLE A = EXT (__·__· AR↓) + (__+__+ AS↓)

Press [CLOCK SELECT] , [▽ SET] four times, [▷] five times, [Hx3 1 H] .

RECORD: Press [ARM] .

REVIEW: Press [TIMING] .

When AR↓ + AS↓ is used, the Timing display should look like Figure 10-53.

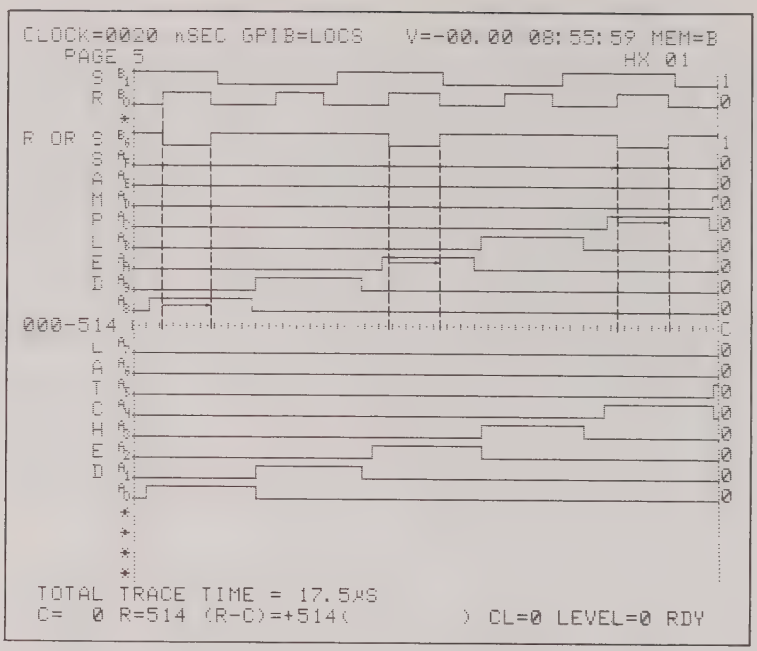


Figure 10-52. Enable = AR↓ + AS↓.

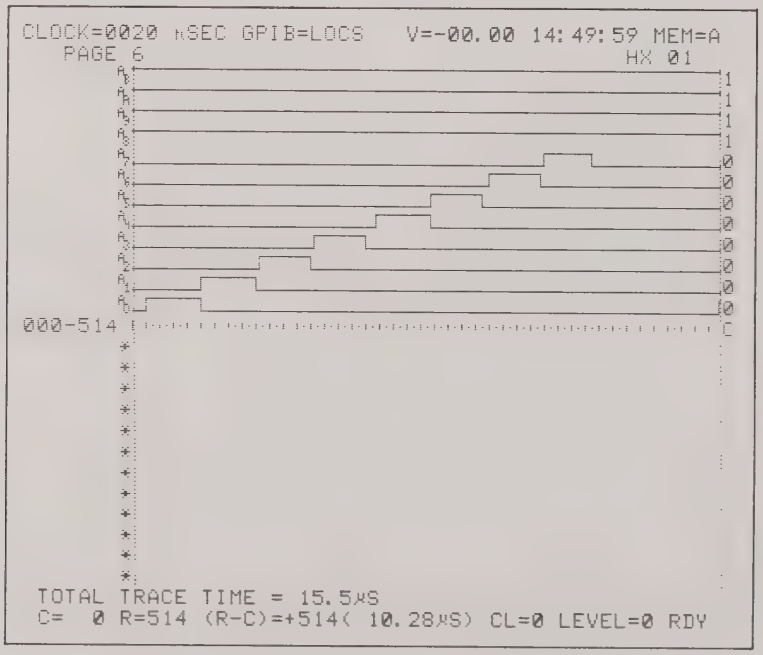


Figure 10-53. Recording for Enable = AR↓ + AS↓.

10.2.4.6 **Demultiplex on a Single Enable Input (AR↑, AR↓, AS↑, AS↓)**

SET UP: The inputs on A7 through A0 are put in the Sample input mode. The inputs on A7 to A0 are also sent to AF through A8 and latched there by the enable signal AR↑.

Change Clock Select display to the following:

ENABLE A = EXT (__·__· AR↑) + (__+__+__)

Change Input mode for inputs AF through A8 and A7 through A0 to display DEMUX.

Display Clock Select screen. Press [CLOCK SELECT], [▽ SET] four times, [▷] twice, [Hx1 0 G], [▷] three times, [Hx6 2 I].

Display Input Mode screen. Press [INPUT MODE], [△] three times, [DEMUX F HEX V].

RECORD: Press [ARM].

REVIEW: Display Timing screen. Press [TIMING].

The display should look like Figure 10-54. The same information is sampled on inputs A7 through A0 and latched before sampling on AF through A8.

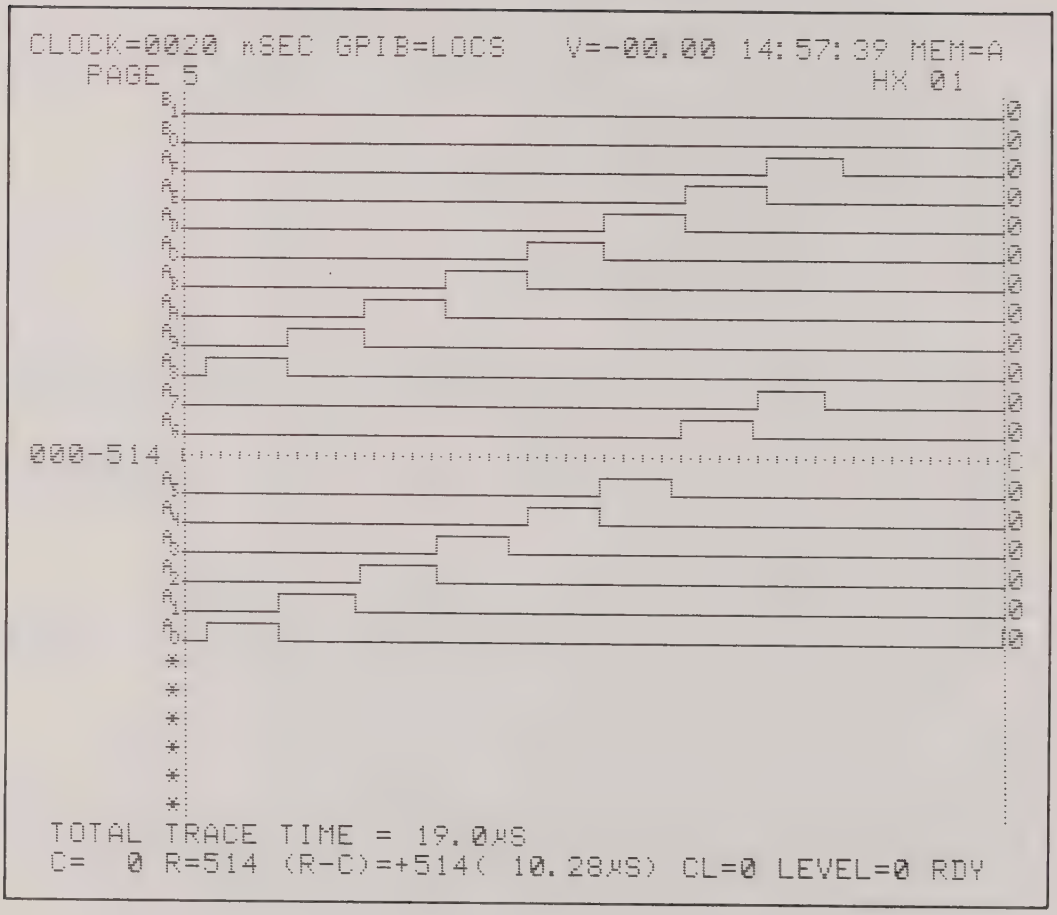


Figure 10-54. AF Through A8 Latched by AR↑.

SET UP: When AR↓ is used the A7 through A0 inputs also sent to AF through A8 are latched there by the enable signal AR↓.

Change Clock Select display to the following:

ENABLE A = EXT (__•__• AR↓) + (__+__+__)

Press [CLOCK SELECT] , [▽ SET] four times, [▷] twice, [Hx3 1 H] .

RECORD: Press [ARM] .

REVIEW: Press [TIMING] .

When AR↓ is used, the Timing display should look like Figure 10-55. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↓.

SET UP: When AS↑ is used, the A7 through A0 inputs also sent to AF through A8 are latched there by the enable signal AS↑.

When AS↑ is used, the Timing display should look like Figure 10-56. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AS↑.

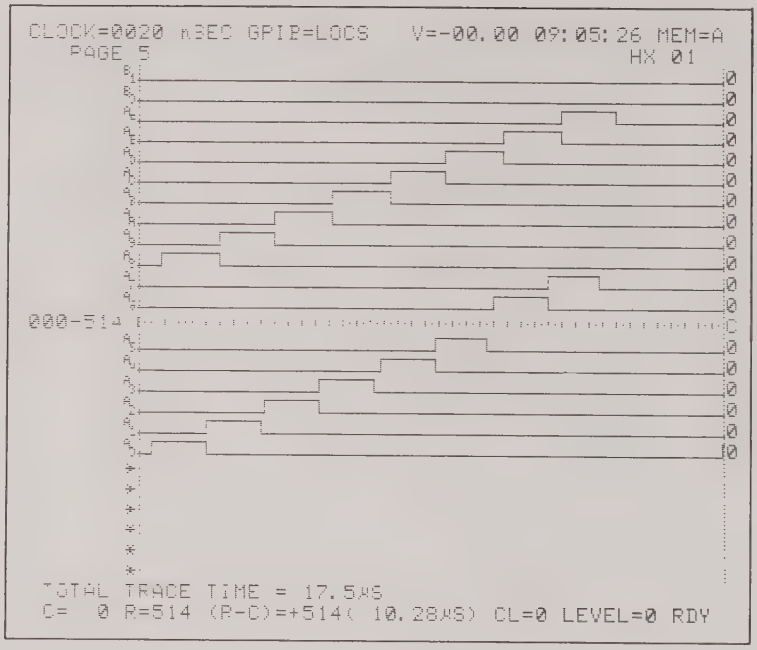


Figure 10-55. AF Through AS Latched by AR↓.

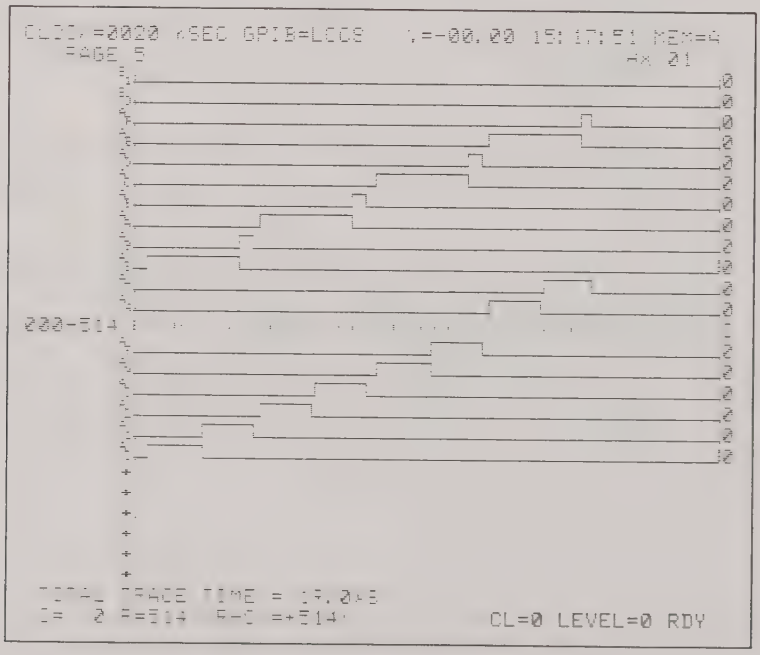


Figure 10-56. AF Through A8 Latched by AS↑.

SET UP: When AS↓ is used, the A7 through A0 inputs also sent to AF through A8, are latched there by the enable signal AS↓.

Change Clock Select display to the following:

ENABLE A = EXT (__•__•__) + (__+__+ AS↓)

Press CLOCK SELECT, ▽ SET four times, ▷ five times, Hx3 1 H.

RECORD: Press ARM.

REVIEW: Press TIMING.

When AS↓ is used, the Timing display should look like Figure 10-57. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AS↓.

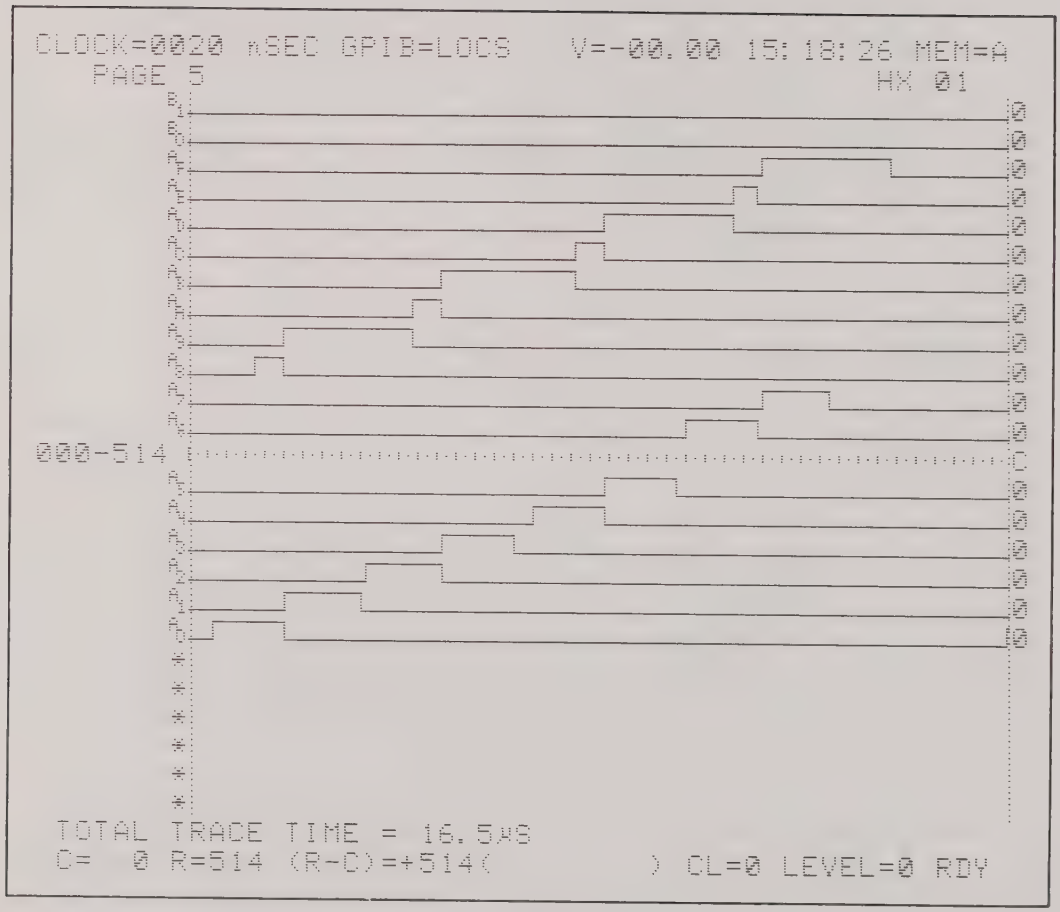


Figure 10-57. AF Through AS Latched by AS↓.

10.2.4.7 **Demultiplex on a Combination of Enable Signals (AR↑ + AS↑, AR↓ + AS↑, AR↑ + AS↓, AR↓ + AS↓)**

SET UP: The A7 through A0 inputs, also sent to AF through A8, are latched there by the enable signal AR↑, AS↑. Change Clock Select display to the following:

ENABLE A = EXT (__ • __ • AR↑) + (__ + __ + AS↑)

Press [CLOCK SELECT], [▽ SET] four times, [▷] twice, [Hx1 0 G], [▷] three times, [Hx1 0 G].

RECORD: Press [ARM].

REVIEW: Display the Timing screen. Press [TIMING].

The display should look like Figure 10-58. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↑ + AS↑.

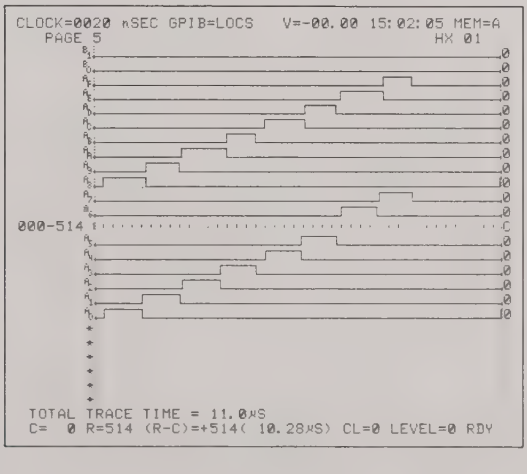


Figure 10-58. AF Through A8 Latched by AR↑ + AS↑.

SET UP: When AR↓ + AS↑ is used, the A7 through A0 inputs, also sent to AF through A8, are latched there by the enable signal AR↓ + AS↑.

Change Clock Select display to the following:

ENABLE A = EXT (__ • __ • AR↓) + (__ + __ + AS↑)

Press [CLOCK SELECT], [▽ SET] four times, [▷] twice, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Press [TIMING].

When AR↓ + AS↑ is used, the display should look like Figure 10-59. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↓ + AS↑.

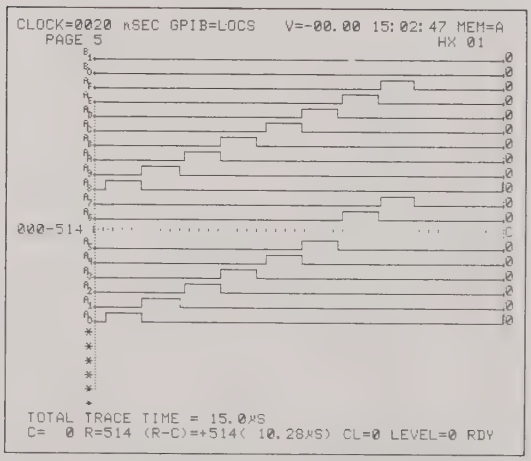


Figure 10-59. AF Through A8 Latched by AR↓ + AS↑.

SET UP: When AR↑ + AS↓ is used, the A7 through A0 inputs also sent to AF through A8, are latched there by the enable signal AR↑ + AS↓.

When AR↑ + AS↓ is used, the Timing display should look like Figure 10-60. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↑ + AS↓.

SET UP: When AR↓ + AS↓is used, the A7 through A0 inputs also sent to AF through A8, are latched there by the enable signal AR↓ + AS↓.

When AR↓ + AS↓ is used, the Timing display should look like Figure 10-61. Demultiplexing the information on inputs A7 through A0 also sends the same information to AF through A8, where it is latched by enable = AR↓ + AS↓.

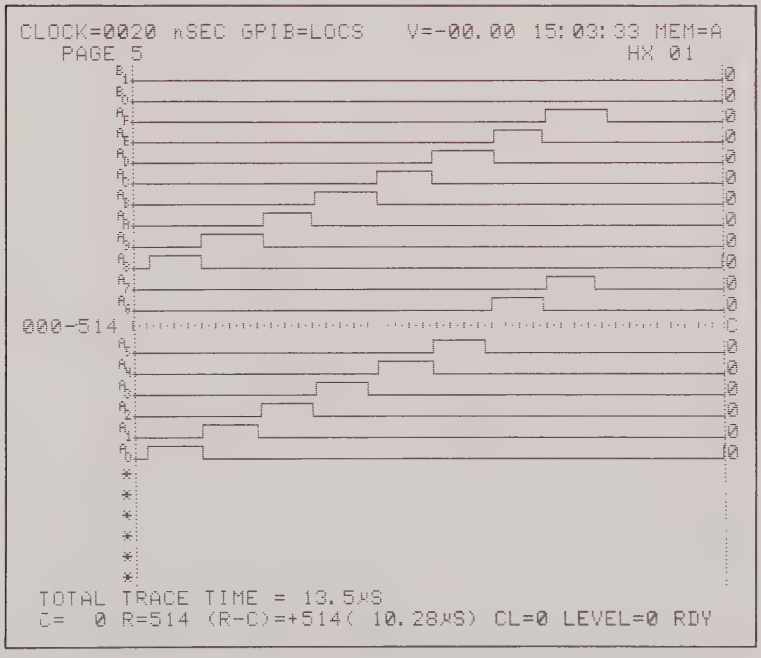


Figure 10-60. AF Through AS Latched by AR↑ + AS↓.

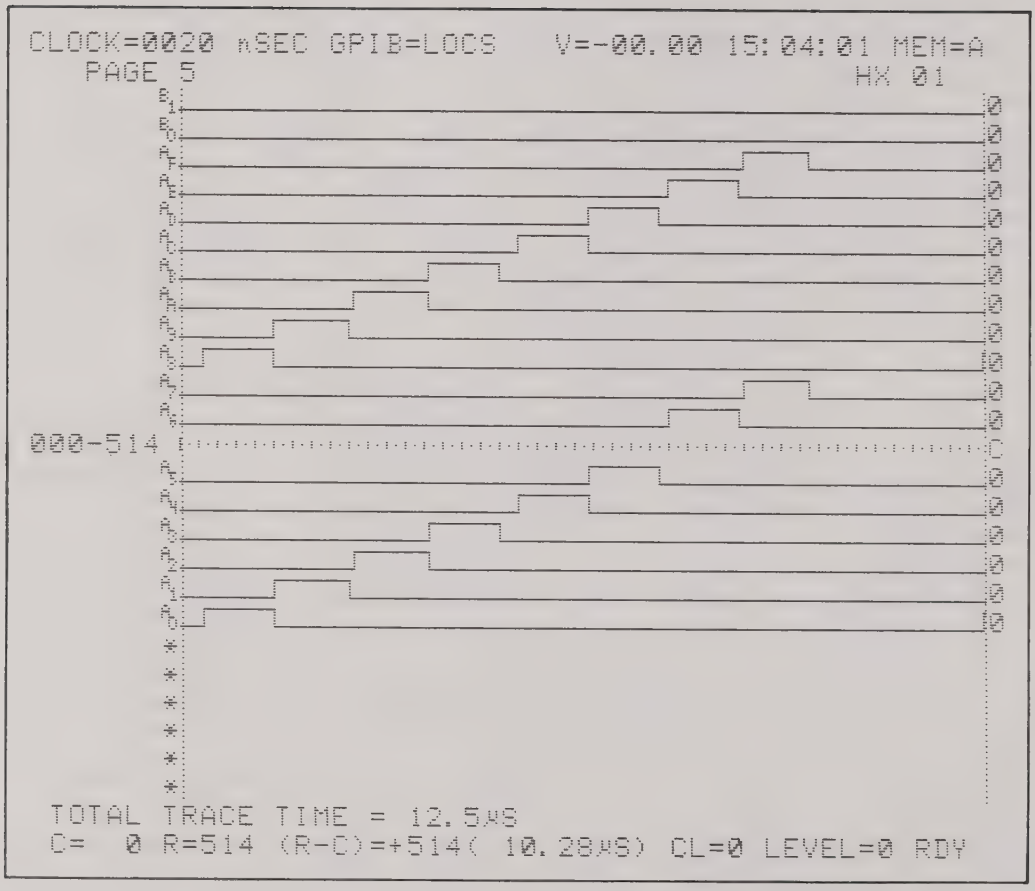


Figure 10-61. AF Through A8 Latched by AR↓ + AS↓.

10.2.5 TRACE CONTROL

The following are specific examples of the basic building blocks of trace control. There are some minor variations in some of the commands. (For example, TRACE IF DATA = T is often substituted for TRACE NEVER to better illustrate the recording process.) You may also notice some difference between a figure and what is displayed on your screen. This is due to remaining values from previous trace control routines. Specifically, if a command is NEVER or ALWAYS, then the value of its associated word recognizer is ignored, as if it were "don't care." Similarly, if DELAY is not used in any of a level's commands, then the specified delay value is ignored, as if it were "zero."

10.2.5.1 **Fill Memory with Samples from Anywhere in Data Stream**

SET UP: Unplug the A7 through A0 probe and connect the AF through A8 probe to PROBE TEST. See setup guide in Figure 10-62.

Display Clock Select screen.

Press [CLOCK SELECT] , [Hx3 1 H] , [▽ SET] twice, [▷] five times, [Hx6 2 '] .

Display Input Mode screen.

Press [INPUT MODE] , [△] , [Hx3 1 H] , [△] twice, [SAMPLE C S] .

Display Data Format screen.

Press [DATA FORMAT] , [Hx12 3 J] , [▽ SET] twice, [ASCII A Q] , [DEMUX F V HEX] ,

[ASCII A Q A] , [LATCH E U OCTAL] , [ASCII A Q A] , [GLITCH D T DECIMAL] , [ASCII A Q A] , [SAMPLE C S] ,

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #51.1 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
D 6	
A 5	
T 4	
A 3	AcAb
2	AcAa
S 1	AbA9
LSB	AcAa

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each over -
TRACE is independent of the other commands
STOP has priority over JUMP.
JUMP has priority over ADVANCE
All four major commands in each leve can come true on any of nine conditions

Quick Key	Command, Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count > Delay
4	If DATA ≠ D and Sample Count < De ay
5	If DATA = D and Sample Count = Delay
6	If DATA ≠ D and Sample Count ≠ Delay
7	If DATA = D and Sample Count < = Delay
8	If DATA = D and Sample Count < Delay

(D - S J A or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = DEC (DEC/HEX) 515 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = X X

(2) JUMP TO 0 (O F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

515 SEQUENTIAL SAMPLES WILL BE RECORDED BEGINNING AT A RANDOM LOCATION.

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

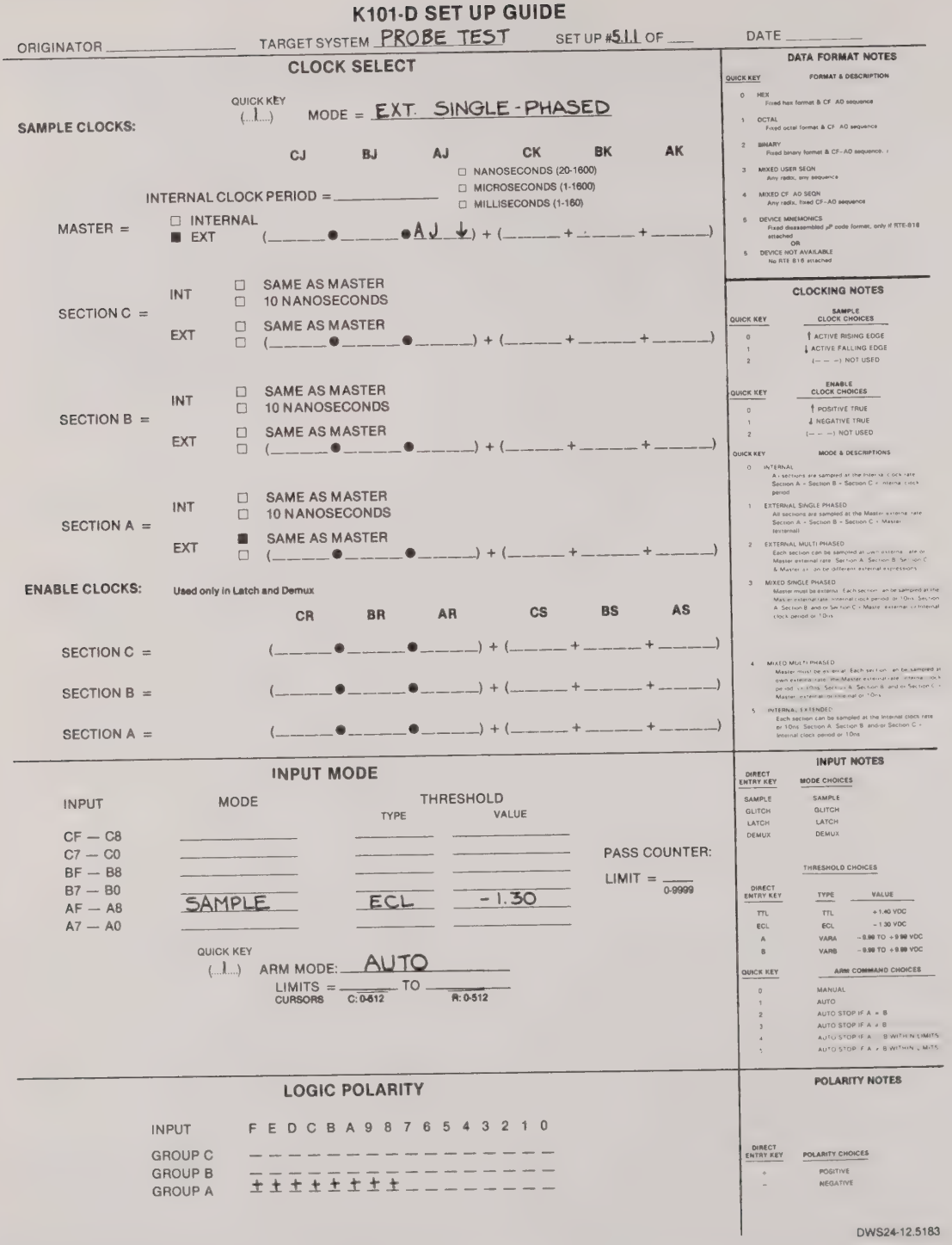
(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

Figure 10-62. Setup Guide: Fill Memory with Samples from Anywhere in Data Stream (Sheet 1 of 2).



K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #5.1.1 OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXT. SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX — Fixed hex format & CF AO sequence
1	OCTAL — Fixed octal format & CF AO sequence
2	BINARY — Fixed binary format & CF-AO sequence, r
3	MIXED USER SEQN — Any radix, any sequence
4	MIXED CF AO SEQN — Any radix, fixed CF-AO sequence
5	DEVICE MNEMONICS — Fixed disassembled μP code format, only if RTE-816 attached OR DEVICE NOT AVAILABLE — No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL — All sections are sampled at the internal clock rate. Section A = Section B = Section C = internal clock period
1	EXTERNAL SINGLE PHASED — All sections are sampled at the Master external rate. Section A = Section B = Section C = Master (external)
2	EXTERNAL MULTI PHASED — Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master can be different external expressions
3	MIXED SINGLE PHASED — Master must be external. Each section can be sampled at the Master external rate, internal clock period or 10ns. Section A, Section B and/or Section C = Master external or internal clock period or 10ns
4	MIXED MULTI PHASED — Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period or 10ns. Section A, Section B, and/or Section C = Master external or internal or 10ns
5	INTERNAL EXTENDED — Each section can be sampled at the internal clock rate or 10ns. Section A, Section B, and/or Section C = internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (1) ARM MODE: AUTO

LIMITS = CURSORS _____ (C: 0-512) TO _____ (R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A > B WITHIN LIMITS
5	AUTO STOP IF A < B WITHIN LIMITS

LOGIC POLARITY

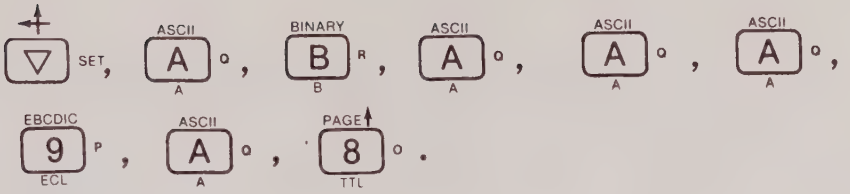
INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

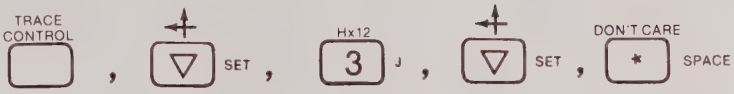
DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

DWS24-12.5183

Figure 10-62. Setup Guide: Fill Memory with Samples from Anywhere in Data Stream (Sheet 2 of 2).



Display Trace Control screen.

Press 

twice.

The Trace Control screen should look like Figure 10-63.

RECORD: Press

.

REVIEW: Display Timing screen.

Press

. You should be on page 4.

Observe how the pattern starts in a different location for every recording. This is because no unique starting or stopping location is specified for capturing the information; it happens randomly.

Stop.

Press

.

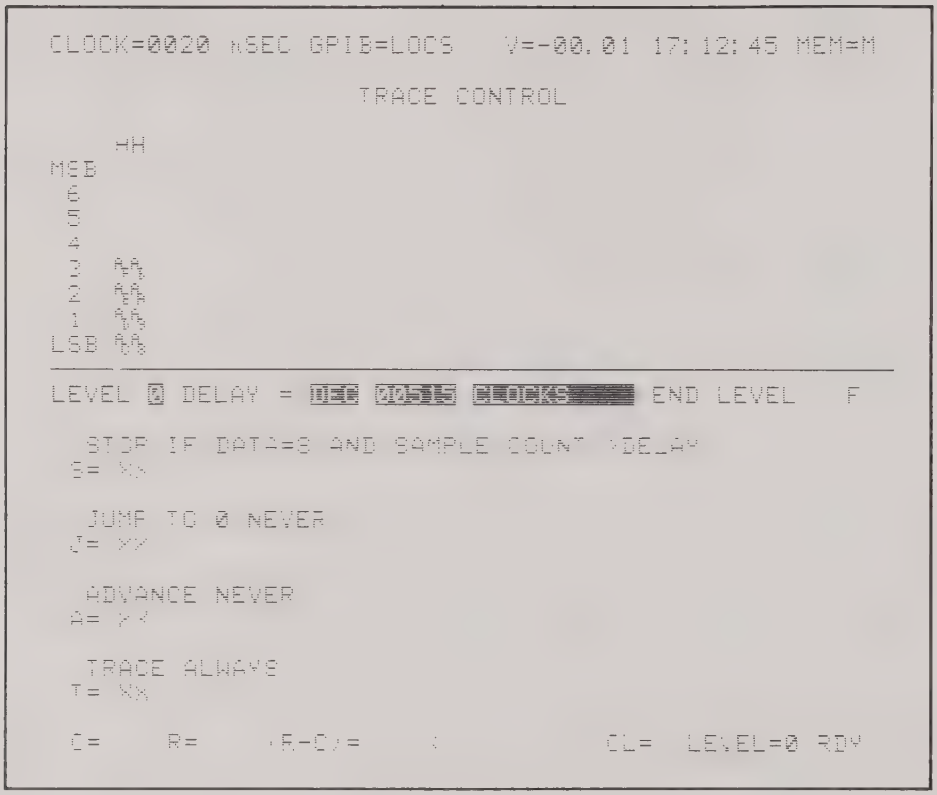


Figure 10-63. Fill Memory From Anywhere in the Data Stream.

10.2.5.2 **Record What Happens Immediately After an Event**

SET UP: Change the trace control program to be as in Figures 10-64 and 10-65.

Press [TRACE CONTROL], [▽ SET], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx3 1 H], [▽ SET], [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx3 1 H], [▽ SET], [Hx3 1 H], [▷] twice, [V24 5 L], [Hx3 1 H], [Hx3 1 H], [▽ SET], [V24 5 L].

RECORD: Press [ARM].

REVIEW: Display Timing screen. Press [TIMING].

Notice that the pattern consistently starts in the same location.

Press [DATA] to see the same thing in the Data Domain display. Stop. Press [STOP].

This display should look like Figure 10-66. Note that the event of interest is the word 01 at location 000; it was captured by the trace control conditions on level 0, as indicated by CL = 0.

Press [▷] (see Figure 10-67).

Note that this and all subsequent words in memory were captured by trace control level 1.

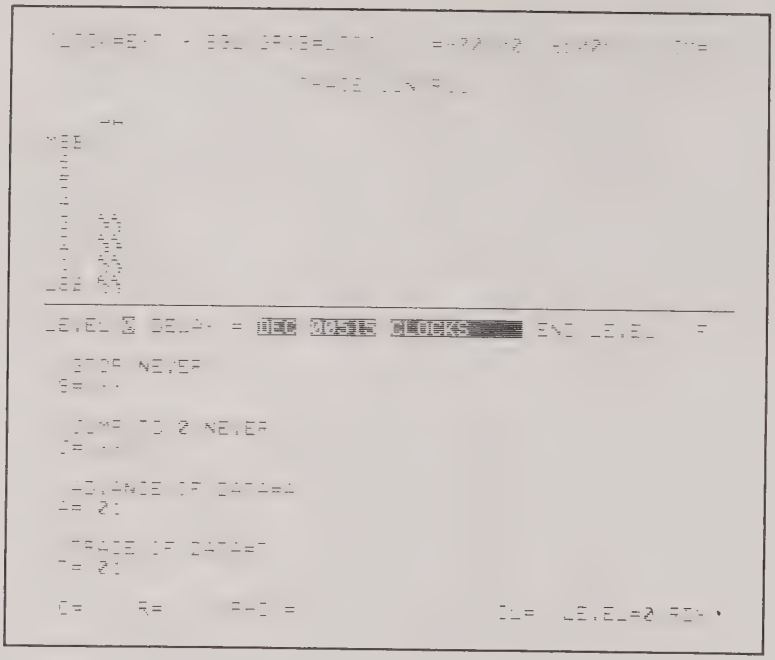


Figure 10-64. First Level, Record Immediately After Event 01.

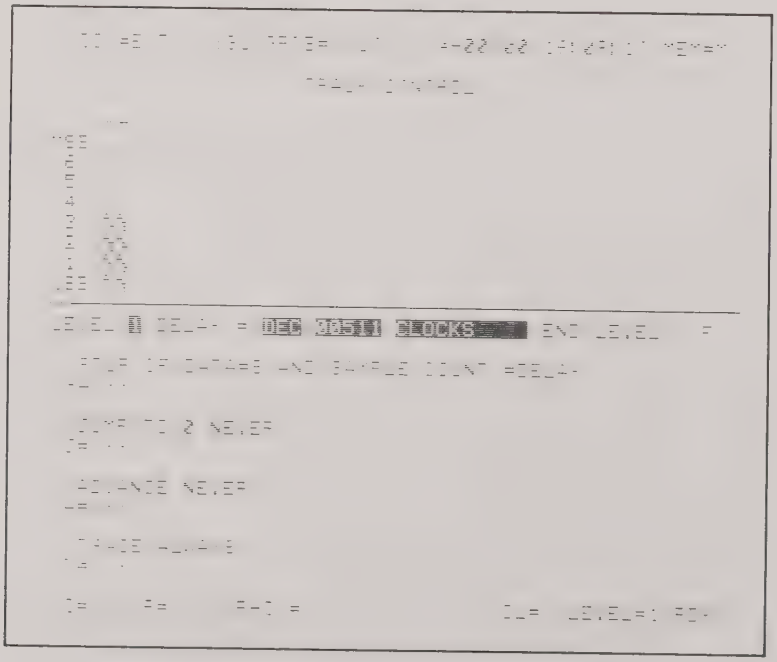


Figure 10-65. Second Level, Record Immediately After Event 01.

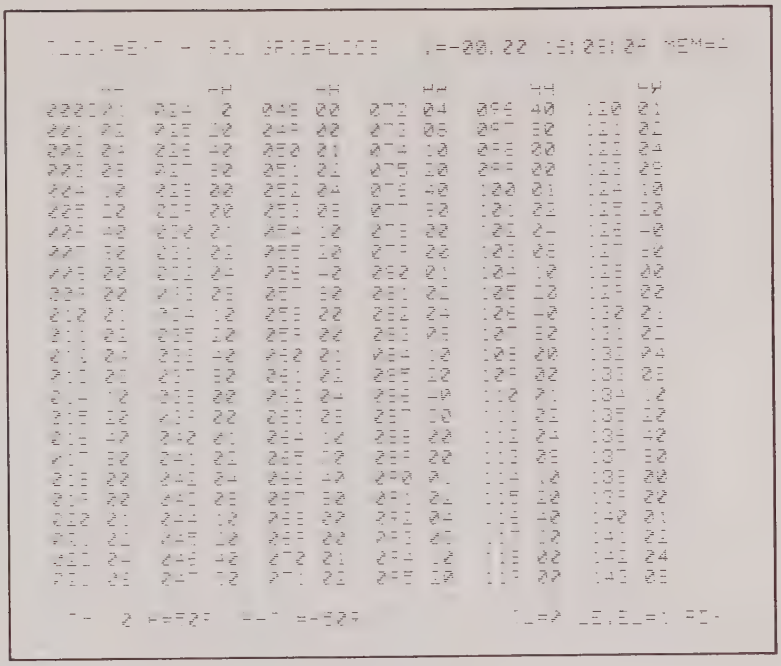


Figure 10-66. Event 01 Recorded by Trace Level 0.

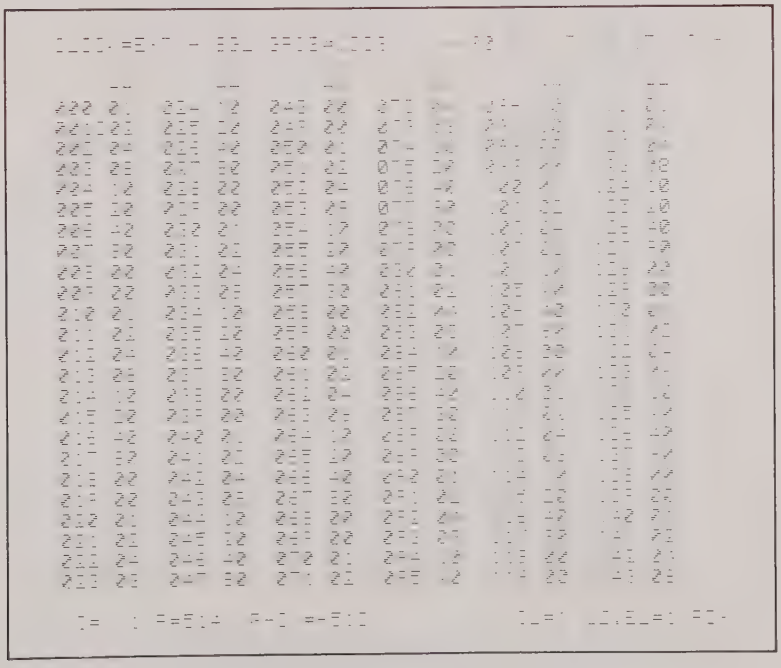


Figure 10-67. Words Recorded by Trace Level 1.

10.2.5.3 **Record What Happens Immediately Before an Event**

SET UP: Change the arm mode to manual.

Press [INPUT MODE] , [△] , [Hx1 0 G] .

Change trace control.

Press [TRACE CONTROL] , [▽ SET] , [Hx1 0 G] , [▽ SET] , [Hx1 0 G] ,
[Hx3 1 H] , [▽ SET] twice, [Hx6 2 I] , [▽ SET] twice, [Hx3 1 H] .

RECORD: Press [ARM] .

REVIEW: Show the Data display. Press [DATA] .

Note that CL = F and that the data are all zeros.

Press [SHIFT] , [◁ SET] , [V24 5 L] , [Hx1 0 G] , [Hx1 0 G] ,
[DATA] .

Press [▷] until CL = 0 (see Figure 10-68).

This is the first traced sample. Tracing continued until 01 occurred and then stopped. Since the Probe Test pattern generator output is continuous and your press of [ARM] is asynchronous with it, tracing can start at any point in the cycle. However, since the pattern repeats every ten sample clocks, a maximum of nine words can occur before the S = 01 condition is met. To see how the first word sampled can vary, press [ARM] again and then [◁ SET], or [▷] .

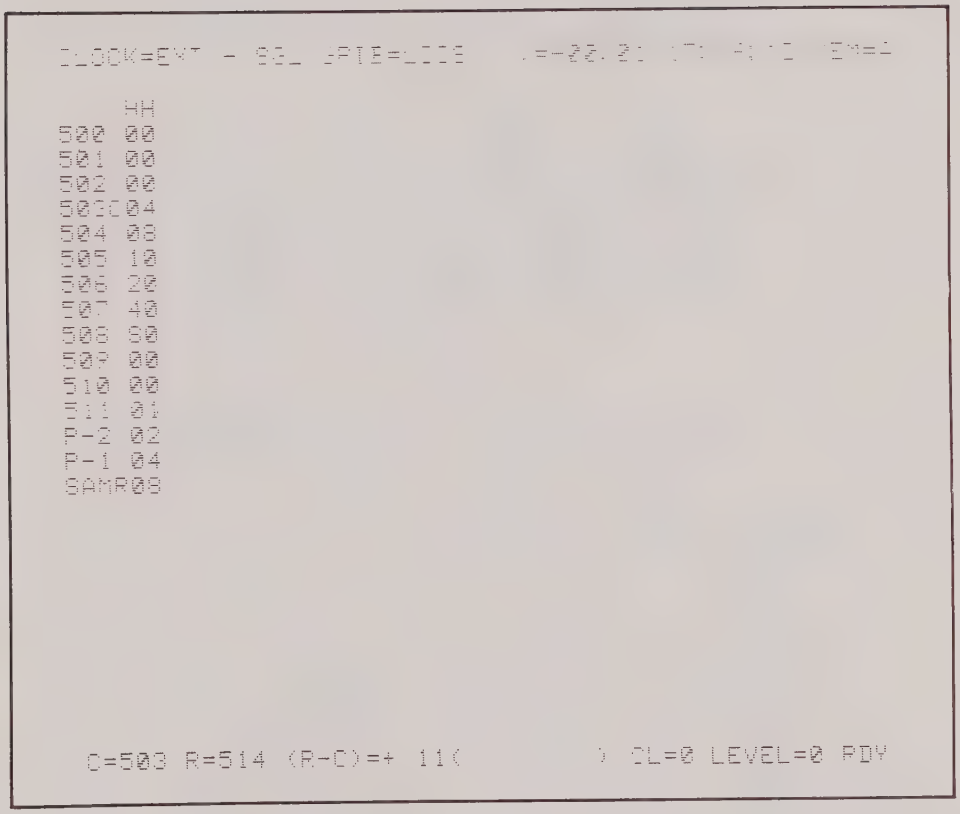


Figure 10-68. First Traced Sample.

This finds the first word captured on level 0 (indicated by CL = 0). Note that location 511 always holds the word 01. Repeat this process several times.

Press until C is at location P-2 (see Figure 10-69).

Note that CL = ?. These last three locations (also referred to as 512, 513, and 514) are the pipeline and sample register contents -- words not yet evaluated by the trace control circuitry.

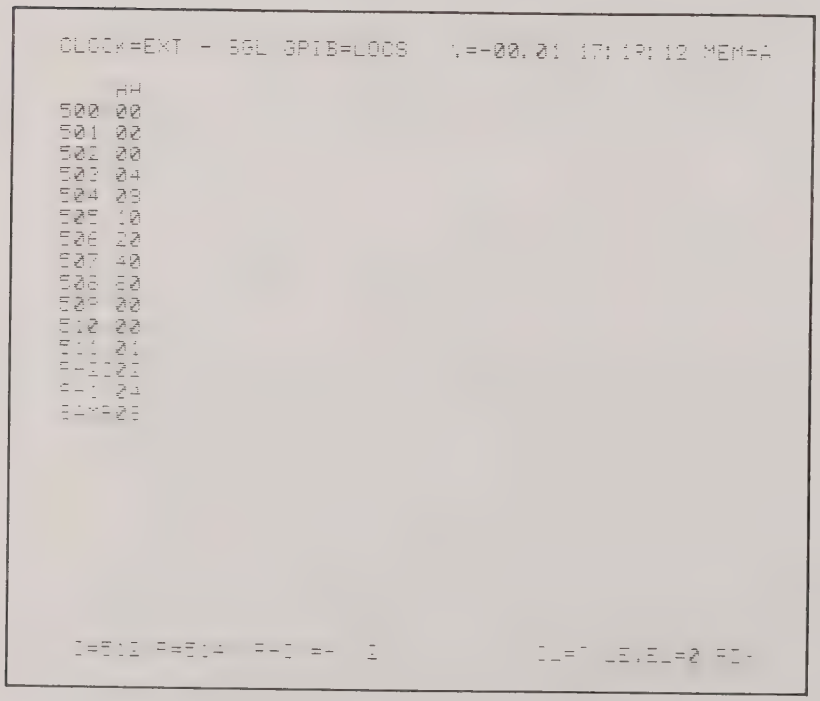


Figure 10-69. Last Three Displayed Words Sampled.

10.2.5.4 **Record What Happens Around an Event**

SET UP: The following will put an event of interest in the middle of memory. Specifically, to put word 01 in sample location 246, the stop of tracing must be delayed by 265(511 - 246) sample clocks. Change the trace control program.

Press [TRACE CONTROL], [▽ SET], [▽ SET] twice, [Hx1 0 G], [▽ SET] three times, [Hx3 1 H], [▷] twice, [Hx6 2 I], [V12 6 M], [V24 5 L].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [Hx6 2 I], [Hx12 3 J], [V12 6 M], [DATA].

Press [▷] until C is at location 246.

The display will look similar to Figure 10-70. The event of interest, 01, has been placed at the specified mid-memory location 246. Note that 01 was recorded there by trace level 0. The following 265 words were recorded by trace level 1. (Again, because of Probe Test's repetitive pattern, only up to nine words could have been recorded on level 0 before 01 occurred.)

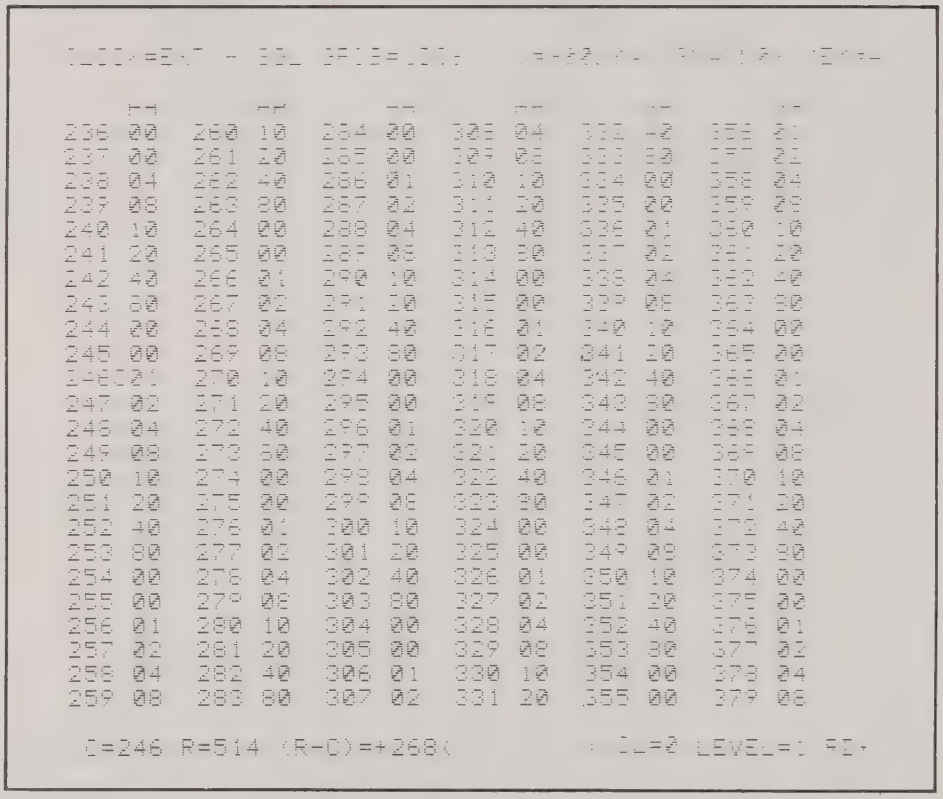


Figure 10-70. Event Placed at Location 246.

10.2.5.5 **Record What Happens Long After an Event**

SET UP: Use the setup guide of Figure 10-71. This will capture a memory full of information long after an event, as well as the event itself, yet without the intervening information.

Press [TRACE CONTROL], [▽ SET] five times, [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx3 1 H], [▽ SET], [Hx3 1 H], [▷] twice, [V24 5 L], [Hx3 1 H], [V24 5 L], [▽ SET], [▽ SET] twice, [V24 5 L], [▽ SET] twice [Hx6 2 I], [▽ SET], [Hx6 2 I], [▷] twice, [V24 5 L], [Hx3 1 H], [Hx1 0 G], [▽ SET], [V24 5 L].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [Hx1 0 G], [DATA].

The display should look like Figure 10-72. Recording the words in locations 002 to 511 was delayed from recording the word at location 001 by 515 sample clocks. The intervening words were not recorded.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5120 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AFAB
A T 2	AEAA
S 1	ADA9
LSB	ACA8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has prior ty over JUMP.
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA 0
1	Always
2	Never
3	If DATA = D and Sample Count = De ay
4	If DATA - D and Sample Count = Delay
5	If DATA D and Sample Count = De ay
6	If DATA - D and Samp e Count = - Delay
7	If DATA = D and Sample Count = Delay
8	If DATA D and Sample Count = Delay

(D = S, A or T which are assigned by command type.)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = _____ (DEC/HEX 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(0) TRACE IF DATA = A
T = 0 1

COMMENTS
ONLY 01 IS TRACED INTO MEMORY. AT ITS OCCURANCE, TRACE CONTROL ADVANCES TO LEVEL 1.

LEVEL 1 (O-F) DELAY = DEC 515 (DEC/HEX 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = X X

(2) TRACE NEVER
T = X X

COMMENTS
NOTHING IS TRACED IN THIS LEVEL IT MERELY WAITS FOR 515 CLOCKS TO OCCUR BEFORE ADVANCING.

LEVEL 2 (O-F) DELAY = DEC 510 (DEC/HEX 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(5) STOP IF DATA = S AND SAMPLE COUNT = DELAY
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS
THE REST OF MEMORY IS FILLED WITH THE NEXT 510 SEQUENTIAL SAMPLES.

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX 0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(____) STOP
S = _____

(____) JUMP TO ___ (O F)
J = _____

(____) ADVANCE
A = _____

(____) TRACE
T = _____

COMMENTS

Figure 10-71. Setup Guide: Record What Happens Around an Event (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.2 D

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____
☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____ + _____ + _____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____ + _____ + _____)
SECTION B = (_____●_____●_____) + (_____ + _____ + _____)
SECTION A = (_____●_____●_____) + (_____ + _____ + _____)

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL
LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
GROUP B	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
GROUP A	↕	↕	↕	↕	↕	↕	↕	↕	_	_	_	_	_	_	_	_

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX — Fixed hex format & CF-A0 sequence
1	OCTAL — Fixed octal format & CF-A0 sequence
2	BINARY — Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN — Any radix any sequence
4	MIXED CF A0 SEQN — Any radix fixed CF-A0 sequence
5	DEVICE MNEMONICS — Fixed disassembled µP code format, only if RTE 818 attached OR
6	DEVICE NOT AVAILABLE — No RTE 818 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL — All sections are sampled at the Internal clock rate. Section A = Section B = Section C = Internal clock period
1	EXTERNAL SINGLE PHASED — All sections are sampled at the Master external rate. Section A = Section B = Section C = Master external
2	EXTERNAL MULTI PHASED — Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED — Master must be external. Each section can be sampled at the Master external rate, Internal clock period or 10ns. Section A, Section B and or Section C = Master external or Internal clock period or 10ns
4	MIXED MULTI PHASED — Master must be external. Each section can be sampled at own external rate, the Master external rate, Internal clock period or 10ns. Section A, Section B and or Section C = Master external or Internal or 10ns
5	INTERNAL EXTENDED — Each section can be sampled at the Internal clock rate or 10ns. Section A, Section B and or Section C = Internal clock period or 10ns

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	−1.30 VDC
A	VARA	−9.99 TO +9.99 VDC
B	VARB	−9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
.	POSITIVE
	NEGATIVE

DWS24-12.5183

Figure 10-71. Setup Guide: Record What Happens Around an Event (Sheet 2 of 2).

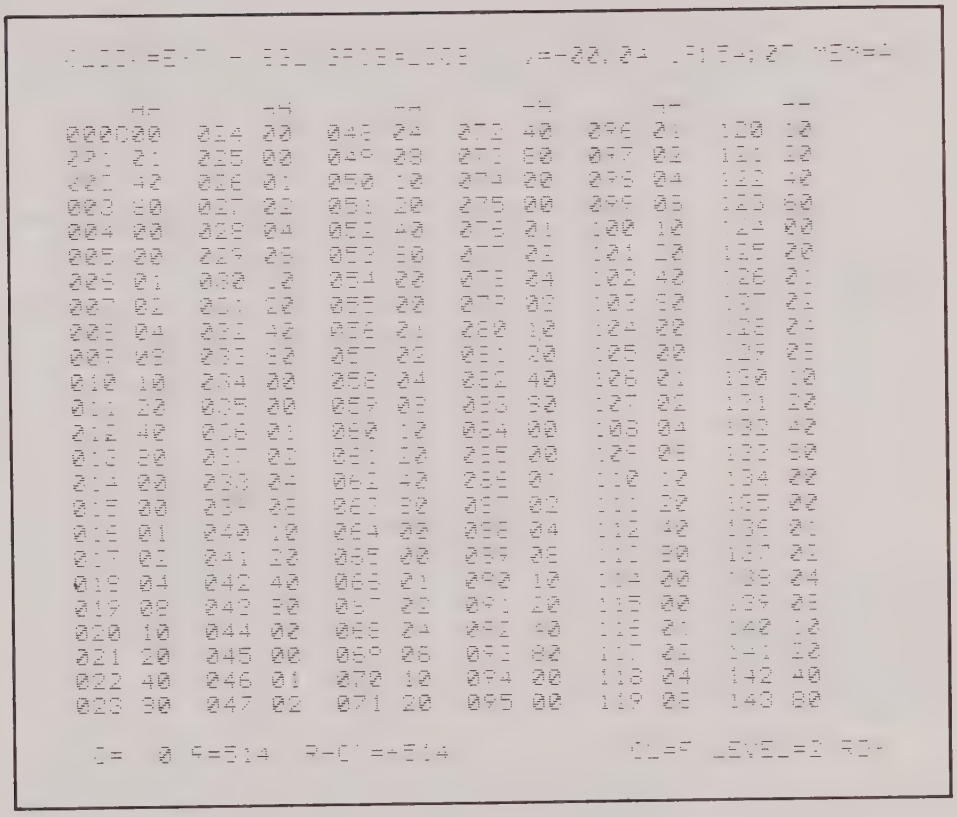


Figure 10-72. Recording of Selected Words.

Press [▷] . Note that CL = F changes to CL = 0; 01 was recorded by trace level 0. Press [▷] again.

Note that CL = 2; the next recorded sample was traced by level 2. Nothing was recorded during level 1. Although 515 samples (1 memoryful) flowed through the analyzer between trace control levels 0 and 2, none of them were stored in memory.

10.2.5.6 **Capture a Segment of Samples: Record from Here to There**

SET UP: Only a part of one cycle of the Probe Test pattern (the word sequence 01, 02, 04, 08, 10, 20, 40, 80) will be captured. See setup guide in Figure 10-73. Change the trace control program.

Press [TRACE CONTROL] , [▽ SET] four times, [Hx1 0 G] , [Hx3 1 H] , [▽ SET] twice, [Hx1 0 G] , [Hx3 1 H] , [▽ SET], [Hx3 1 H] , [▽ SET] three times, [Hx1 0 G] , [▽ SET], [PAGE 8 O TTL], [Hx1 0 G], [▽ SET], [Hx3 1 H] , [▽ SET], [Hx6 2 '] , [▽ SET] , [Hx3 1 H] , [▽ SET] four times, [Hx6 2 '] .

RECORD: Press [ARM] .

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.3 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H_H

MSB	
6	
DATA 5	
PAT 4	
TURN 3	AF AB
AT 2	AE AA
S 1	AD A9
LSB	AC A8

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
A TRUE major command in each level can come true on any of nine conditions:

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA ≠ D and Sample Count = Delay
5	If DATA < D and Sample Count = Delay
6	If DATA > D and Sample Count = Delay
7	If DATA = D and Sample Count ≠ Delay
8	If DATA ≠ D and Sample Count ≠ Delay

(D = S, A, or T, which are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = _____ (DEC/HEX) _____ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 0 1
(0) TRACE IF DATA = T
T = 0 1

COMMENTS

TRACE CONTROL WAITS FOR 01 TO OCCUR, THEN TRACES IT AND ADVANCES.

LEVEL 1 (O-F) DELAY = _____ (DEC/HEX) _____ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 8 0
(1) TRACE ALWAYS
T = X X

COMMENTS

EVERYTHING IS TRACED UP UNTIL 80 OCCURS, THEN TRACE CONTROL ADVANCES.

LEVEL 2 (O-F) DELAY = _____ (DEC/HEX) _____ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(1) STOP ALWAYS
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(2) ADVANCE NEVER
A = X X
(2) TRACE NEVER
T = X X

COMMENTS

NO MORE SAMPLES ARE TRACED AND THE RECORDING PROCESS STOPS, SINCE THE DESIRED SEGMENT HAS BEEN RECORDED.

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) _____ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(___) STOP
S = _____
(___) JUMP TO ___ (O-F)
J = _____
(___) ADVANCE
A = _____
(___) TRACE
T = _____

COMMENTS

Figure 10-73. Setup Guide: Capture a Segment of Samples: Record from Here to There (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.3

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

INTERNAL CLOCK PERIOD = _____

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)
SECTION B = (_____●_____●_____) + (_____+_____+_____)
SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF AO sequence
1	OCTAL Fixed octal format & CF-AO sequence
2	BINARY Fixed binary format & CF-AO sequence
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF-AO SEQN Any radix, fixed CF-AO sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format only if RTE 816 attached OR
5	DEVICE NOT AVAILABLE No RTE 815 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the Internal clock rate Section A - Section B - Section C - Internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A - Section B - Section C - Master (external)
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, Internal clock period, or 10ns. Section A, Section B, and/or Section C - Master (external) or Internal clock period or 10ns
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, Internal clock period, or 10ns. Section A, Section B, and/or Section C - Master (external) or Internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the Internal clock rate or 10ns. Section A, Section B, and or Section C - Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8	_____	_____	_____
C7 — C0	_____	_____	_____
BF — B8	_____	_____	_____
B7 — B0	_____	_____	_____
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	↕	↕	↕	↕	↕	↕	↕	↕	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 10-73. Setup Guide: Capture a Segment of Samples: Record from Here to There (Sheet 2 of 2).

REVIEW: Press SHIFT , ◁ SET , 5 L , 0 G , 3 J , DATA , ▷ .

The display should look like Figure 10-74. The first word of the pattern segment was captured by level 0 and the following nine by level 1.

Press ▷ to location 511 (see Figure 10-75).

The segment was captured on levels 0 and 1; recording stopped on level 2 (as indicated by LEVEL = 2 RDY).

Press TIMING and move the Control Cursor ◁ SET to verify that only one pattern was recorded.

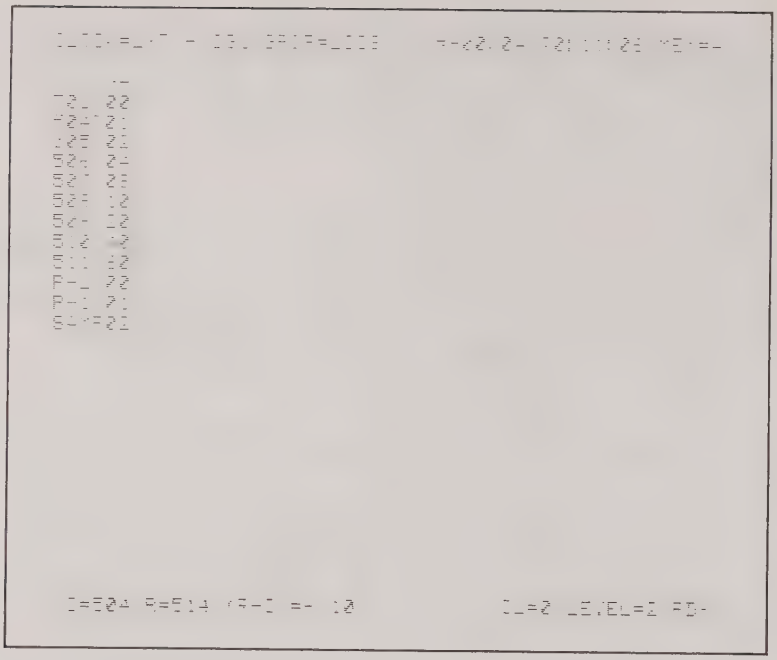


Figure 10-74. First Word (01) Recorded by Level 0.

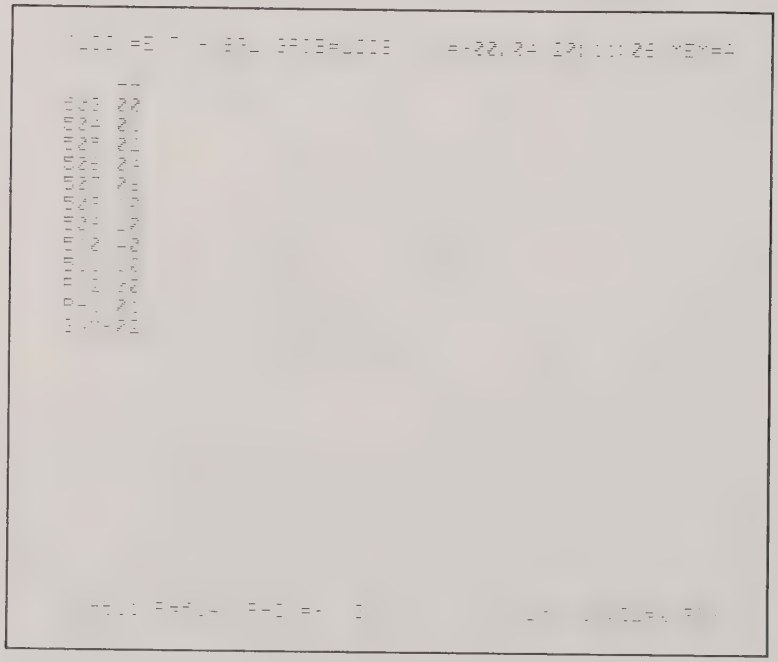


Figure 10-75. Words of Segment Recorded by Level 1.

10.2.5.7 Exclude Recording a Segment of Samples: Don't Record from Here to There

SET UP: To exclude capturing all the words between the first (01) and last (80) words of one cycle of the pattern, see setup guide in Figure 10-76.

Press [TRACE CONTROL] , [▽ SET] five times, [Hx3 1 H] , [▽ SET], [Hx3 1 H] , [▽ SET] five times, [Hx1 0 G] , [▽ SET], [PAGE 8 O TTL], [Hx1 0 G] , [▽ SET], [Hx6 2 I] , [▷] twice, [V24 5 L] , [Hx1 0 G] , [Hx1 0 G] , [▽ SET], [Hx12 3 J] , [▽ SET] five times, [Hx3 1 H] .

RECORD: Press [ARM] .

REVIEW: Press [SHIFT] , [◁ SET] , [Hx1 0 G] , [TIMING] .

This display should look like Figure 10-77. The six pulses between the first and last pulse of the pattern were not recorded in memory, although they were sampled into the analyzer. Notice the six missing pulses in the first cycle. They correspond to the excluded data words 02, 04, 08, 10, 20, and 40. Move the Control Cursor to verify the trace level on which each word was recorded.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.4 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
D N 6	
A P 5	
T U 4	
A T 3	AF AB
S 2	AE AA
1	AD A9
LSB	AC A8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(1) TRACE ALWAYS
T = X X

COMMENTS

EVERYTHING IS TRACED UNTIL 01 OCCURS WHEN TRACE CONTROL THEN ADVANCES

LEVEL 1 (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 8 0

(0) TRACE IF DATA = T
T = 8 0

COMMENTS

THIS LEVEL WAITS FOR 80 TO OCCUR, TRACING NOTHING UNTIL IT DOES AND THEN ADVANCING.

LEVEL 2 (O-F) DELAY = DEC (DEC/HEX) 500 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

FULL TRACING OF ALL SAMPLES RESUMES FOR 500 MORE CLOCKS.

LEVEL ___ (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(. .) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

Figure 10-76. Setup Guide: Exclude Recording a Segment of Samples: Don't Record from Here to There (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.4

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

	CJ	BJ	AJ	CK	BK	AK
INTERNAL CLOCK PERIOD = _____				☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)		
MASTER = ☐ INTERNAL ■ EXT			(_____●_____●AJ ↓) + (_____+_____+_____)			
SECTION C = INT			☐ SAME AS MASTER ☐ 10 NANOSECONDS			
EXT			☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)			
SECTION B = INT			☐ SAME AS MASTER ☐ 10 NANOSECONDS			
EXT			☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)			
SECTION A = INT			☐ SAME AS MASTER ☐ 10 NANOSECONDS			
EXT			■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)			

ENABLE CLOCKS: Used only in Latch and Demux

	CR	BR	AR	CS	BS	AS
SECTION C =	(_____●_____●_____) + (_____+_____+_____)					
SECTION B =	(_____●_____●_____) + (_____+_____+_____)					
SECTION A =	(_____●_____●_____) + (_____+_____+_____)					

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence.
1	OCTAL Fixed octal format & CF-A0 sequence
2	BINARY Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF A0 SEQN Any radix, fixed CF-A0 sequence.
5	DEVICE MNEMONICS Fixed disassembled μP code format, only if RTE-816 attached OR
5	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the Internal clock rate Section A = Section B = Section C = Internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A = Section B = Section C = Master (external)
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, Internal clock period or 10ns. Section A, Section B and/or Section C = Master (external) or Internal clock period or 10ns
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, Internal clock period or 10ns. Section A, Section B and/or Section C = Master (external) or Internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the Internal clock rate or 10ns. Section A, Section B and or Section C = Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8	_____	_____	_____
C7 — C0	_____	_____	_____
BF — B8	_____	_____	_____
B7 — B0	_____	_____	_____
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ (CURSORS C: 0-512, R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	↕	↕	↕	↕	↕	↕	↕	↕	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

DWS24-12.5183

Figure 10-76. Setup Guide: Exclude Recording a Segment of Samples: Don't Record from Here to There (Sheet 2 of 2).

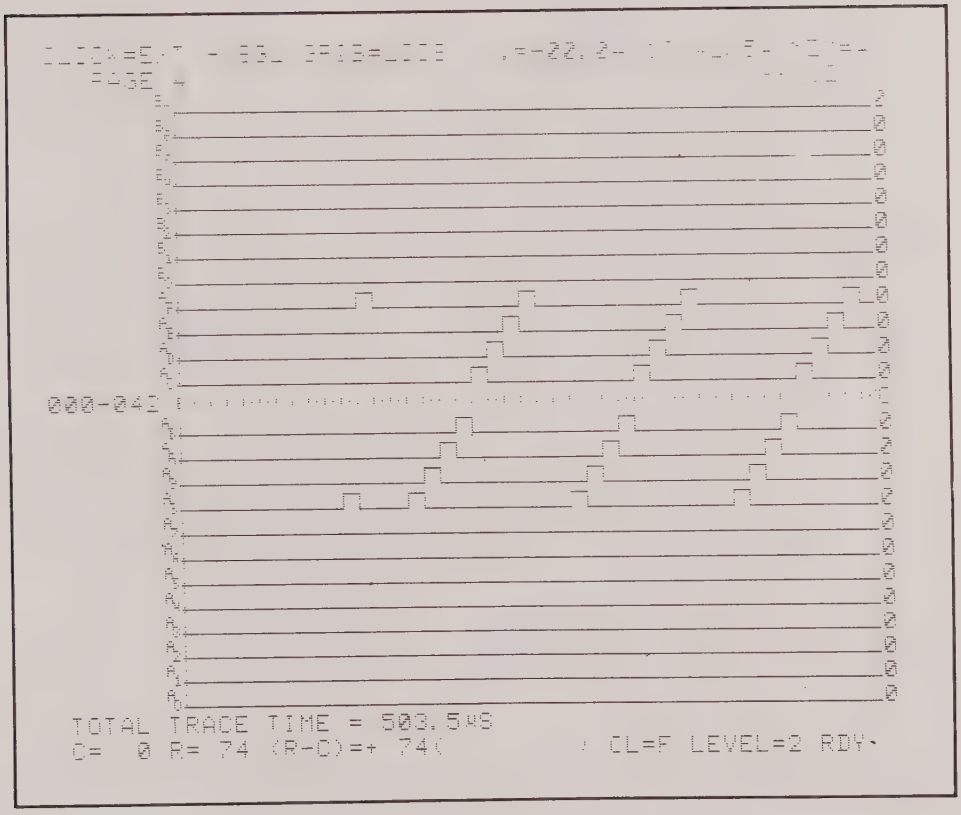


Figure 10-77. Six Pulses Sampled and Not Recorded.

10.2.5.8 Selectively Record Only One Kind of Sample for a Certain Number of Times

SET UP: To record only one memoryful of the word 01, change trace control.

Press [TRACE CONTROL], [▷], three times, [Hx3 1 H], [▽ SET], [V24 5 L], [▽ SET] three times, [Hx6 2 I], [▽ SET] twice, [Hx1 0 G].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [Hx12 3 J], [V12 6 M], [DATA].

The display should look like Figure 10-78. Only 01s were recorded. P-2, P-1, and SAM show some of the other sampled words that flowed through the analyzer but did not meet the trace control TRACE conditions.

10.2.5.8 Follow a Path, Then Record

SET UP: Fill memory only after confirming that four words of the pattern occur in their proper sequence: 02, 08, 20, then 80. See setup guide in Figure 10-79.

Press [TRACE CONTROL], [▽ SET], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [Hx6 2 I], [▽ SET], [Hx3 1 H], [▽ SET] four times, [Hx1 0 G], [PAGE 8 O TTL], [▽ SET] twice, [Hx1 0 G], [PAGE 8 O TTL],

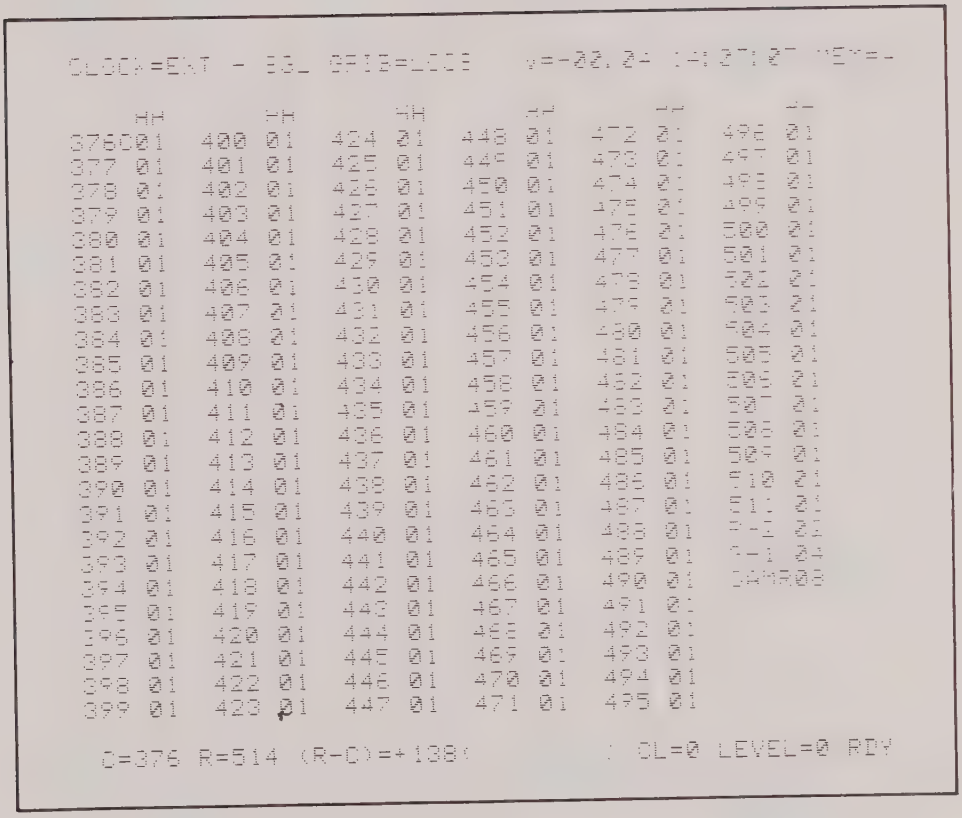


Figure 10-78. Word 01 Selected to be Recorded.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.6 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AEAB
A T 2	AEAA
S 1	ADA1
LSB	ACAB

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands on each level can come true on any of nine conditions.

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count - Delay
4	If DATA ≠ D and Sample Count - Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count - = Delay
7	If DATA = D and Sample Count - = Delay
8	If DATA = D and Sample Count - - Delay

(D = S, J, A, or T, which are assigned by command type.)

TRACE CONTROL

LEVEL (QUICK KEY) 0 (0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (0-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 0 2
(0) TRACE IF DATA = T
T = 0 2

COMMENTS: WAIT FOR 02, TRACE IT AND ADVANCE.

LEVEL (QUICK KEY) 1 (0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (0-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 0 8
(0) TRACE IF DATA = T
T = 0 8

COMMENTS: WAIT FOR 08, TRACE IT AND ADVANCE.

LEVEL (QUICK KEY) 2 (0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (0-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 2 0
(0) TRACE IF DATA = T
T = 2 0

COMMENTS: WAIT FOR 20, TRACE IT AND ADVANCE.

LEVEL (QUICK KEY) 3 (0-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (0-F)

(2) STOP NEVER
S = X X
(2) JUMP TO 0 (0-F) NEVER
J = X X
(0) ADVANCE IF DATA = A
A = 8 0
(0) TRACE IF DATA = T
T = 8 0

COMMENTS: WAIT FOR 80, TRACE IT AND ADVANCE.

Figure 10-79. Setup Guide: Follow a Path, Then Record (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.6 (cont.) ___ OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3
A T 2
S 1
LSB

AEAB
AEAA
ADA9
ACA8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
A four major commands (to match each pair of hex
bytes in any Mnemonic or Binary
Quick Key (1 missing combination

0 If DATA = D
1 Always
2 Never
3 If DATA = D and Sample Count = Delay
4 If DATA = D and Sample Count > Delay
5 If DATA = D and Sample Count < Delay
6 If DATA = D and Sample Count > = Delay
7 If DATA = D and Sample Count < = Delay
8 If DATA = D and Sample Count = Delay

(D = S J A or T which are assigned by command type

TRACE CONTROL

QUICK KEY (3) LEVEL 4 (O-F) DELAY = DEC (DEC/HEX) 500 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(3) STOP IF DATA = 5 AND SAMPLE COUNT > DELAY
S = X X

(2) JUMP TO 0 (O F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

TRACE ALL THE FOLLOWING 500 SAMPLES AND STOP.

QUICK KEY (.....) LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

QUICK KEY (.....) LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

QUICK KEY (.....) LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

Figure 10-79. Setup Guide: Follow a Path, Then Record (Sheet 2 of 2).

[▽ SET], [Hx6 2 I], [▽ SET], [Hx6 2 I], [▽ SET] twice,
[Hx1 0 G], [▽ SET], [Hx6 2 I], [Hx1 0 G], [▽ SET], [Hx1 0 G],
[▽ SET], [Hx6 2 I], [Hx1 0 G], [▽ SET], [Hx12 3 J],
[▽ SET], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [▽ SET],
[PAGE↑ 8 O TTL], [Hx1 0 G], [▽ SET], [PAGE↓ 4 K], [▷] twice,
[V24 5 L], [Hx1 0 G], [Hx1 0 G].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [Hx1 0 G], [TIMING].

The display should look like Figure 10-80. The first four pulses had to occur in their proper sequence before the following pulses could be recorded.

Press [DATA], then press [▷] slowly ten times,

noting the cursor level of each word (see Figure 10-81). The words 02, 08, 20, and 80 were traced on levels 0, 1, 2, and 3, respectively, before the following data could be recorded by level 4.

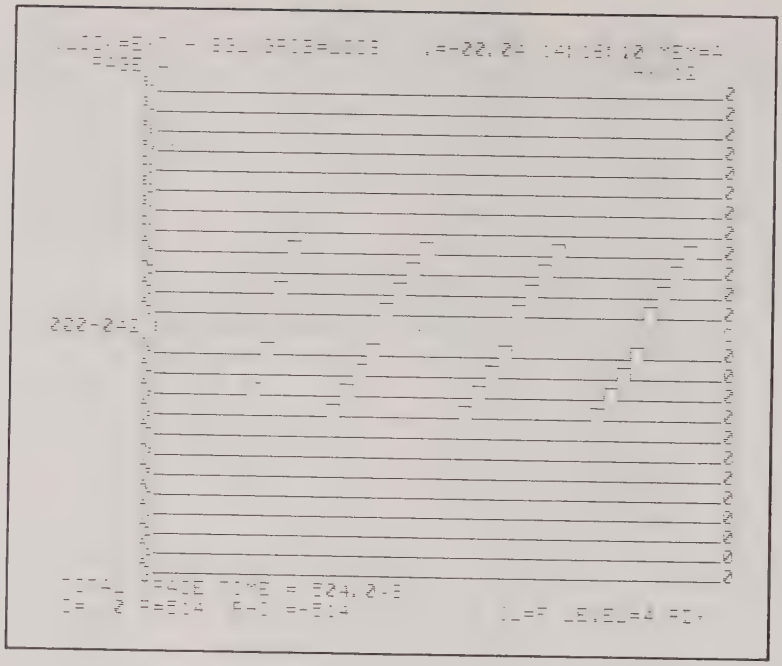


Figure 10-80. Four Pulses Sequence for Recording.

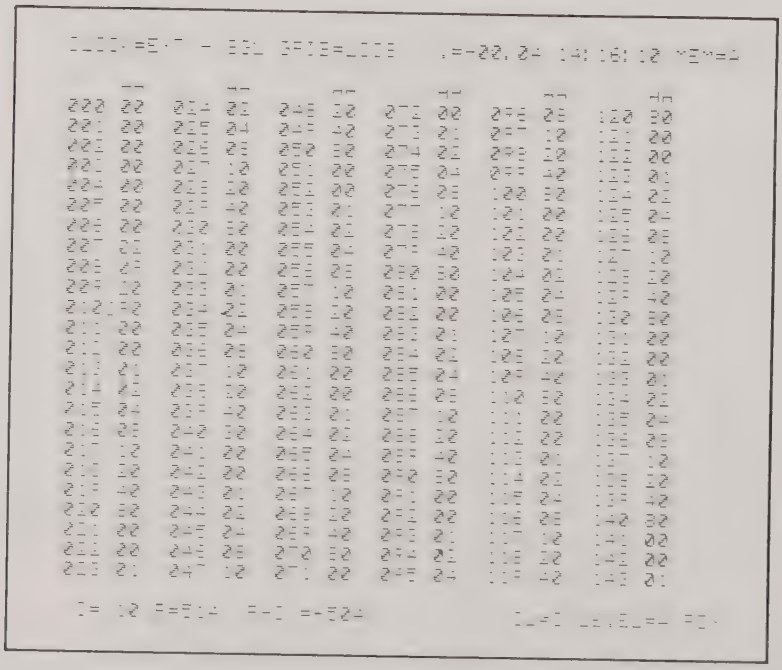


Figure 10-81. Trace on Four Levels Before Recording.

10.2.5.10 **Record, then Follow a Path**

SET UP: After capturing a memoryful of information, confirm that several subsequent words of the pattern occur in their proper sequence, i.e., 08, 20, then 80. See setup guide in Figure 10-82.

Press [TRACE CONTROL], [▷], twice, [V24 5 L], [Hx3 1 H], [V24 5 L], [▷], [Hx1 0 G], [▽ SET] three times, [Hx12 3 J], [▽ SET], [DON'T CARE *] [SPACE] twice, [▽ SET], [Hx3 1 H], [▽ SET], [Hx12 3 J], [▽ SET], [Hx1 0 G], [▽ SET], [PAGE↑ 8 O TTL], [Hx1 0 G], [▽ SET] twice, [Hx6 2 '].

RECORD: Press [ARM].

REVIEW: Press [SHIFT], [◁ SET], [PAGE↓ 4 K], [EBCDIC 9 P ECL], [V12 6 M], [DATA].

Press [▷] slowly.

Note the cursor level at each location; this verifies the sequence of events that occurred after the main information was recorded (see Figure 10-83). After the information was recorded, subsequent words were checked to verify that the expected execution path occurred.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP #5.1.7 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AE AB
A T 2	AE AA
S 1	AD A9
LSB	AC A8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
A trace, jump or commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA = D and Sample Count > Delay
5	If DATA = D and Sample Count < Delay
6	If DATA = D and Sample Count ≥ Delay
7	If DATA ≠ D and Sample Count ≤ Delay
8	If DATA = D and Sample Count ≤ Delay

(D = S, J, A, or T, which are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = DEC 515 (DEC/HEX 0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(3) ADVANCE IF DATA = A AND SAMPLE COUNT > DELAY
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS: TRACE EVERYTHING FOR 515 SAMPLES THEN ADVANCE.

LEVEL 1 (O-F) DELAY = ____ (DEC/HEX) ___ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 8

(0) TRACE IF DATA = T
T = 0 8

COMMENTS: WAIT FOR 08, TRACE IT AND ADVANCE

LEVEL 2 (O-F) DELAY = ____ (DEC/HEX) ___ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 2 0

(0) TRACE IF DATA = T
T = 2 0

COMMENTS: WAIT FOR 20, TRACE IT AND ADVANCE.

LEVEL 3 (O-F) DELAY = ____ (DEC/HEX) ___ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(0) STOP IF DATA = S
S = 8 0

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(0) TRACE IF DATA = T
T = 8 0

COMMENTS: WAIT FOR 80, TRACE IT AND STOP RECORDING

Figure 10-82. Setup Guide: Record, Then Follow a Path (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.7

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____
☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)
SECTION B = (_____●_____●_____) + (_____+_____+_____)
SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX — Fixed hex format & CF-A0 sequence
1	OCTAL — Fixed octal format & CF-A0 sequence
2	BINARY — Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN — Any radix, any sequence
4	MIXED CF-A0 SEQN — Any radix, fixed CF-A0 sequence.
5	DEVICE MNEMONICS — Fixed disassembled µP code format, only if RTE-816 attached OR
6	DEVICE NOT AVAILABLE — No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL — All sections are sampled at the internal clock rate Section A = Section B = Section C = internal clock period
1	EXTERNAL SINGLE PHASED — All sections are sampled at the Master external rate Section A = Section B = Section C = Master external
2	EXTERNAL MULTI PHASED — Each section can be sampled at own external rate or Master external rate Section A, Section B Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED — Master must be external Each section can be sampled at the Master external rate Internal clock period or 10ns Section A Section B and/or Section C = Masterexternal or Internal clock period or 10ns
4	MIXED MULT PHASED — Master must be external Each section can be sampled at own external rate the Master external rate Internal clock period, or 10ns Section A Section B and or Section C = Master external or Internal or 10ns
5	INTERNAL EXTENDED — Each section can be sampled at the Internal clock rate or 10ns Section A Section B and or Section C = Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A > B WITHIN LIMITS
5	AUTO STOP IF A < B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

DWS24-12.5183

Figure 10-82. Setup Guide: Record, Then Follow a Path (Sheet 2 of 2).

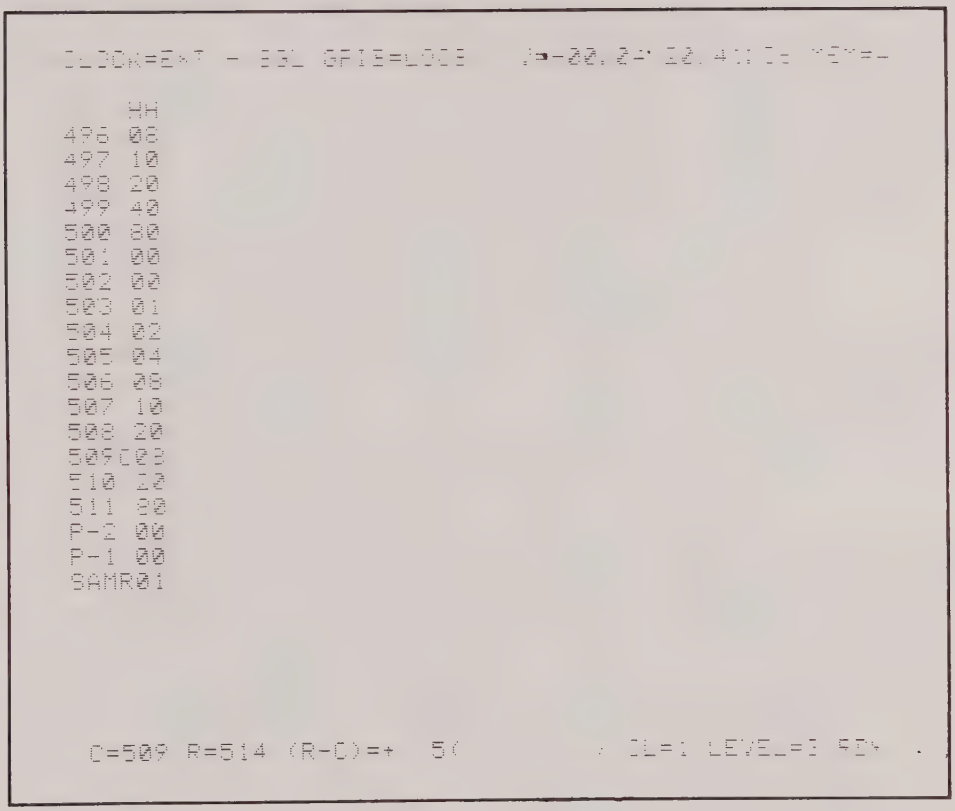


Figure 10-83. Verify Expected Execution Path.

10.2.5.11 **Check for Event 1 or Event 2**

SET UP: The place in the pattern cycle where the analyzer will begin sampling will vary with each recording. For example, if the first word sampled is 01, the next will be 02, the next 04, and so on; if the first word is 10, the next will be 20, the next 40, and so on. Therefore, one cannot predict whether 01 will appear before 10 or vice versa. The trace control program will end on level 1 if 10 occurs first and level 8 if 01 occurs first, thereby indicating exactly which happened when (see setup guide in Figure 10-84).

Press [TRACE CONTROL], [▽ SET] twice, [PAGE 8 TTL], [▷], [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx3 1 H], [▽ SET], [Hx1 0 G], [▽ SET], [Hx3 1 H], [Hx1 0 G], [▽ SET] twice, [Hx3 1 H], [▽ SET], [Hx3 1 H], [▽ SET] twice, [Hx6 2 I], [▽ SET] twice, [Hx3 1 H], [▽ SET], [PAGE 8 TTL], [▽ SET], [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Observe the trace level status field. It indicates which path was taken and therefore, which word occurred first. LEVEL = 1 RDY means 10 happened first. LEVEL = 8 RDY means 01 happened first.

Press [DATA] to verify.

Press [ARM] several times to see the varying end levels.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.8A OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AE AB
A T 2	AE AA
S 1	AD A9
LSB	AC AD

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions.

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA ≠ D and Sample Count = Delay
5	If DATA < D and Sample Count = Delay
6	If DATA > D and Sample Count = Delay
7	If DATA ≥ D and Sample Count = Delay
8	If DATA ≤ D and Sample Count = Delay

(D = S, J, A, or T which are assigned by command type.)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = _____ (DEC/HEX) _____ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(Quick Key 2) STOP NEVER
S = X X

(Quick Key 0) JUMP TO 8 (O-F) IF DATA = J
J = 0 1

(Quick Key 0) ADVANCE IF DATA = A
A = 1 0

(Quick Key 1) TRACE ALWAYS
T = X X

COMMENTS

TRACE EVERYTHING WHILE LOOKING FOR 10 OR 01. IF 01 OCCURS 1st, GO TO LEVEL 8. OTHERWISE GO TO LEVEL 1.

LEVEL 1 (O-F) DELAY = _____ (DEC/HEX) _____ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(Quick Key 1) STOP ALWAYS
S = X X

(Quick Key 2) JUMP TO 0 (O-F) NEVER
J = X X

(Quick Key 2) ADVANCE NEVER
A = X X

(Quick Key 1) TRACE ALWAYS
T = X X

COMMENTS

THIS LEVEL IS ONLY ENTERED IF 10 OCCURED BEFORE 01. IT TRACES ONE SAMPLE AND STOPS.

LEVEL 8 (O-F) DELAY = _____ (DEC/HEX) _____ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(Quick Key 1) STOP ALWAYS
S = X X

(Quick Key 2) JUMP TO 0 (O-F) NEVER
J = X X

(Quick Key 2) ADVANCE NEVER
A = X X

(Quick Key 1) TRACE ALWAYS
T = X X

COMMENTS

THIS LEVEL IS ONLY ENTERED IF 01 OCCURED BEFORE 10. IT TRACES ONE SAMPLE AND STOPS.

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) _____ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(Quick Key ___) STOP
S =

(Quick Key ___) JUMP TO ___ (O-F)
J =

(Quick Key ___) ADVANCE
A =

(Quick Key ___) TRACE
T =

COMMENTS

Figure 10-84. Setup Guide: Check for Event 1 or Event 2 (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.8A

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____
- ☐ NANOSECONDS (20-1600)
- ☐ MICROSECONDS (1-1600)
- ☐ MILLISECONDS (1-160)

MASTER =
- ☐ INTERNAL
- ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A =
- INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
- EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence
1	OCTAL Fixed octal format & CF-A0 sequence
2	BINARY Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE-816 attached OR
6	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— —) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A = Section B = Section C = Internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A = Section B = Section C = Master external
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, internal clock period or 10ns. Section A, Section B and or Section C = Master external or internal clock period or 10ns
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period or 10ns. Section A, Section B and or Section C = Master external or internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns. Section A, Section B and or Section C = internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ (CURSORS C: 0-512, R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A ≠ B
3	AUTO STOP IF A = B
4	AUTO STOP IF A ≠ B WITHIN LIMITS
5	AUTO STOP IF A = B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	↕	↕	↕	↕	↕	↕	↕	↕	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

DWS24-12.5183

Figure 10-84. Setup Guide: Check for Event 1 or Event 2 (Sheet 2 of 2).

10.2.5.12 **Take the Same Path Regardless of Which Event Occurred**

SET UP: As in paragraph 10.2.5.11, either 10 or 01 may be sampled first. Regardless, trace control goes to level 1 and stops. See setup guide in Figure 10-85.

Press TRACE CONTROL , ▽ SET twice, Hx3 1 H .

RECORD: Press ARM .

REVIEW: Press SHIFT , ◁ SET , V24 5 L , Hx1 0 G , Hx12 3 J , DATA , ▷ seven times.

Your display should look like either Figure 10-86 or 10-87.

Press ARM repeatedly and observe the word in location 510. It may be 01 or 10, but tracing always stops at level 1.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.88 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3
A T 2
S 1
LSB

A E A B
A E A A
A D A 9
A C A 8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA = D and Sample Count < Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count > = Delay
7	If DATA = D and Sample Count = Delay
8	If DATA = D and Sample Count = Delay

(D = S, J, A, or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X
(0) JUMP TO 1 (O-F) IF DATA = J
J = 0 1
(0) ADVANCE IF DATA = A
A = 1 0
(1) TRACE ALWAYS
T = X X

COMMENTS

EVERYTHING IS TRACED WHILE LOOKING FOR EVENT 01 OR 10 TO OCCUR. REGARDLESS OF WHICH HAPPENS 1st, GO TO LEVEL 1.

LEVEL 1 (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(1) STOP ALWAYS
S = X X
(2) JUMP TO 0 (O-F) NEVER
J = X X
(2) ADVANCE NEVER
A = X X
(1) TRACE ALWAYS
T = X X

COMMENTS

TRACE ONE SAMPLE AND STOP.

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =
(.....) JUMP TO ___ (O-F)
J =
(.....) ADVANCE
A =
(.....) TRACE
T =

COMMENTS

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =
(.....) JUMP TO ___ (O-F)
J =
(.....) ADVANCE
A =
(.....) TRACE
T =

COMMENTS

Figure 10-85. Setup Guide: Take the Same Path Regardless of Which Event Occurred (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.8B

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

INTERNAL CLOCK PERIOD = _____

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence
1	OCTAL Fixed octal format & CF-A0 sequence
2	BINARY Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence
5	DEVICE MNEMONICS Fixed disassembled μP code format, only if RTE-B18 attached OR
5	DEVICE NOT AVAILABLE No RTE B18 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL
All sections are sampled at the internal clock rate
Section A = Section B = Section C = Internal clock period

1 EXTERNAL SINGLE PHASED
All sections are sampled at the Master external rate
Section A = Section B = Section C = Master external

2 EXTERNAL MULT PHASED
Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section & Master can be different external expressions

3 MIXED SINGLE PHASED
Master must be external. Each section can be sampled at the Master external rate, internal clock period, or 10ns. Section A, Section B and or Section C = Master external or internal clock period or 10ns

4 MIXED MULT PHASED
Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period, or 10ns. Section A, Section B and or Section C = Master external or internal clock period or 10ns

5 INTERNAL EXTENDED
Each section can be sampled at the internal clock rate or 10ns. Section A, Section B and or Section C = internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 10-85. Setup Guide: Take the Same Path Regardless of Which Event Occurred (Sheet 2 of 2).

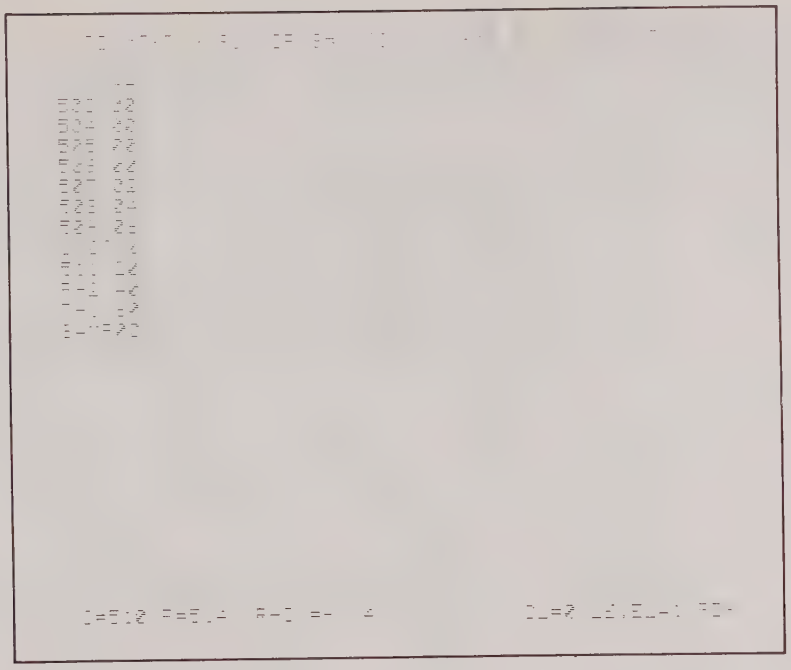


Figure 10-86. Sometimes 10 will occur on level 0.

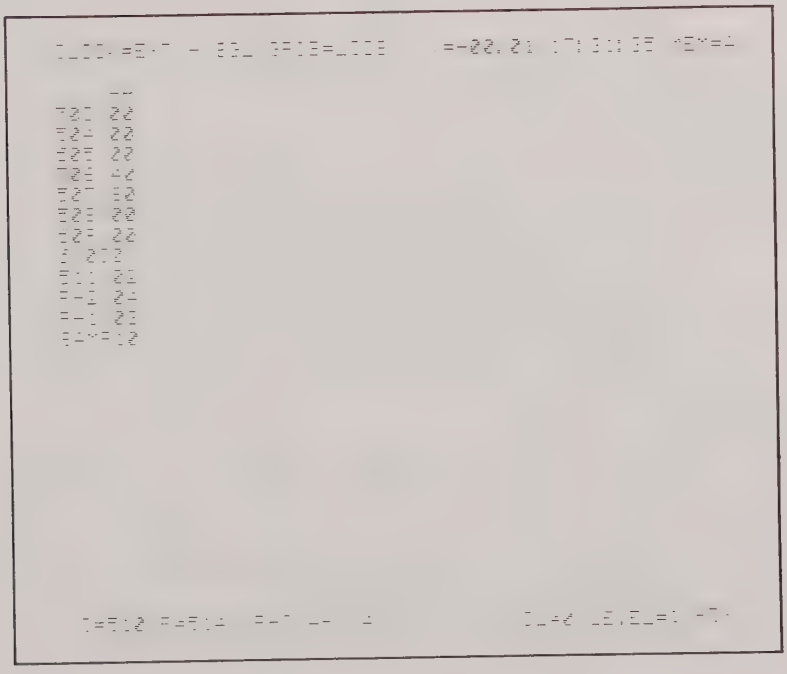


Figure 10-87. Sometimes 01 will occur on level 0.

10.2.5.13 **Check for Correct Timing Between Two Events**

SET UP: According to the Probe Test pattern there should be exactly four samples, or "ticks" of the master sample clock, between words 01 and 10. See setup guide in Figure 10-88 to verify this time interval.

Press [TRACE CONTROL], [▽ SET] twice, [▷], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [Hx3 1 H], [▽ SET] twice, [Hx3 1 H], [▷] twice, [Hx12 3 J], [▽ SET], [Hx6 2 I], [▽ SET], [PAGE 8 O TTL], [▷], [V6 7 N], [▽ SET], [Hx3 1 H], [Hx1 0 G], [▽ SET], [Hx12 3 J], [▽ SET], [Hx3 1 H], [Hx1 0 G], [▽ SET] twice, [Hx6 2 I], [▽ SET], [Hx3 1 H], [▽ SET] twice, [Hx6 2 I], [▽ SET] twice, [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Note that in the status field, tracing stopped at level 2 (2 RDY), indicating the time interval was correct (four or more sample clock pulses apart). There is no way to vary the actual time between the pulses; to simulate an incorrect time interval, change the delay on level 1 to four clocks.

Press [TRACE CONTROL], [Hx3 1 H], [▷] twice, [PAGE 4 K], [ARM].

Now notice that tracing stopped on level 8 because 10 came true at SAMPLE COUNT = 4 CLOCKS and therefore satisfied the JUMP condition of level 1.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST #SET UP #519 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AF AB
A T 2	AE AA
S 1	AD A9
LSB	AC A8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions:

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA > D and Sample Count = Delay
5	If DATA < D and Sample Count = Delay
6	If DATA = D and Sample Count > Delay
7	If DATA = D and Sample Count < Delay
8	If DATA ≠ D and Sample Count = Delay

(D = S, J, A, or T, which are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(1) TRACE ALWAYS
T = X X

COMMENTS

TRACE EVERYTHING WHILE LOOKING FOR 01. ADVANCE WHEN IT IS FOUND.

LEVEL 1 (O-F) DELAY = DEC (DEC/HEX) 3 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(7) JUMP TO 8 (O-F) IF DATA = J AND SAMPLE COUNT < = DELAY
J = 1 0

(3) ADVANCE IF DATA = A AND SAMPLE COUNT > DELAY
A = 1 0

(1) TRACE ALWAYS
T = X X

COMMENTS

EVENT 10 SHOULD OCCUR EXACTLY 4 CLOCKS AFTER ENTERING LEVEL 1 AND TRACE CONTROL THEREFORE ADVANCES TO LEVEL 2.

LEVEL 2 (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(1) STOP ALWAYS
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

IF THE TIME BETWEEN 01 AND 10 WAS CORRECT, TRACING ADVANCES TO HERE AND STOPS.

LEVEL 8 (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(1) STOP ALWAYS
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

IF THE TIME BETWEEN 01 AND 10 WAS INCORRECT TRACE CONTROL JUMPS TO HERE AND STOPS.

Figure 10-88. Setup Guide: Check Correct Timing Between Two Events (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.9

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____ + _____ + _____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS; EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = (_____●_____●_____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX — Fixed hex format & CF, A0 sequence
1	OCTAL — Fixed octal format & CF - A0 sequence
2	BINARY — Fixed binary format & CF, A0 sequence
3	MIXED USER SEQN — Any radix, any sequence
4	MIXED CF, A0 SEQN — Any radix, fixed CF, A0 sequence
5	DEVICE MNEMONICS — Fixed disassembled µP code format, only if RTE 816 attached
5	DEVICE NOT AVAILABLE — No RTE 816 attached

CLOCKING NOTES

SAMPLE CLOCK CHOICES

QUICK KEY	
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

ENABLE CLOCK CHOICES

QUICK KEY	
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

MODE & DESCRIPTIONS

0 INTERNAL — All sections are sampled at the internal clock rate. Section A = Section B = Section C = Internal clock period.

1 EXTERNAL SINGLE PHASED — All sections are sampled at the Master external rate. Section A = Section B = Section C = Master (external).

2 EXTERNAL, MULTI PHASED — Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions.

3 MIXED SINGLE PHASED — Master must be external. Each section can be sampled at the Master external rate, Internal clock period, or 10ns. Section A, Section B, and/or Section C = Master (external) or Internal clock period or 10ns.

4 MIXED MULTI PHASED — Master must be external. Each section can be sampled at own external rate, the Master external rate, Internal clock period, or 10ns. Section A, Section B, and/or Section C = Master (external) or Internal or 10ns.

5 INTERNAL EXTENDED — Each section can be sampled at the Internal clock rate or 10ns. Section A, Section B, and/or Section C = Internal clock period or 10ns.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ (CURSORS C: 0-512, R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A > B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A > B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	↕	↕	↕	↕	↕	↕	↕	↕	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
•	POSITIVE
	NEGATIVE

DWS24-12.5183

Figure 10-88. Setup Guide: Check Correct Timing Between Two Events (Sheet 2 of 2).

10.2.5.14 **Continuously Monitor for Correct Operation**

a. Word 02

SET UP: To repeatedly check that word 02 occurs immediately after word 01, see setup guide in Figure 10-89.

Press [TRACE CONTROL], [▽ SET], [Hx6 2 I], [▽ SET] twice, [Hx1 0 G], [▽ SET] twice, [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx3 1 H], [▽ SET], [Hx3 1 H], [▽ SET] twice, [Hx1 0 G], [▷], [Hx1 0 G], [▽ SET], [Hx1 0 G], [Hx6 2 I], [▽ SET], [Hx1 0 G], [▽ SET], [DON'T CARE * SPACE] twice.

RECORD: Press [ARM].

REVIEW: Watch the trace level status field; it should alternate between 0 BUSY and 1 BUSY (the changing of the 0 and 1 may be difficult to detect). If and when an error occurs, it will go to 2 RDY. When it does,

Press [SHIFT], [◁ SET], [V24 5 L], [Hx1 0 G], [Hx1 0 G], [DATA].

See Figure 10-90 for an example. In Figure 10-90 the word 02 should have occurred after word 01. Since it did not, tracing was halted. (The exact erroneous word will vary for each machine and recording, as well as the amount of elapsed time before an error occurs.)

K101-D SET UP GUIDE

5.1.10(1)

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # __ OF __ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AE AB
A T 2	AE AA
S 1	AD A9
LSB	AC A8

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All true TRACE commands in each level cause the trace at any given time
Quick Key — Command Condition
0 If DATA = D
1 Always
2 Never
3 If DATA = D and Sample Count = Delay
4 If DATA = D and Sample Count = Delay
5 If DATA = D and Sample Count = Delay
6 If DATA = D and Sample Count = Delay
7 If DATA = D and Sample Count = Delay
8 If DATA = D and Sample Count = Delay
ID = S, J, A, or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(0) TRACE IF DATA = T
T = 0 1

COMMENTS

WAIT FOR 01 - TRACE IT AND ADVANCE.

LEVEL 1 (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(0) JUMP TO 0 (O-F) IF DATA = J
J = X X

(0) ADVANCE IF DATA = A
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

EVENT 02 SHOULD OCCUR IMMEDIATELY UPON ENTERING LEVEL 1. IF SO, JUMP BACK. IF NOT, ADVANCE. TRACE THE EVENT THAT DOES OCCUR.

LEVEL 2 (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(1) STOP ALWAYS
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

TRACE CONTROL COMES HERE AND STOPS ONLY IF 02 DID NOT OCCUR RIGHT AFTER 01.

LEVEL ____ (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL ____ (O-F)

(____) STOP
S =

(____) JUMP TO ____ (O-F)
J =

(____) ADVANCE
A =

(____) TRACE
T =

COMMENTS

Figure 10-89. Setup Guide:Continuously Monitor for Correct Operation (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.10 (1)

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____
☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX — Fixed hex format & CF-A0 sequence
1	OCTAL — Fixed octal format & CF-A0 sequence
2	BINARY — Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN — Any radix, any sequence
4	MIXED CF-A0 SEQN — Any radix, fixed CF A0 sequence
5	DEVICE MNEMONICS — Fixed disassembled µP code format, only if RTE-816 attached OR
6	DEVICE NOT AVAILABLE — No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL — All sections are sampled at the internal clock rate. Section A = Section B = Section C = Internal clock period
1	EXTERNAL SINGLE PHASED — All sections are sampled at the Master external rate. Section A = Section B = Section C = Master (external)
2	EXTERNAL MULTI-PHASED — Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external inputs/ons
3	MIXED SINGLE PHASED — Master must be external. Each section can be sampled at the Master external rate, internal clock period, or 10ns. Section A, Section B and/or Section C = Master (external) or internal clock period or 10ns
4	MIXED MULTI-PHASED — Master must be external. Each section can be sampled at own external rate, the Master external rate, internal clock period or 10ns. Section A, Section B, and/or Section C = Master (external) or internal or 10ns
5	INTERNAL EXTENDED — Each section can be sampled at the internal clock rate or 10ns. Section A, Section B and or Section C = Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	↕	↕	↕	↕	↕	↕	↕	↕	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

DWS24-12.5183

Figure 10-89. Setup Guide:Continuously Monitor for Correct Operation (Sheet 2 of 2).

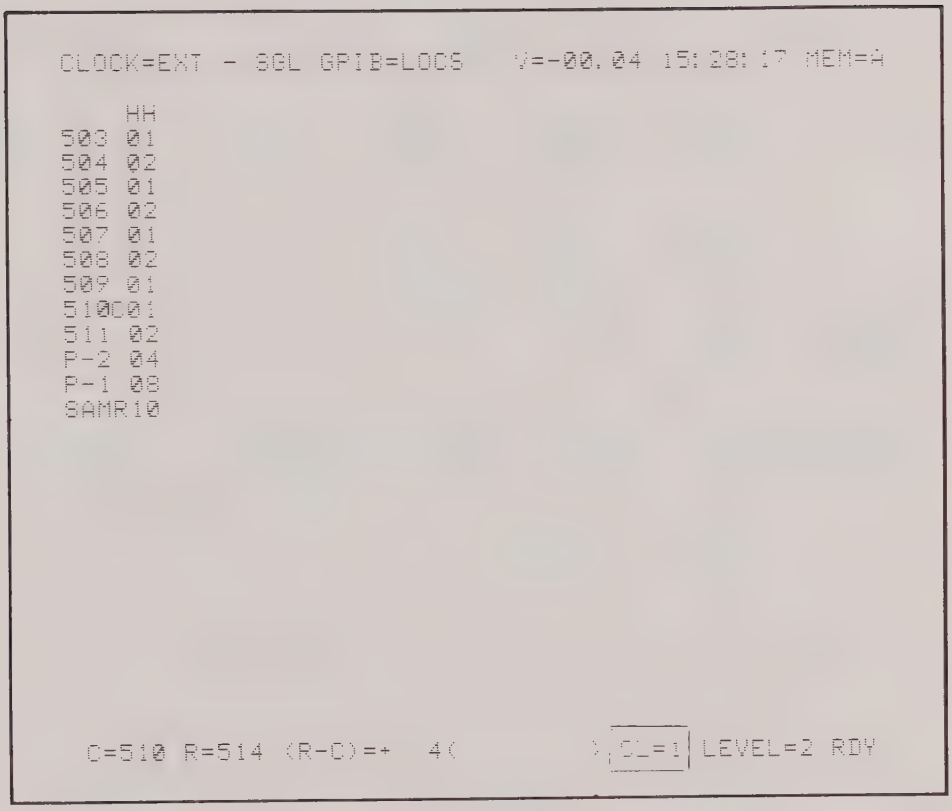


Figure 10-90. Tracing Halted.

b. Word 80

SET UP: To repeatedly check that word 80 occurs within the proper time interval (seven clocks) from the occurrence of 01, see setup guide in Figure 10-91.

Press [TRACE CONTROL], [Hx3 1 H], [▷], twice, [V6 7 N], [▽ SET] twice, [Hx1 0 G], [▷], [V6 7 N], [▽ SET], [PAGE 8 O TTL], [Hx1 0 G], [▽ SET], [Hx12 3 J].

RECORD: Press [ARM].

REVIEW: Watch the trace level status field. Again, it should toggle between 0 BUSY and 1 BUSY. If and when an error occurs, it will go to 2 RDY.

Press [DATA] to see the cause of the error, as in Figure 10-92. Because an extra sample (40) occurred between 01 and 80, the time interval between them was in error and tracing stopped.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.1.10 (2) OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

TRACE CONTROL NOTES

RADIX: H H

	MSB	
	I 6	
D	N 5	
A	P 4	
T	U 3	AE AD
A	T 2	AE AA
	S 1	AD A9
	LSB	AC A8

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL

LEVEL 0 (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(0) TRACE IF DATA = T
T = 0 1

COMMENTS
WAIT FOR 01, TRACE IT AND ADVANCE WHEN IT OCCURS.

LEVEL 1 (O-F) DELAY = DEC 7 (DEC/HEX) ___ (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(7) JUMP TO 0 (O F) IF DATA = J AND SAMPLE COUNT < = DELAY
J = 8 0

(3) ADVANCE IF DATA = A AND SAMPLE COUNT > DELAY
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS
EVENT 80 SHOULD OCCUR EXACTLY 7 CLOCKS AFTER EVENT 01. IF SO, JUMP BACK. IF NOT, ADVANCE, TRACE EVERYTHING THAT HAPPENS BETWEEN 01 AND 80.

LEVEL 2 (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(1) STOP ALWAYS
S = X X

(2) JUMP TO 0 (O F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS
IF THIS LEVEL IS REACHED, A TIMING ERROR OCCURED.

STOP.

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(____) STOP
S = _____

(____) JUMP TO ___ (O F)
J = _____

(____) ADVANCE
A = _____

( ) TRACE
T = _____

COMMENTS

Figure 10-91. Setup Guide: Repeatedly Check Word 80 (Sheet 1 of 2).

K101-D SET UP GUIDE 5.1.10(2)

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence
1	OCTAL Fixed octal format & CF-A0 sequence
2	BINARY Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE 816 attached OR
5	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
≡	↑ ACTIVE RISING EDGE
≡	↓ ACTIVE FALLING EDGE
≡	|– – –| NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	|– – –| NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate Section A = Section B = Section C = Internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A = Section B = Section C = Master external
2	EXTERNAL MULTI PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, Internal clock period or 10ns. Section A, Section B and/or Section C = Master external or Internal clock period or 10ns
4	MIXED MULT. PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, Internal clock period or 10ns. Section A, Section B and/or Section C = Master external or Internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the Internal clock rate or 10ns. Section A, Section B and/or Section C = Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A < B WITHIN LIMITS
5	AUTO STOP IF A > B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	↕	↕	↕	↕	↕	↕	↕	↕	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 10-91. Setup Guide: Repeatedly Check Word 80 (Sheet 2 of 2).

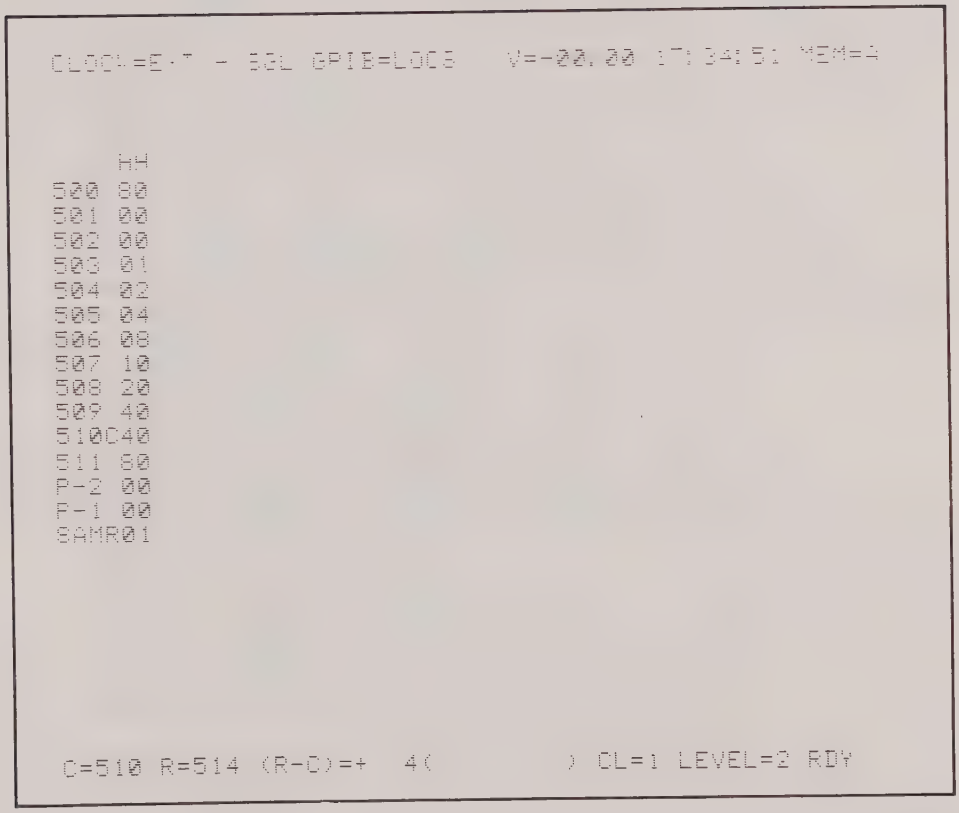


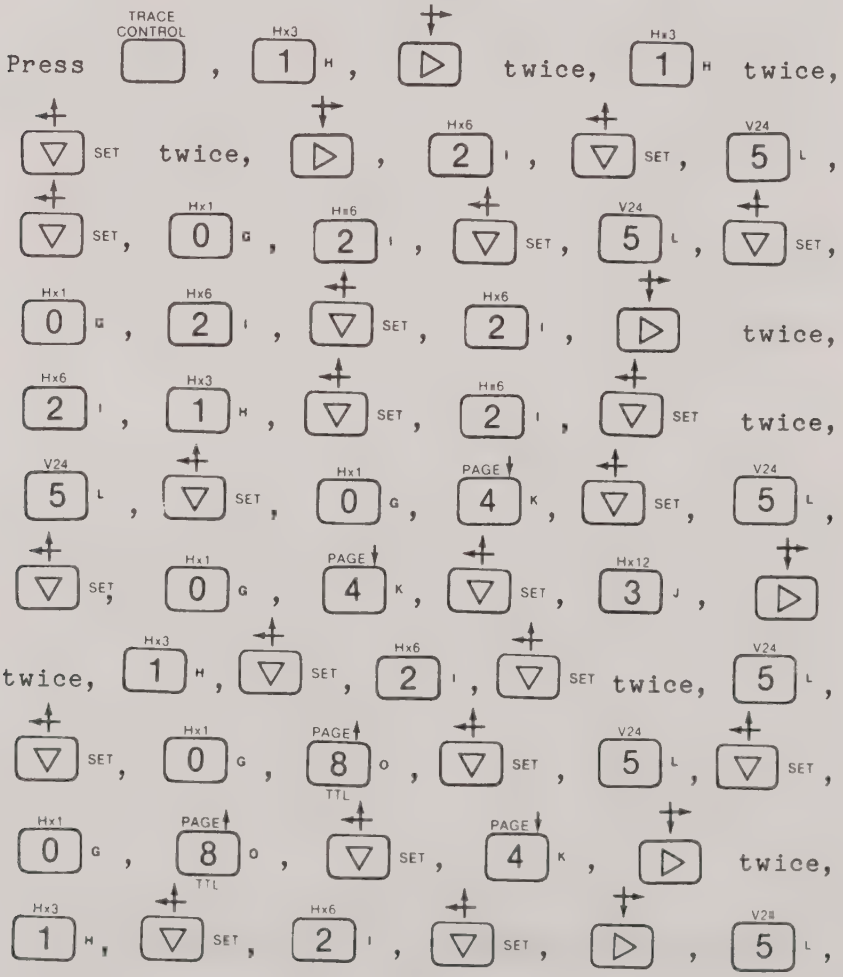
Figure 10-92. Time Interval Error, Tracing Stopped.

10.2.6 ADVANCED TRACE CONTROL

Combining and varying the basic building blocks let you create more complex and powerful trace control programs. The following examples will illustrate some of the more advanced trace control capabilities.

10.2.6.1 **Continuously Check Execution Path and Timing**

SET UP: To check that certain words occur in their expected sequence as well as within their expected time interval, see setup guide in Figure 10-93.


Press TRACE CONTROL , Hx3 1 H , ▷ twice, Hx3 1 H twice,
▽ SET twice, ▷ , Hx6 2 I , ▽ SET , V24 5 L ,
▽ SET , Hx1 0 G , Hx6 2 I , ▽ SET , V24 5 L , ▽ SET ,
Hx1 0 G , Hx6 2 I , ▽ SET , Hx6 2 I , ▷ twice,
Hx6 2 I , Hx3 1 H , ▽ SET , Hx6 2 I , ▽ SET twice,
V24 5 L , ▽ SET , Hx1 0 G , PAGE 4 K , ▽ SET , V24 5 L ,
▽ SET , Hx1 0 G , PAGE 4 K , ▽ SET , Hx12 3 J , ▷
twice, Hx3 1 H , ▽ SET , Hx6 2 I , ▽ SET twice, V24 5 L ,
▽ SET , Hx1 0 G , PAGE 8 O TTL , ▽ SET , V24 5 L , ▽ SET ,
Hx1 0 G , PAGE 8 O TTL , ▽ SET , PAGE 4 K , ▷ twice,
Hx3 1 H , ▽ SET , Hx6 2 I , ▽ SET , ▷ , V24 5 L ,

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 5.2.1 OF ___ DATE _____

QUICK KEY (See back for notes) (.....) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AF A8
A T 2	AE A4
S 1	AD A2
LSB	AC A0

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four TRACE commands in each level are combined in some logical fashion
QUICK KEY Command Definition
0 = DATA D
1 = Always
2 = Never
3 = DATA = D and Sample Count = Delay
4 = DATA = D and Sample Count = Delay
5 = DATA = D and Sample Count = Delay
6 = DATA = D and Sample Count = Delay
7 = DATA = D and Sample Count = Delay
8 = DATA = D and Sample Count = Delay
(D = 5 - A or T were previously assigned by command level)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(2.) STOP NEVER
S = X X
(2.) JUMP TO ___ (O-F) NEVER
J = X X
(0.) ADVANCE IF DATA = A
A = 0 1
(0.) TRACE IF DATA = T
T = 0 1

COMMENTS
BEGIN AT KNOWN STARTING POINT.

LEVEL 1 (O-F) DELAY = DEC (DEC/HEX) 11 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(2.) STOP NEVER
S = X X
(2.) JUMP TO 0 (O-F) NEVER
J = X X
(5.) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 2
(5.) TRACE IF DATA = T AND SAMPLE COUNT = DELAY
T = 0 2

COMMENTS
02 SHOULD OCCUR 1 CYCLE AND 1 WORD LATER.

LEVEL 2 (O-F) DELAY = DEC (DEC/HEX) 21 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(2.) STOP NEVER
S = X X
(2.) JUMP TO 0 (O-F) NEVER
J = X X
(5.) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 4
(5.) TRACE IF DATA = T AND SAMPLE COUNT = DELAY
T = 0 4

COMMENTS
04 SHOULD OCCUR 2 CYCLES AND 1 WORD LATER.

LEVEL 3 (O-F) DELAY = DEC (DEC/HEX) 1 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

QUICK KEY
(2.) STOP NEVER
S = X X
(2.) JUMP TO 0 (O-F) NEVER
J = X X
(5.) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 8
(5.) TRACE IF DATA = A AND SAMPLE COUNT = DELAY
T = 0 8

COMMENTS
08 IS NEXT IMMEDIATE WORD.

Figure 10-93. Setup Guide: Continuously Check Execution Path and Timing (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST (CONTINUED) SET UP # 5.2.1 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3 AEAB
A T 2 AEAA
S 1 ADA9
LSB ACA8

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count = Delay
4	If DATA = D and Sample Count < Delay
5	If DATA = D and Sample Count > Delay
6	If DATA = D and Sample Count > = Delay
7	If DATA = D and Sample Count < = Delay
8	If DATA = D and Sample Count ≠ Delay

(D = S, J, A, or T, which are assigned by command type.)

TRACE CONTROL

LEVEL 4 (O-F) DELAY = DEC (DEC/HEX) 1 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(5) JUMP TO 0 (O-F) IF DATA = J AND SAMPLE COUNT = DELAY
J = 1 0

(5) ADVANCE IF DATA = J AND SAMPLE COUNT = DELAY
A = X X

(0) TRACE IF DATA = T
T = 1 0

COMMENTS

BOTH JUMP AND ADVANCE ARE TRUE SIMULTANEOUSLY, BUT JUMP HAPPENS 1st, SO IT CONTINUOUSLY LOOPS BETWEEN LINK 0, 1, 2, 3, 4.

LEVEL 5 (O-F) DELAY = DEC (DEC/HEX) 515 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

THIS LEVEL SHOULD NEVER BE REACHED.

LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

Figure 10-93. Setup Guide: Continuously Check Execution Path and Timing (Sheet 2 of 2).

[▽ SET], [Hx3 1 H], [Hx1 0 G], [▽ SET], [V24 5 L], [▽ SET]

twice, [Hx1 0 G], [▽ SET], [Hx3 1 H], [Hx1 0 G].

RECORD: Press [ARM].

REVIEW: Watch the trace level status field continuously sequence through LEVEL = 0, 1, 2, 3, 4 BUSY as the conditions on each level are satisfied and the commands executed.

Note

If an error occurs in the generation or clocking of the Probe Test pattern, the trace program will get hung up (as indicated by a steady LEVEL = n BUSY) because the expected word on that level did not happen when it should have.

Press [M→A].

The recording will most likely stop on level 2 since more time is spent in that level than the others.

Press [SHIFT], [◁ SET], [V24 5 L], [Hx1 0 G], [Hx1 0 G], [DATA].

Your display should look like Figure 10-94. The trace program repeatedly captures only one word on each of five levels until manually stopped.

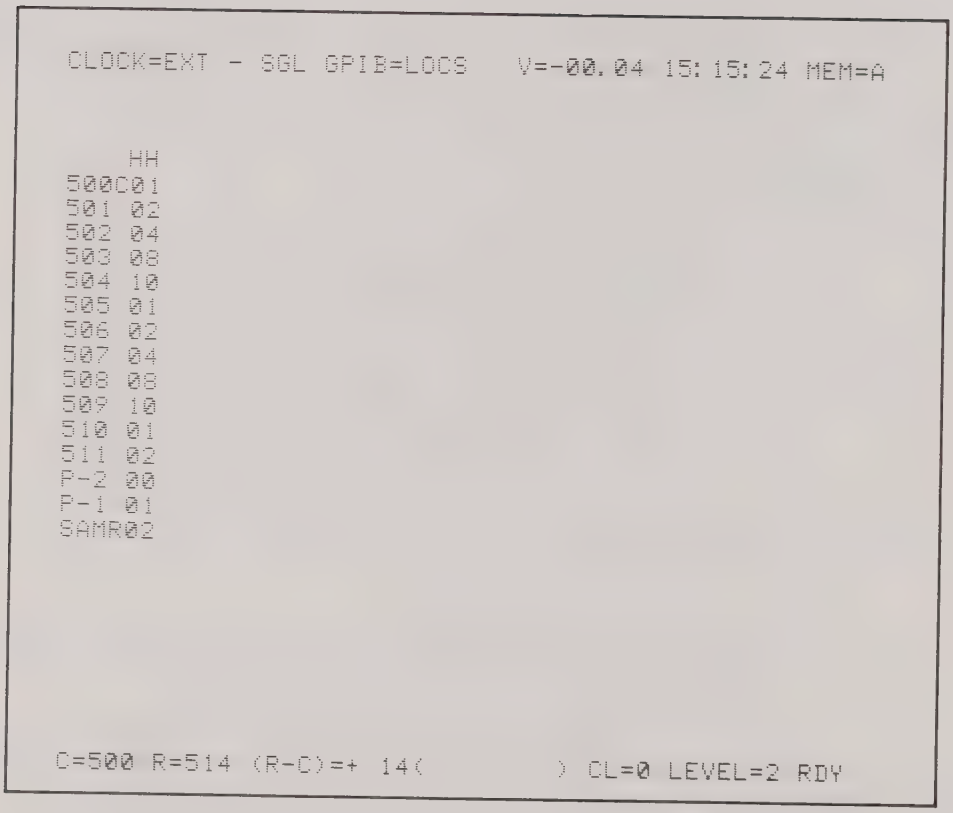


Figure 10-94. Capture One Word on Each Level until Stopped.

Press [▷] slowly and

notice that 01 is captured by level 0; one cycle (ten sample clocks) and one sample later 02 is captured by level 1; two cycles and one sample later 04 is captured by level 2; one sample later 08 is captured by level 3; one sample later 10 is captured by level 4; then the whole process repeats. Figure 10-95 shows the exact words that were traced by this program out of all the words that were sampled. Note that of all the samples being evaluated by trace control, only certain samples will be transferred into memory.

10.2.6.2 **Trace Independently of the Execution Path**

SET UP: Change the trace control setup on level 2.

Press [TRACE CONTROL] , [Hx6 / 2 I] , [▽ SET] five times, [Hx1 / 0 G] ,

[▽ SET] , [PAGE / 8 O TTL] , [Hx1 / 0 G] .

RECORD: Press [ARM] .

REVIEW: Press [M→A] , [SHIFT] , [◁ SET] , [PAGE / 4 K] , [EBCDIC / 9 P ECL] ,

[Hx3 / 1 H] , [DATA] .

Your display will look similar to Figure 10-96. Taking the same execution path as before, different samples are selected to be recorded.

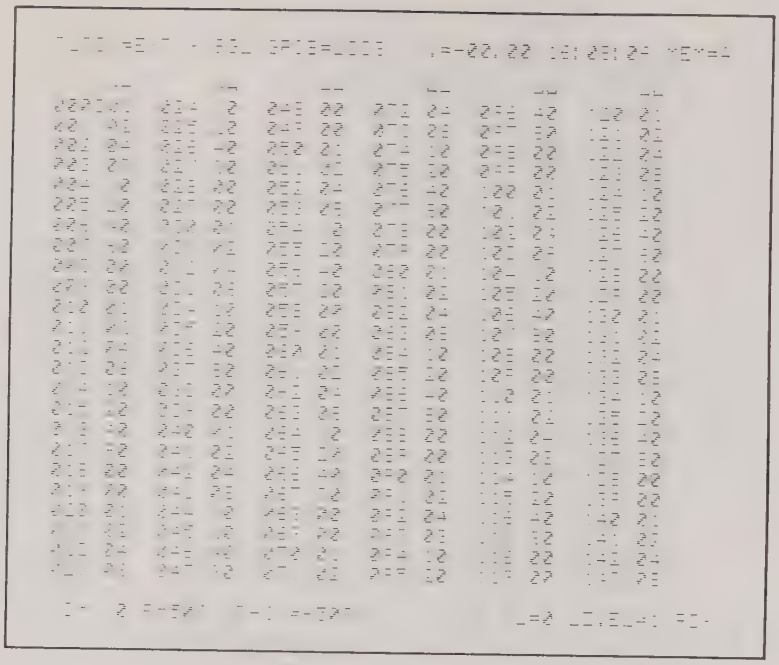


Figure 10-95. Transfer Certain Samples into Memory.

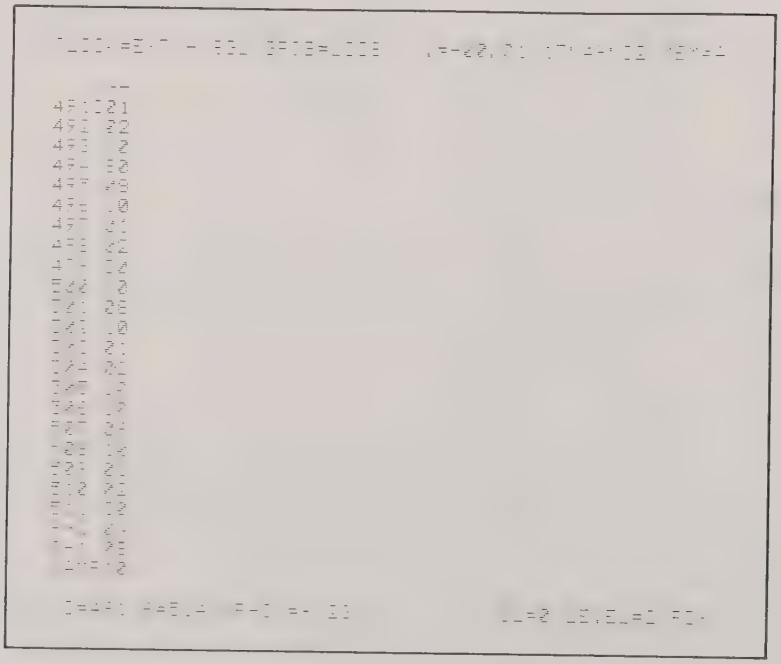


Figure 10-96. Changing Sample Selection.

Press until CL = 2.

Level 2 still checks for and advances on the second occurrence of 04, but it now traces the two occurrences of 80 that happen while waiting for ADVANCE to come true (see Figure 10-97). While waiting for the level 2 ADVANCE condition to come true, two occurrences of 80 are traced. The TRACE command and its T word recognizer do not have to be the same as any of the other commands and their word recognizers. The words you choose to record don't have to be the same as the words that define the execution path to be followed.

10.2.6.3 **End Level Breakpoint**

SET UP: Change the trace control program end level to 3.

Press

.

Press , then

repeatedly to verify that the end level you set applies to all 16 levels.

RECORD: Press

.

REVIEW: Press

, and use to move the Control Cursor to location 511 (Figure 10-98). Note that though the last sample traced occurred in level 3, end level 3 forces an advance to level 4 and stops the recording there.

Note that the last word was traced by level 3 (CL = 3) and the recording stopped on level 4 (LEVEL = 4 RDY), although none of the level 4 commands were performed. Setting end level to n (where n is a level used in the current program) causes trace control to advance to level

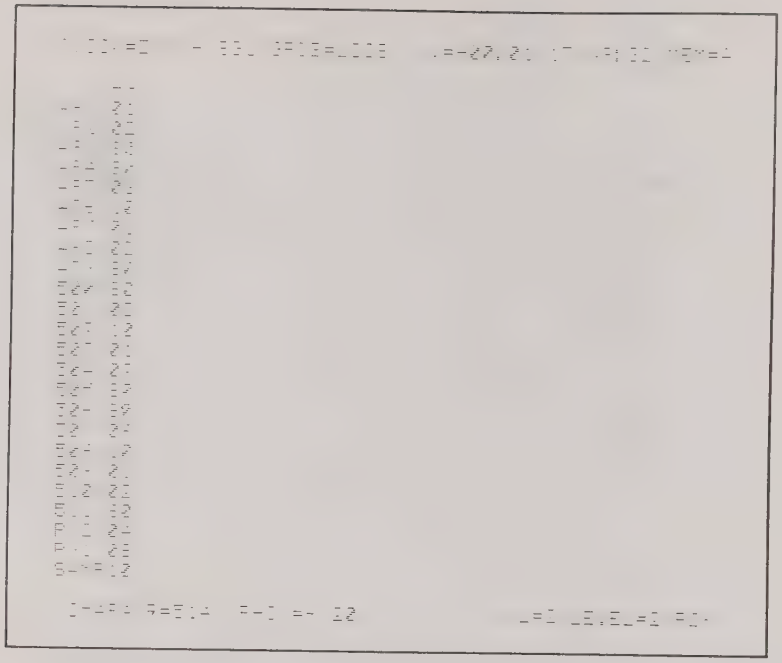


Figure 10-97. Record While Waiting.

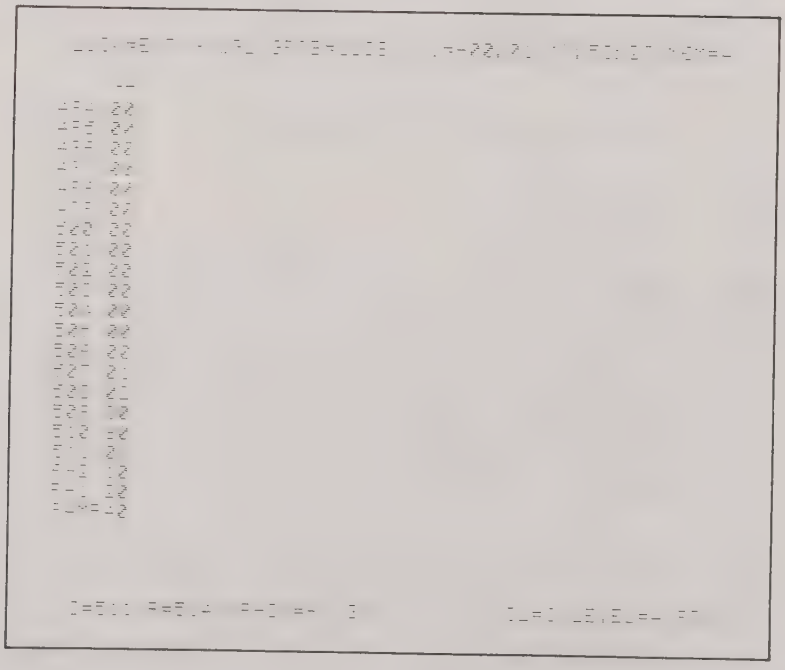


Figure 10-98. End Level 3 Forces.

n + 1, regardless of the commands on level n, and stop on level n + 1 without performing any of the commands on n + 1. In this way, end level can be used as a breakpoint to check out segments of your trace control program.

10.2.6.4 **Segments, Patterns, and Total Trace Time**

SET UP: See setup guide in Figure 10-99.

Press [TRACE CONTROL], [Hx3 1 H], [▷], twice, [V12 6 M], [V24 5 L],
[Hx1 0 G], [Hx1 0 G], [Hx1 0 G], [▷], [Hx3 1 H], [▷],
[DEMUX HEX F V], [▷], [Hx6 2 I], [▷] twice, [Hx3 1 H],
[Hx1 0 G], [Hx3 1 H], [▽ SET] five times, [Hx6 2 I], [▽ SET],
[Hx12 3 J], [▽ SET], [Hx3 1 H].

RECORD: Press [ARM].

REVIEW: Notice that the trace level status word remains at 1 BUSY for a moment before going to 3 RDY.

Press [SHIFT], [◁ SET], [V24 5 L], [Hx1 0 G], [V24 5 L],
[Hx3 1 N], [▷] six times.

Your display should look like Figure 10-100.

Press [TIMING] and note the total trace time of 2 micro-

seconds. This is because trace control was only enabled to record one word on levels 0, 1, and 2. Change trace control to trace every occurrence of the level 2 A pattern.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 524 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB
I 6
D N 5
A P 4
T U 3
A T 2
S 1
LSB

A F A 8
A E A A
A D A 9
A C A 8

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions:

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA ≠ D and Sample Count = Delay
4	If DATA = D and Sample Count = Delay
5	If DATA ≠ D and Sample Count = Delay
6	If DATA = D and Sample Count > Delay
7	If DATA = D and Sample Count < Delay
8	If DATA = D and Sample Count ≠ Delay

(D = S, J, A, or T, which are assigned by command type.)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(0) ADVANCE IF DATA = A
A = 0 1

(0) TRACE IF DATA = T
T = 0 1

COMMENTS
WAIT FOR 01, TRACE IT AND ADVANCE WHEN IT OCCURS.

LEVEL 1 (O-F) DELAY = DEC 65000 (DEC/HEX) (0-65 K) A PATTERNS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 2

(5) TRACE IF DATA = T AND SAMPLE COUNT = DELAY
T = 0 2

COMMENTS
WAIT FOR THE 65000 TH OCCURANCE OF EVENT 02. TRACE ONLY THAT LAST OCCURANCE AND THEN ADVANCE.

LEVEL 2 (O-F) DELAY = DEC (DEC/HEX) 101 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2) STOP NEVER
S = X X

(2) JUMP TO 0 (O-F) NEVER
J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 4

(2) TRACE NEVER
T = 0 4

COMMENTS
DON'T TRACE ANYTHING WHILE CHECKING FOR EVENT 04 WHICH SHOULD OCCUR EXACTLY 101 CLOCKS AFTER LEAVING THE LAST LEVEL.

LEVEL 3 (O-F) DELAY = DEC 1 (DEC/HEX) (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(1) STOP ALWAYS
S = X X

(2) JUMP TO 0 (O F) NEVER
J = X X

(5) ADVANCE IF DATA = A AND SAMPLE COUNT = DELAY
A = 0 8

(5) TRACE IF DATA = T AND SAMPLE COUNT = DELAY
T = 0 8

COMMENTS
CHECK THAT EVENT 08 OCCURS IMMEDIATELY UPON ENTERING THIS LEVEL. IF IT DOES, TRACE IT. STOP RECORDING, THE ADVANCE COMMAND SHOULD NOT BE EXECUTED WHEN IT COMES TRUE AS STOP TAKES PRIORITY.

Figure 10-99. Setup Guide: Segments, Patterns, and Total Trace Time (Sheet 1 of 2).

K101-D SET UP GUIDE 5.2.4

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXTERNAL SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS

EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX — Fixed hex format & CF-A0 sequence
1	OCTAL — Fixed octal format & CF-A0 sequence
2	BINARY — Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN — Any radix any sequence
4	MIXED CF A0 SEQN — Any radix fixed CF-A0 sequence
5	DEVICE MNEMONICS — Fixed disassembled µP code format, only if RTE-816 attached OR DEVICE NOT AVAILABLE — no RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL — All sections are sampled at the internal clock. Are Section A = Section B = Section C = internal clock period
1	EXTERNAL SINGLE PHASED — All sections are sampled at the Master external rate. Section A = Section B = Section C = Master external
2	EXTERNAL MULTI-PHASED — Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master M can be different external expressions
3	MIXED SINGLE PHASED — Master must be external. Each section can be sampled at the Master external rate or internal rate. Internal clock period = 10ns. Section A, Section B and/or Section C = Master external or internal clock period or 10ns
4	MIXED MULTI PHASED — Master must be external. Each section can be sampled at own external rate or the Master external rate or internal clock period = 10ns. Section A, Section B and/or Section C = Master external or internal or 10ns
5	INTERNAL EXTENDED — Each section can be sampled at the internal clock rate or 10ns. Section A, Section B and/or Section C = internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0	SAMPLE	ECL	-1.30

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ (CURSORS C: 0-512 R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	±	±	±	±	±	±	±	±	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

DWS24-12.5183

Figure 10-99. Setup Guide: Segments, Patterns, and Total Trace Time (Sheet 2 of 2).

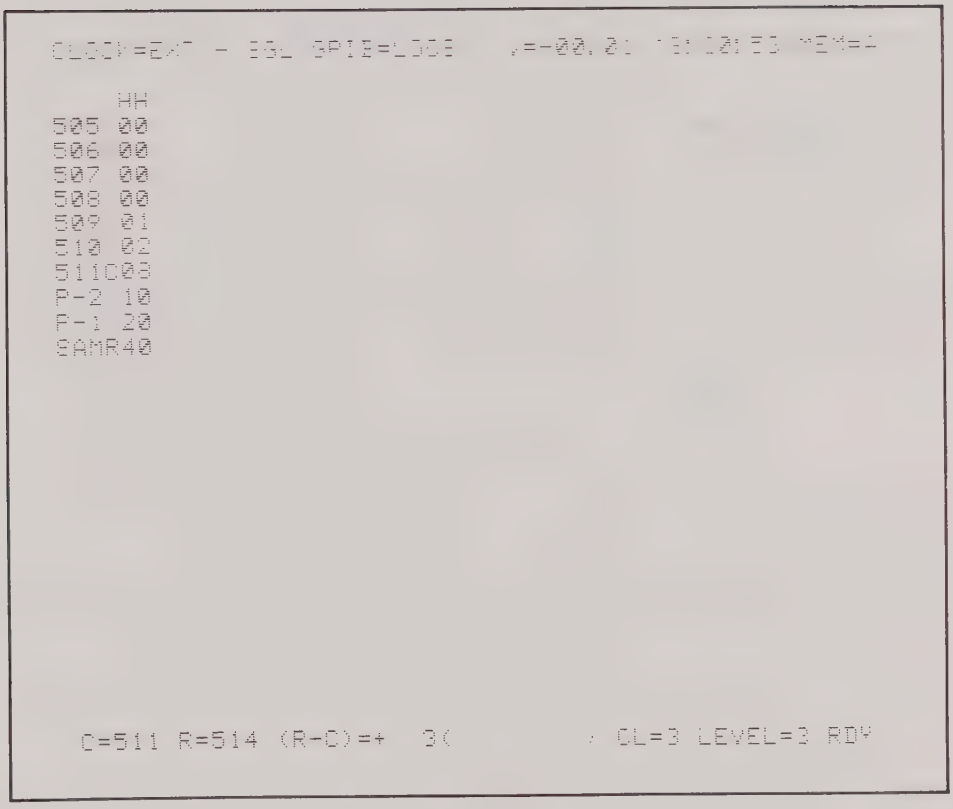


Figure 10-100. Only Three Words are Traced into Memory.

Press [TRACE CONTROL] , [Hx3 1 H] , [▽ SET] five times, [Hx1 0 G] .

Press [ARM] , [TIMING] .

Note that the total trace time is now (typically) 65.26 milliseconds.

10.2.7 RECORD

10.2.7.1 **Manual Arm**

SET UP: See setup guide in Figure 10-101.

Press [TRACE CONTROL] , [▽ SET] , [Hx12 3 J] , [▽ SET] , [Hx1 0 G] ,
[Hx3 1 H] , [▽ SET] twice, [Hx6 2 I] , [▽ SET] twice, [Hx3 1 H] ,
[INPUT MODE] , [△] twice, [▷] , [PAGE↑ 8 O TTL] .

RECORD: Press [ARM] .

The instrument makes a single recording for each manual press of [ARM] . This allows you to take all the time you need to review and analyze each recording.

REVIEW: Press [SHIFT] , [◁ SET], [Hx1 0 G] , [TIMING] , [Hx12 3 J] (and [PAGE↓ 4 K] or [PAGE↑ 8 O TTL] as necessary to be on Page 4).

Your display should look like Figure 10-102 which is a timing display of a Probe Test recording. Manual recording allows unlimited time to review and analyze a display.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM PROBE TEST SET UP # 6.1 OF ___ DATE _____

QUICK KEY (See back for notes) (3) DATA FORMAT MIXED USER SEQN.

RADIX: H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	AFAB
A T 2	AEAA
S 1	ADA9
LSB	ACA8

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level –
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA - D
1	Always
2	Never
3	If DATA = D and Sample Count - Delay
4	If DATA ≠ D and Sample Count - Delay
5	If DATA > D and Sample Count - Delay
6	If DATA < D and Sample Count - = Delay
7	If DATA ≥ D and Sample Count - ≥ Delay
8	If DATA ≤ D and Sample Count - ≤ Delay

(D = S, J, A, or T which are assigned by command type)

TRACE CONTROL

LEVEL 0 (O-F) DELAY = DEC 515 (DEC/HEX) CLOCKS (0-65 K CLOCKS/A PATTERNS) END LEVEL F (O-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY
S = 0 1

(2) JUMP TO 0 (O-F) NEVER
J = X X

(2) ADVANCE NEVER
A = X X

(1) TRACE ALWAYS
T = X X

COMMENTS

FILL MEMORY AND STOP THE NEXT TIME 0.1 OCCURS.

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP
S =

(.....) JUMP TO ___ (O-F)
J =

(.....) ADVANCE
A =

(.....) TRACE
T =

COMMENTS

Figure 10-101. Setup Guide: Manual Arm (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # 6.1 OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (1) MODE = EXT. SINGLE-PHASED

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____ ☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)

MASTER = ☐ INTERNAL ■ EXT (_____●_____●AJ ↓) + (_____+_____+_____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ■ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

CR BR AR CS BS AS

SECTION C = (_____●_____●_____) + (_____+_____+_____)

SECTION B = (_____●_____●_____) + (_____+_____+_____)

SECTION A = (_____●_____●_____) + (_____+_____+_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence
1	OCTAL Fixed octal format & CF A0 sequence
2	BINARY Fixed binary format & CF-A0 sequence, .
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE-816 attached OR
6	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the internal clock rate. Section A = Section B = Section C = Internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A = Section B = Section C = Master (external)
2	EXTERNAL MULTI PHASED Each section can be sampled at user-selectable rates. Master external rate: Section A, Section B, Section C & Master (Section B only will maintain expressions
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate or internal clock period, or 10ns. Master external rate = internal clock period, or 10ns. Section A, Section B and/or Section C = Master (external) or internal clock period or 10ns.
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at its own external rate, the Master external rate, internal clock period, 10ns. Section A, Section B, Section C = Master (external) or internal clock period or 10ns.
5	INTERNAL EXTENDED Each section can be sampled at the internal clock rate or 10ns. Section A, Section B, Section C = Master (internal) or internal clock period or 10ns.

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	ECL	-1.30
A7 — A0			

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A < B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A > B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	+	+	+	+	+	+	+	+	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

DWS24-12.5183

Figure 10-101. Setup Guide: Manual Arm (Sheet 2 of 2).

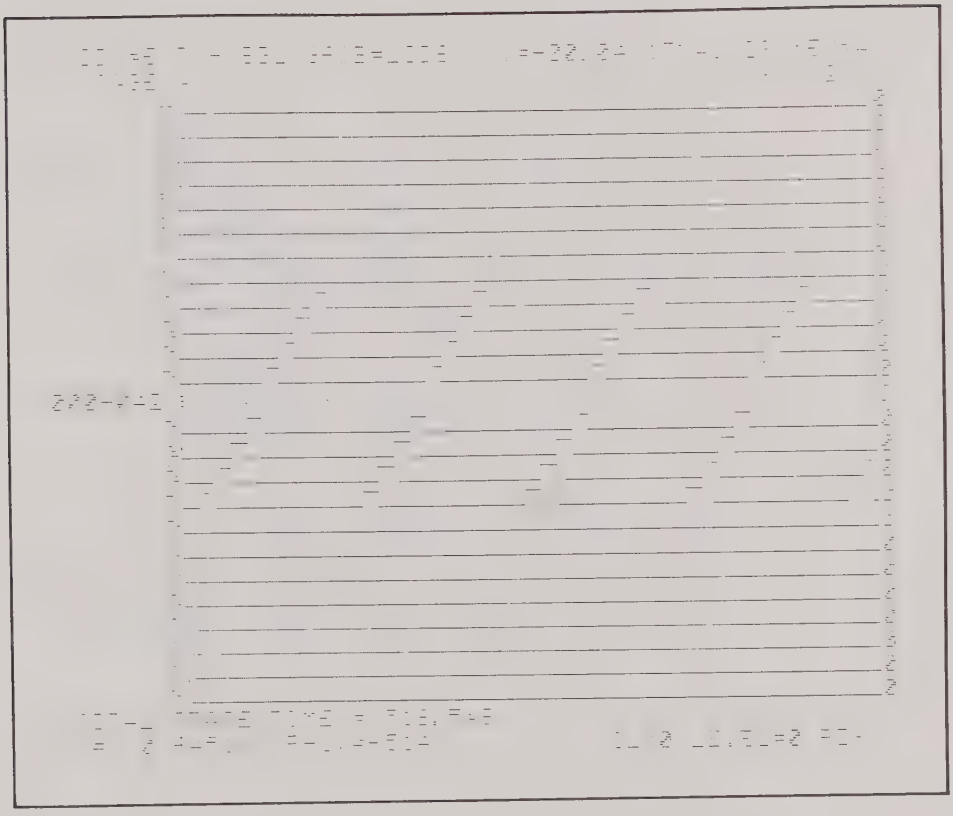


Figure 10-102. Probe Test Timing Display.

10.2.7.2 **Auto Arm**

SET UP: To avoid repeatedly pressing [ARM] by hand when you need to make multiple recordings, change the arm mode to Auto.

Press [INPUT MODE] , [△] , [Hx3 1 H] .

RECORD: Press [ARM] .

Watch the trace control level and status words. LEVEL = alternates between * and 0. The current trace level and number of the current recording are indicated in the bottom status field. A cumulative count of completed recordings is displayed in the upper right of the Input Mode screen (see Figure 10-103). While this automatic rearming and recording process is going on you can press any DISPLAY or SPECIFY key at any time.

Note

It is possible to change a setup parameter of Specify screen during auto recordings. However, to ensure that the change is accepted, press [STOP] , make the change, then press [ARM] .

Press [DATA] , [TIMING] , [GRAPH] .

Observe several recording cycles in each display mode. Press the other DISPLAY keys to see their effect.

This process can continue indefinitely as long as the trace control conditions of each recording are satisfied. If an expected STOP, JUMP, or ADVANCE command condition

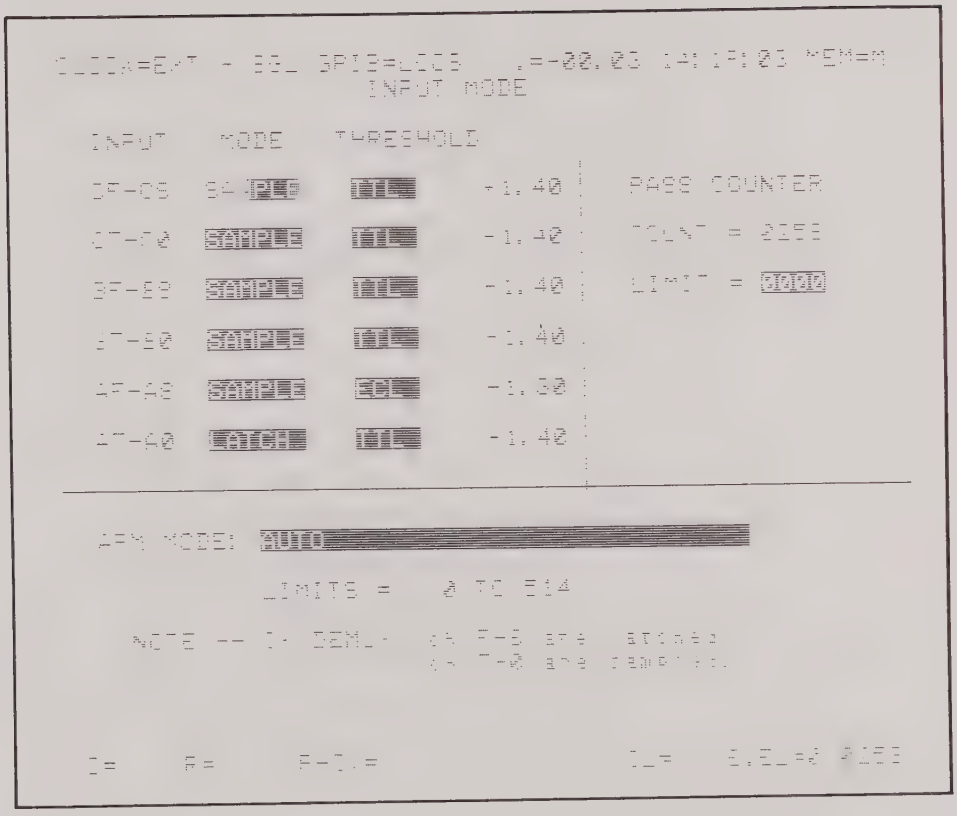


Figure 10-103. Status Field Display.

is not met, the process stops. The level message displays the number of the "stuck" trace level and the count stays at the count of the current hung up recording. If and when the condition comes true, the auto arming and count resume where they left off. Similarly, loss of an external clock input causes a halt. To simulate such an error, unplug the probe from the test socket. Note that the trace status says F CLK? because the expected external sample clock is absent. Plug the probe back in. The recordings and count will resume.

To completely halt the process you must press [STOP] or [M→A]. Press [STOP].

REVIEW: Notice that the trace status word has gone to RDY. The total number of recordings you made can be seen by pressing **INPUT MODE** (see Figure 10-104). The trace status word RDY indicates the completion of an auto arming recording cycle. The total number of recordings made is held until a new arm cycle is begun. If you press **ARM** again, the count initializes to zero and the process begins again.

10.2.7.3 **Limiting the Count**

SET UP: Set a limit of 100 cycles.

Press [INPUT MODE], [▷] twice, [Hx3 1]H, [Hx1 0]G twice.

Setting a limit on the pass counter stops automatic recordings when that limit is reached. If all 100 recordings are successful (i.e., do not fail or get hung up) then you can be reasonably confident your system will not fail more than 1 time out of 100. Confidence that

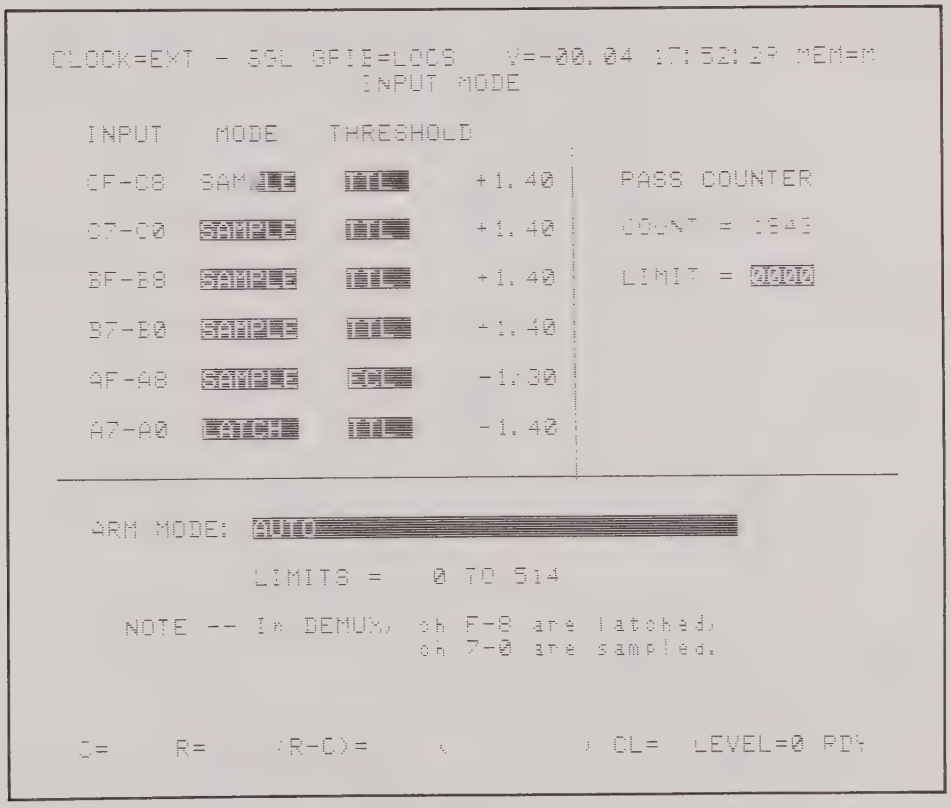


Figure 10-104. Completion of Auto Arming Recording Cycle.

your system is truly operational and debugged comes from obtaining successful test results over numerous recordings.

RECORD: Press [ARM] and observe the count.

It continues until 100 recordings have been made and then stops (see Figure 10-104a and 10-104b) as long as each test is successful. Remove the count limit.

Press [INPUT MODE] , [▷] twice, [Hx1 0 G] .

10.2.7.4 **Stop if A ≠ B**

SET UP: Press [INPUT MODE] , [△] , [Hx12 3 J] .

To load memory B with a known "good" recording, press [A→B] .

RECORD: Press [ARM] .

New recordings are continually compared to the contents of B in search of any unknown or intermittent errors. This process is sometimes referred to as "baby-sitting." Observe the count. To create an "error" or difference between the current and stored recording, edit the B memory.

Press [DATA] , [B] , [EDIT] , [▽ SET] , [Hx3 1 H] , [EDIT] .

The process stops since A and B are now unequal.

REVIEW: Press [COMPARE A/B] .

The display should look like Figure 10-105. Any difference between the current and reference recording will stop the automatic arming process. To see the number of recordings and comparisons made before the "error" occurred,

press [INPUT MODE] .

ALTERNATE

SET UP: An alternate method of comparing recordings is to change Clock Select display to the following:

MODE = INTERNAL

INTERNAL CLOCK PERIOD = 40 NANOSECONDS

Press [CLOCK SELECT] , [Hx1 0 G] , [▽ SET] , [PAGE 4 K] , [Hx1 0 G] .

RECORD: Press [ARM] .

The instrument will make one recording and stop. Press [A→B] to load memory B.

Press [ARM] again.

Even though the trace control routine is identical, samples are now being taken asynchronously. It is therefore unlikely that every sample will be taken at exactly the same place in the pattern as in the previous recording. Therefore, auto arming will probably stop after only one recording.

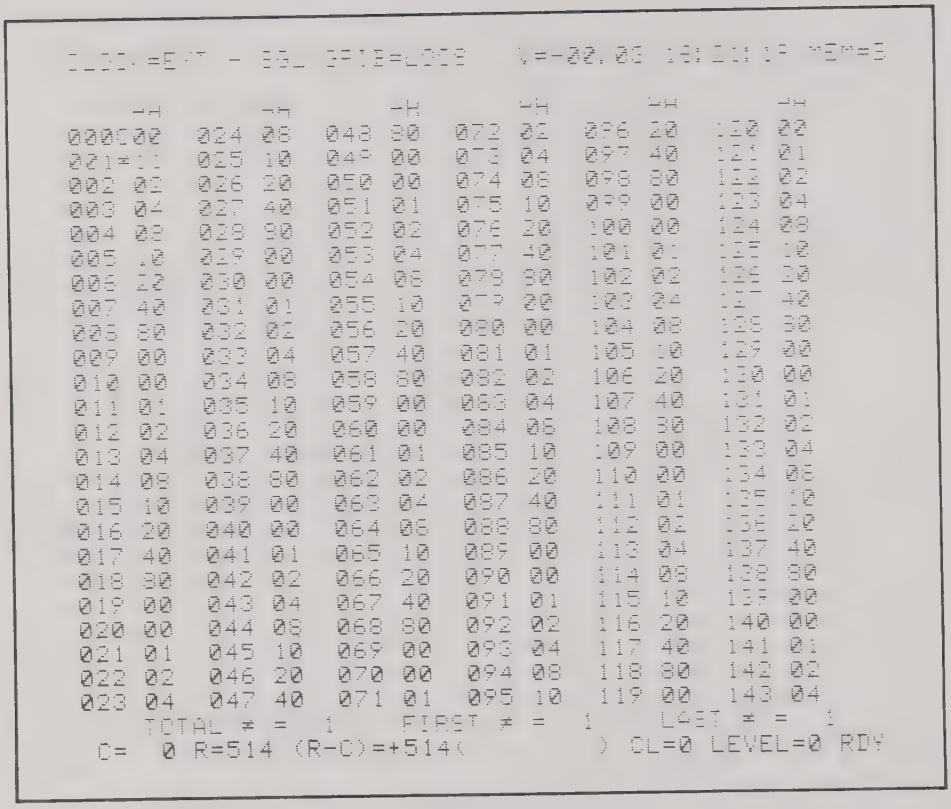


Figure 10-105. Automatic Arming Process Stopped.

REVIEW: Press DATA to see the specific differences.

There may be a few differences (see Figure 10-106) or many (see Figure 10-107). Figure 10-106 shows that even similarly traced asynchronous recordings usually differ due to the one sample uncertainty of plus or minus one. Figure 10-107 shows that similarly traced asynchronous recordings may differ significantly depending on the specified sample rate and trace condition.

Press ARM several times.

10.2.7.5 **Auto Stop if A = B**

SET UP: To check for a specific suspected error, or to check if and when a system will perform as specifically desired, change the arm mode to look for equality.

Press INPUT MODE , △ , Hx6 2 ' .

RECORD: Press ARM .

Watch the count. Because of the asynchronous sampling, each new recording will most likely be different from the stored recording. However, the odds are good that eventually an exact match will occur and therefore halt the process. In Figure 10-108 267 asynchronous recordings were taken and compared before a match occurred.

REVIEW: When rearming stops, press DATA .

Note that the memory contents are identical. In Figure 10-109 every sample of the 267th recording is identical to the previously stored recording.

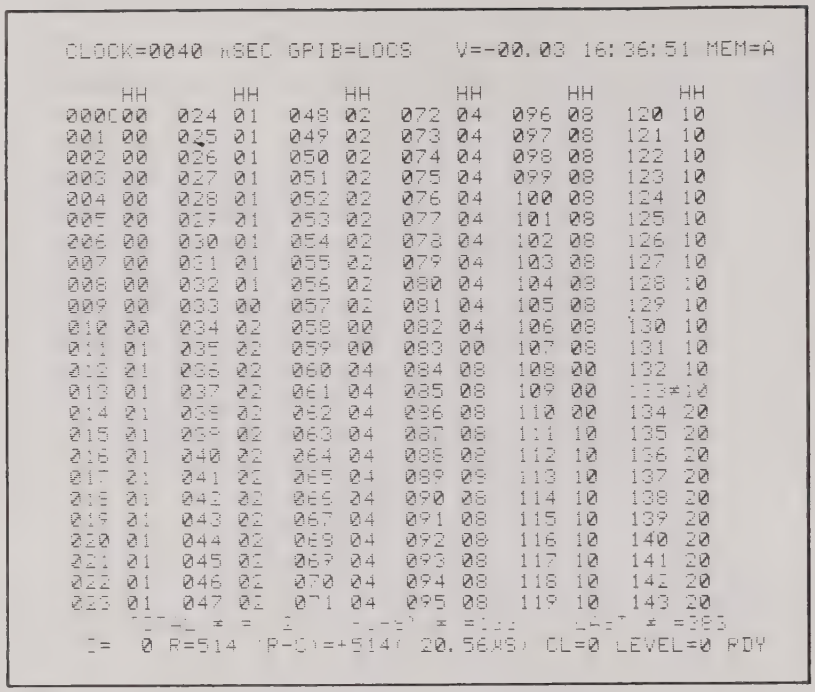


Figure 10-106. Asynchronous Recordings Differences.

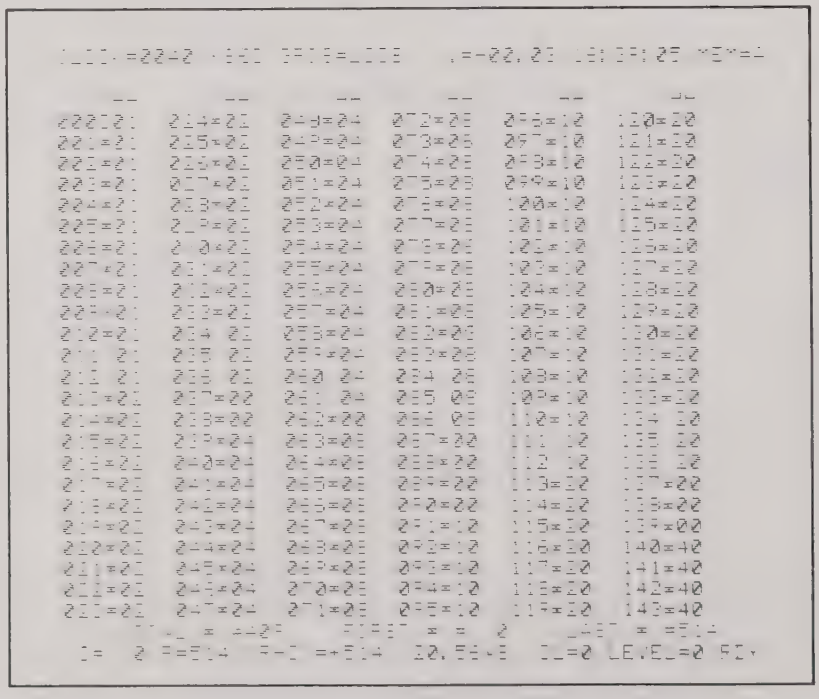


Figure 10-107. Effect of Specified Sample Rate and Trace Condition.

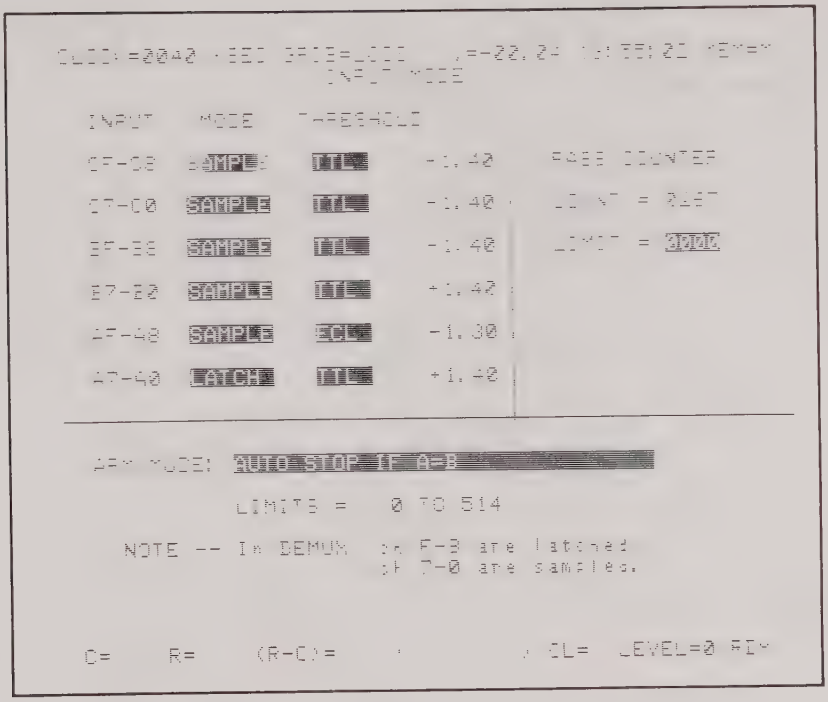

INPUT MODE THRESHOLD
F-08 SAMPLE TTL -1.40
07-00 SAMPLE TTL -1.40
17-10 SAMPLE TTL -1.40
27-20 SAMPLE TTL +1.40
37-30 SAMPLE ECL -1.30
47-40 LATCH TTL +1.40
COMPARE MODE: AUTO STOP IF A=B
LIMITS = 0 TO 514
NOTE -- In DEMUX: or F-B are latched
or 7-0 are samples.
C= R= (R-C)=

Figure 10-108. 267 Recordings Compared Before Match.

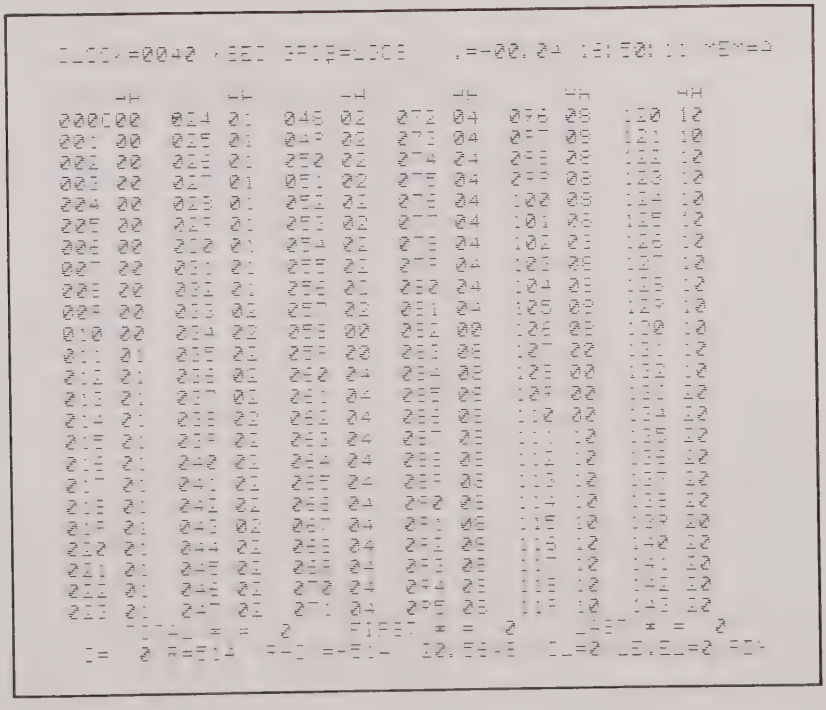


Figure 10-109. Identical Recordings.

10.2.7.6 **Auto Stop if A ≠ B Within Limits**

SET UP: Once the problem area has been narrowed down, it often isn't necessary to compare the entire recording, only portions of it. To do this, change the arm mode.

Press [INPUT MODE] , [△] , [V24 5 L] , then go back to synchronous clocking.

Press [CLOCK SELECT] , [Hx3 1 H] .

RECORD: Press [ARM] , [A→B] , [ARM] to load memory B and initiate the auto arming.

Press [SHIFT] , [◁ SET] , [V24 5 L] , [Hx1 0 G] , twice to set the cursors to frame the area of comparison.

Press [INPUT MODE] to check the cursors' locations (see Figure 10-110).

Press [DATA] , [B] , [▷] , [EDIT] , [DEMUX F HEX V] , [EDIT] .

Rearming does not stop because the inequality is outside the area defined by the cursors (see Figure 10-111).

Press [EDIT] , [▽ SET] twice, [Hx3 1 H] , [EDIT] .

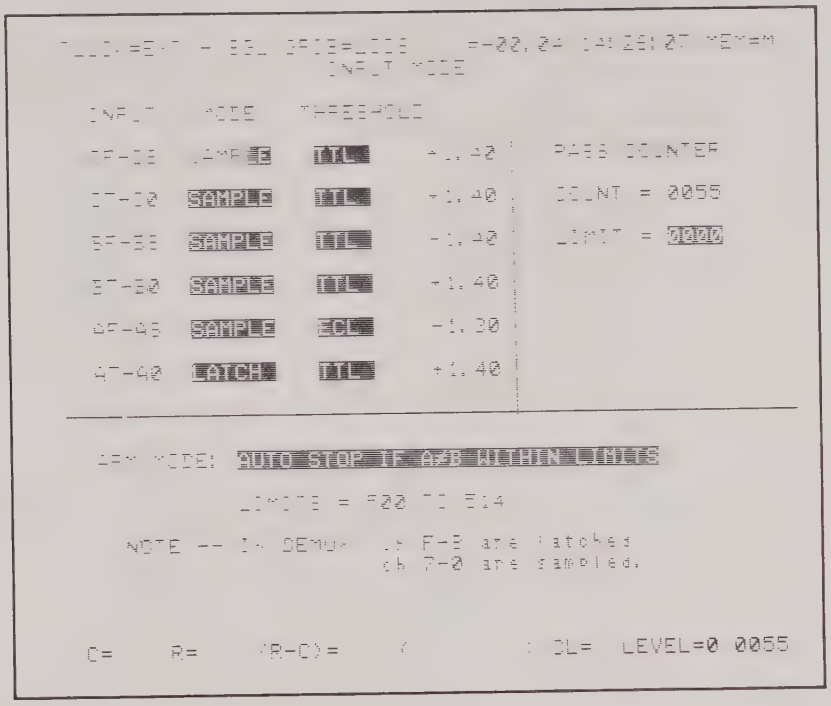


Figure 10-110. Comparison Between Location 500 and 514.

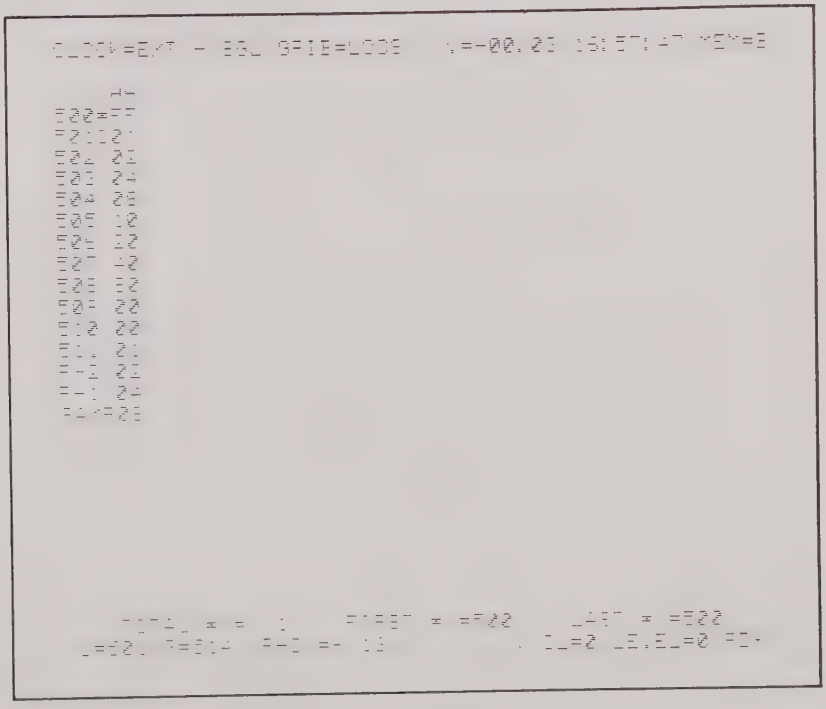


Figure 10-111. Inequality Outside Window.

The auto stop condition is now satisfied as the change is within the cursor limits.

REVIEW: The display should look like Figure 10-112 which shows that an inequality within the limited comparison window stops auto arming.

10.2.7.7 **Auto Stop if A = B Within Limits**

SET UP: A check for equality similarly may be focused on a smaller area of the recording. Change the arm mode.

Press [INPUT MODE], [△], [PAGE 4 K], [DATA], [B].

RECORD: Press [ARM] to start the recording process.

Since the memories were made unequal in the previous exercise, the rearming could continue indefinitely.

Press [EDIT], [▽ SET], [Hx1 0 G], [EDIT].

Recording will stop.

REVIEW: Between the Control Cursor and the Reference Cursor, memories A and B are now identical (see Figure 10-113), which satisfied the auto stop condition. Figure 10-113 shows that arming stops when the samples in the windowed area become the same.

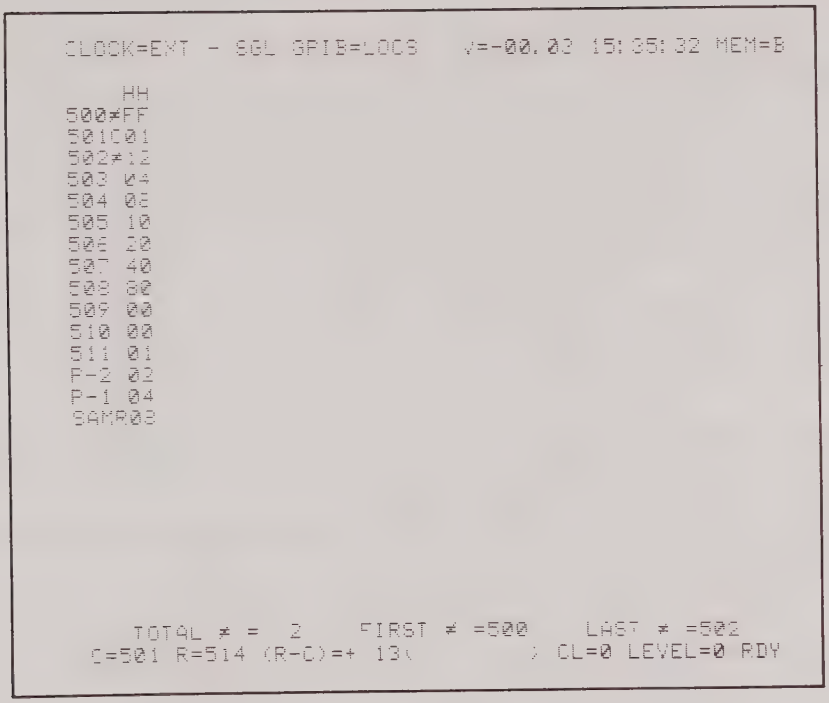


Figure 10-112. Inequality Within Window.

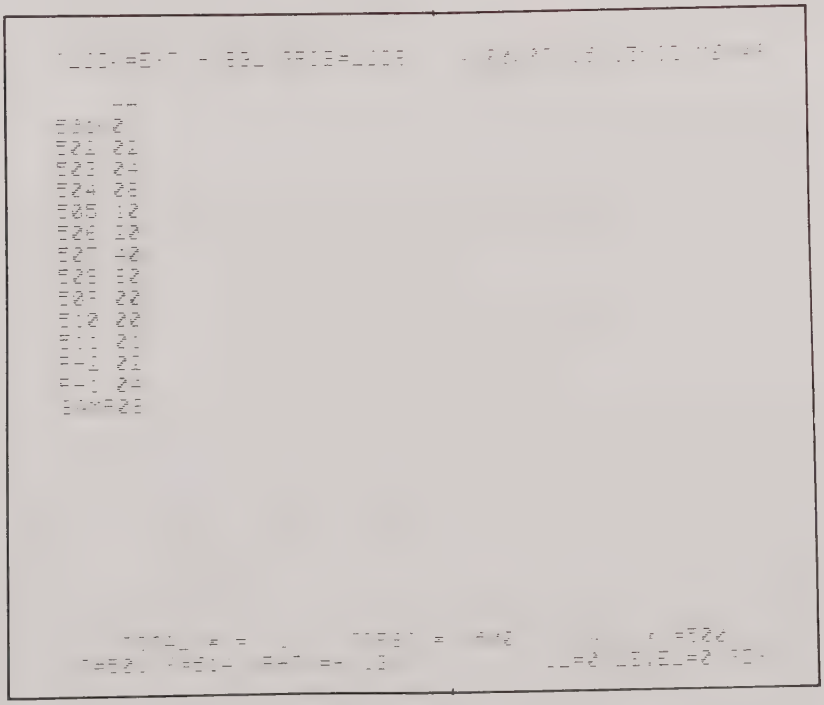


Figure 10-113. Samples in Window Same Arming Stops.

10.3 POWER UP TEST

As soon as the power is turned on, the K101-D will beep and start executing an automatic diagnostic routine of six tests. As each test is completed, the next test is automatically run. When all tests are successfully completed, the analyzer beeps again and displays the Clock Select setup screen.

If an error is detected in any of the tests, the name of the failed test is displayed and further testing halted. To run the rest of the power up tests, or to attempt to operate the instrument despite the error, press **NEXT** to continue. When the last test (successful or not) is completed, the Clock Select setup screen is displayed. At this point, since an error has been detected, you should run the appropriate Self-Test diagnostic routine (see paragraph 10.4, Self Test). Table 10-2 lists the power up error messages and the action you should take to respond to these messages. The following paragraphs briefly describe the six power up tests.

10.3.1 K101-D ROM TEST

A total of 16 EPROMs are individually tested against known check sums. The failure display uses an 8 x 2 grid to indicate the physical location of the bad ROM on the K101-D MPU PC board (see Figure 10-114). Any failure can cause incorrect operation of the unit.

10.3.2 K101-D RAM TEST

A total of sixteen 64K RAMs are tested and any failures are displayed in a grid indicating the faulty RAM location on the K101-D MPU PC board (see Figure 10-115). Any failure can cause incorrect operation of the unit.

Table 10-2. Power Up Test Error Messages

Error Message	Appropriate Response
1. ROM: see Figure 10-114	Advise Gould repair facility
2. RAM: see Figure 10-115	Advise Gould repair facility
3. Power supply: see Figure 10-116	Run indicated Self-Test and advise Gould repair
4. CMOS RAM checks in error	See paragraph 10.3.4. Advise Gould repair facility if error does not clear
5. USART: see Figure 10-117	
6. Stuck key	See paragraph 10.3.6. Advise Gould repair facility as to which key is stuck

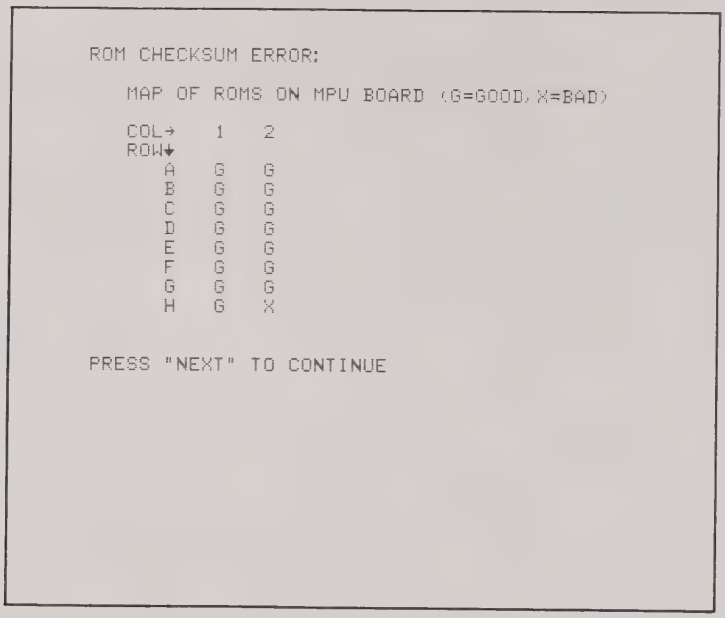


Figure 10-114. ROM Test Grid.

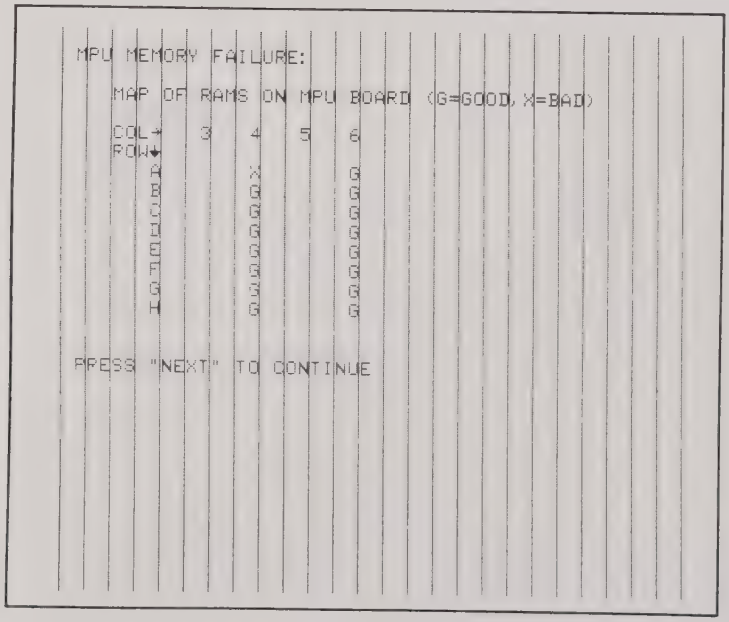


Figure 10-115. RAM Test Grid.

10.3.3 POWER SUPPLY TEST

Each of the power supply's voltage outputs is tested on a pass/fail basis. If any supply is out of tolerance, the testing stops and a message is displayed indicating which power supply failed (see Figure 10-116). Power supply tolerances are discussed in paragraph 10.4. A failure may or may not cause improper operation of the unit, depending on the nature of the failure.

10.3.4 CMOS RAM TEST

The stored data are tested against a check sum also stored in the CMOS RAM. (This is not the same as the CMOS RAM Self-Test.) A failure causes an error message (CMOS RAM CHECKSUM ERROR) to be displayed. An error indicates that the unit will not properly recall the recording setup parameters previously stored, nor correctly save new ones.

The appearance of the error message does not necessarily mean a component has failed. The source could be an intermittent, "soft" error. The following procedure will clear such a soft error:

Press CHOICE NEXT . Wait for Clock Select to be displayed.

Press SHIFT , RECALL , and SAVE .

This loads the default setups from ROM into the CMOS RAM. If the original error was not caused by a component failure, the CMOS RAM CHECKSUM ERROR should not appear on the next power up and the CMOS memory should operate correctly. You can test this by changing any parameter from its default value, pressing **SAVE**, then **RECALL**, and seeing if the changed parameter is still there as it should be.

10.3.5 USART ERRORS

The status of the communication I/O USART is checked for failures. USART failures may cause incorrect operation of the unit. See Figure 10-117 for USART error messages.

10.3.6 KEYBOARD TEST

Each one of the keys on the front panel keyboard is tested for a NOT PRESSED condition. If a pressed key is observed, the unit displays an error message: STUCK KEY. Press one key at a time; keys that are not stuck cause the unit to beep when pressed. Stuck keys must be repaired in order to continue operation of the unit.

10.4 SELF-TEST

Self-Test is selected by pressing **SHIFT**, then **SELF TEST.** The screen will display a menu of the various tests that can be run (see Figure 10-118). To run a specific test, move the cursor up or down (field up or field down) to the desired test then press **NEXT.** Depending on the test, the unit either starts an actual test or displays a more detailed submenu. To run a specific submenu test, again move the cursor to the desired test and press **NEXT.** To exit a submenu and return to the main menu, press **PREV.** To exit Self-Test altogether, press **PREV** while in the main Self-Test menu.

A confidence test generally runs all the specific tests listed beneath it. At the completion of a confidence test, the display says only whether the tests passed or failed; no detailed failure information is given. At the completion of the confidence tests (there is no screen indication showing that a test is being run while it is executing) END OF TEST and test PASSED, or FAILED are displayed. Have patience. Some tests (such as trace control) take several minutes to complete. Also, failures will extend the testing time.

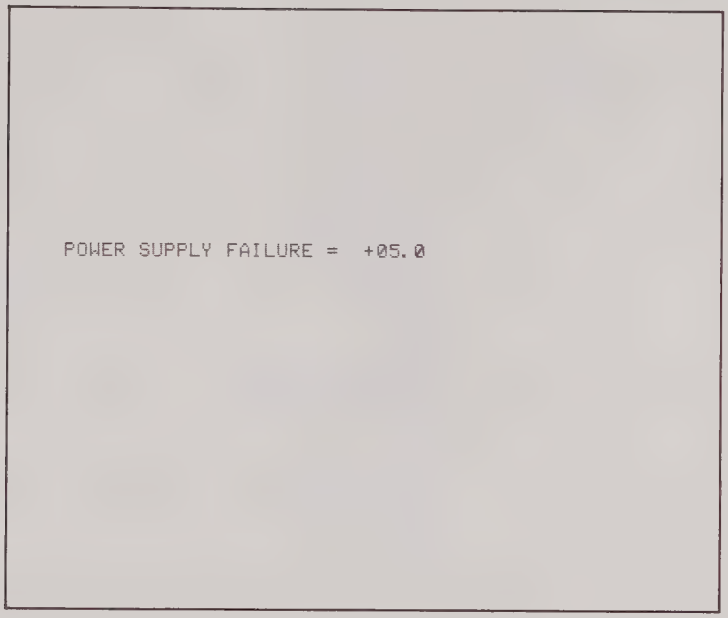


Figure 10-116. Power Supply Error Messages.

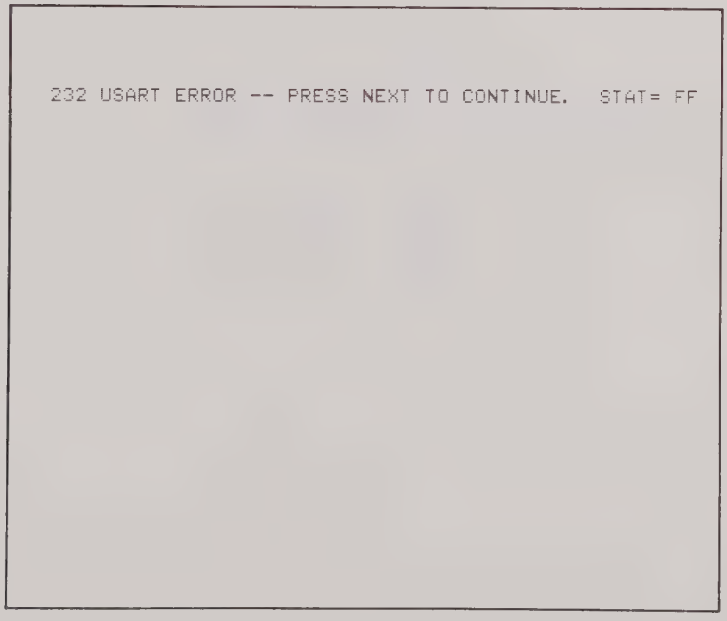


Figure 10-117. USART Error Messages.

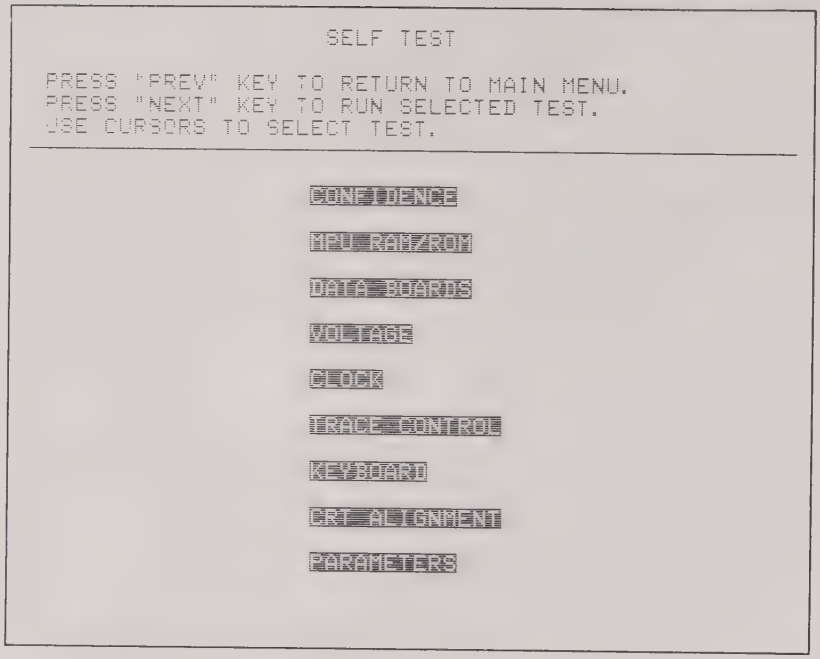


Figure 10-118. Main Menu When First Entering Self-Test.

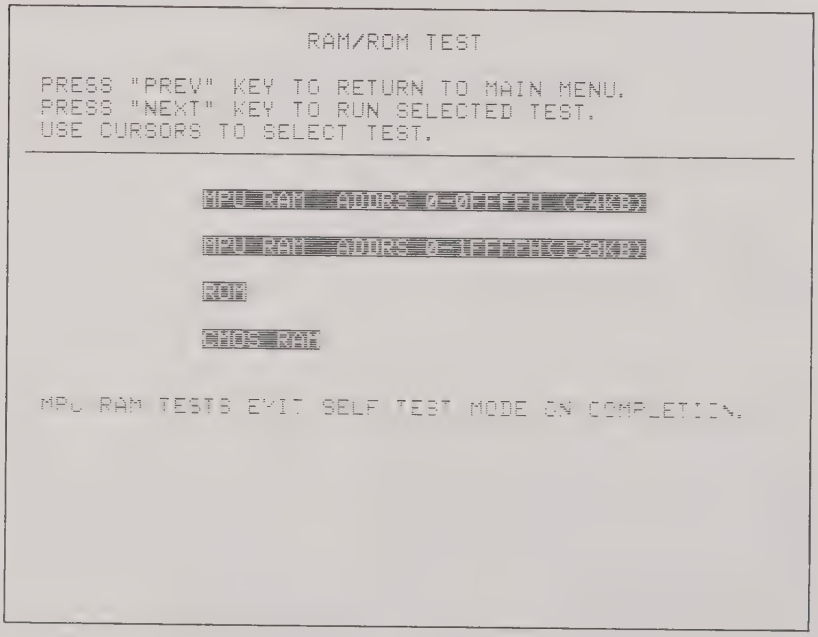

RAM/ROM TEST
PRESS "PREV" KEY TO RETURN TO MAIN MENU.
PRESS "NEXT" KEY TO RUN SELECTED TEST.
USE CURSORS TO SELECT TEST.
MPU RAM ADDRS 0-0FFFFH (64KB)
MPU RAM ADDRS 0-1FFFFH(128KB)
ROM
CHDS RAM
MPU RAM TESTS EXIT SELF TEST MODE ON COMPLETION.

Figure 10-119. MPU RAM/ROM Test Submenu.

Running the specific diagnostic tests individually results in an error summary listing of the type and number of failures as well as specific failure information. The format of this detailed error information is specified in the Parameters screen (discussed later in this section).

10.4.1 CONFIDENCE TEST

Runs all tests in the main menu except for Keyboard, CRT alignment, and Parameters.

10.4.2 K101-D MPU RAM/ROM

When this test is selected, the submenu appears as shown in Figure 10-119.

10.4.2.1 **MPU RAM (64K)**

This test checks the first half of the memory RAM on the MPU board. Failures are displayed on a grid showing faulty RAM locations on the MPU board. This test is also run during power up testing. Failures may or may not affect system operation. Failures can be listed by each bad memory location when using the scroll selection of the Parameter screen. Note that upon completion of this test, Self-Test mode is automatically exited.

10.4.2.2 **MPU RAM (128K)**

This test checks all of memory RAM on the MPU board. It operates identically to the MPU RAM (64K) test.

10.4.2.3 **ROM**

This test verifies the check sum of all 16 EPROMs on the MPU board. Any failures are displayed on a grid, to show the location of the faulty ROM. This test is also run during power up testing.

10.4.2.4 **CMOS RAM**

This test checks the ability of the CMOS RAMs to store new data. Failures are listed as specified by the Parameter screen. A failure indicates the unit will fail the CMOS RAM test (of the power up tests), and that the unit will power up with unwanted recording setups. Refer to paragraph 10.3.4 for instructions to clear CMOS RAM errors.

10.4.3 DATA BOARDS

When this test is selected, the submenu shown in Figure 10-120 is displayed.

10.4.3.1 **Confidence**

This test runs all three data board tests.

10.4.3.2 **Data Board A**

When this test is selected, the submenu shown in Figure 10-121 is displayed.

10.4.3.3 **Confidence Test**

Runs all of the tests on the specific data board.

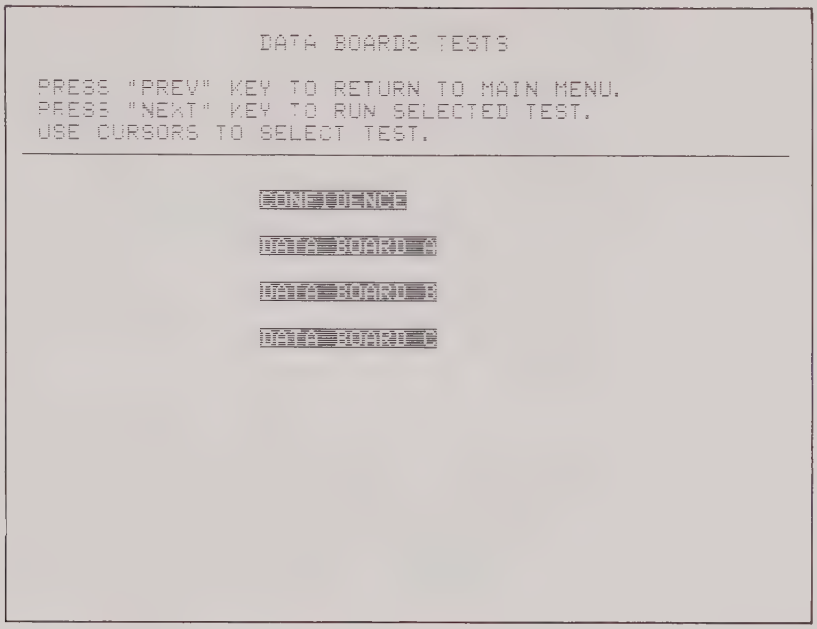
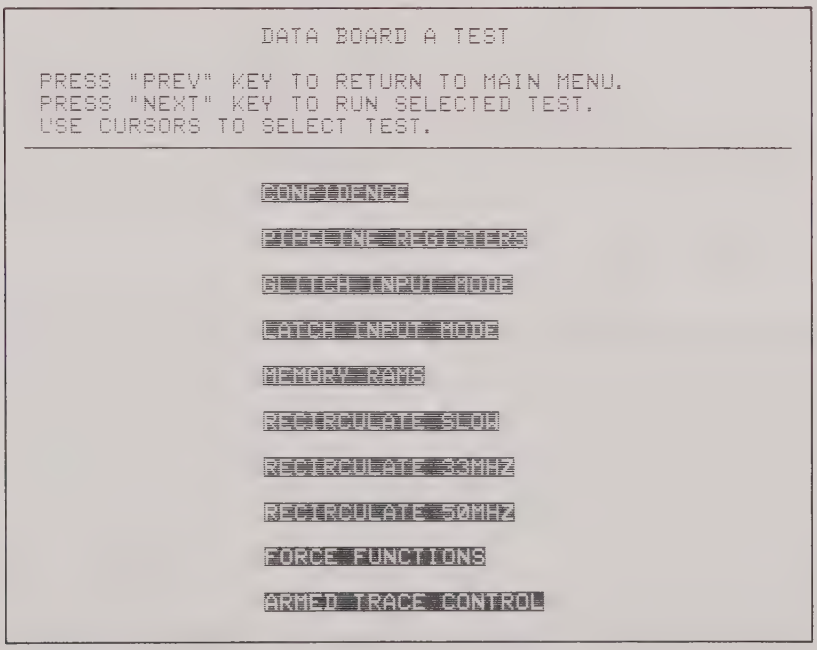

DATA BOARDS TESTS
PRESS "PREV" KEY TO RETURN TO MAIN MENU.
PRESS "NEXT" KEY TO RUN SELECTED TEST.
USE CURSORS TO SELECT TEST.
CONFIDENCE
DATA BOARD A
DATA BOARD B
DATA BOARD C

Figure 10-120. Data Board Tests Submenus.



Note: The Menus for boards B and C are identical.

Figure 10-121. Data Board A Submenu.

10.4.3.4 **Pipeline Registers**

This test checks the pipeline register circuitry on the data board. A failure indicates which of that section's 16 inputs will not record properly. Failures are displayed to show the data expected and data actually recorded in hex words.

10.4.3.5 **Glitch Input Mode**

This test checks the ability of all the inputs to detect glitches while in the glitch mode. Failures are displayed to show hex data words that indicate which inputs are not detecting properly. If this is the only test that failed, the only operation that should be affected is that of glitch capture.

10.4.3.6 **Latch Input Mode**

All of the latch inputs are tested for proper operation. For failures, readings similar to those for other data board tests are displayed. Typically, if the unit fails this test, an input is not sampled.

10.4.3.7 **Memory RAMs**

This test checks the ability of the high-speed memory RAMs to store information. Note that if there are failures in the previous data board test, the memory RAMs appear to be bad but may not be. Failures are displayed in hex as in previous tests. Typically, if the memory RAMs fail, recorded information is incorrect.

10.4.3.8 **Recirculate Slow**

This is a slow-speed test of the capability of the data board to feed information out of the memory RAM and then back into RAM. A failure in

this process may not be apparent when making a normal recording unless certain functions are performed with the logic analyzer. Failures are displayed in hex.

10.4.3.9 **Recirculate 33 MHz**

This is the same test as Recirculate Slow, except the test runs at 33 MHz.

10.4.3.10 **Recirculate 50 MHz**

This is the same test as Recirculate Slow, except the test runs at 50 MHz.

10.4.3.11 **Force Functions**

This test checks the recording control of the data board. If failures are observed, more than one channel may be inoperative. (Test mnemonics require a technical description from the factory.)

10.4.3.12 **Armed Trace Control**

This test checks trace control functions within the data board for errors. (Error descriptions require further technical information from the factory.) Failures may or may not cause improper operation of the unit, depending upon the failure and nature of the trace control functions being performed.

10.4.3.13 **Confidence**

This test runs all tests except for DVM and Calibrate. Note that the probes must be connected before running this test.

10.4.3.14 **ADC Calibration**

This test checks the voltage measurement circuits by measuring the +10.00 V reference. An error here may indicate the DVM circuitry is faulty or out of calibration. A DVM fault can cause incorrect failures to be displayed on any voltage test. Another cause could be the +10.00 V reference being out of tolerance. Refer to paragraph 10.4.3.22 for information on the reference supply.

10.4.3.15 **Power Supply Test**

This test checks that each power supply is within set tolerances. Refer to paragraph 10.4.3.21 for power supply tolerances. Each failed power supply is displayed. The tested power supplies are the +15, -15, -10, -5.2, and -2 V battery and the +10 V reference supply.

10.4.3.16 **Threshold Source**

There are four different threshold selections available. The circuitry that generates the four voltages (TTL, ECL, VAR A, VAR B) is tested for accuracy. Any failures displayed indicate that the threshold voltage is not accurate on any probes that are trying to use that threshold.

10.4.3.17 **Threshold Selection**

This test verifies that each probe can be operated on TTL, ECL, VAR A, or VAR B. A failure is displayed if any threshold selector does not put out the correct voltage. This test may fail if there was a failure in the Threshold Source test.

10.4.3.18 **Probe Loading**

This test verifies the accuracy of the load the input probe has on the threshold voltage. If there is no connection to a probe, the voltage measures too high and is indicated as a failure. Also, if the probe is bad, it may short the voltage such that it measures too low, and so indicates a failure. The probes must be connected to run this test.

10.4.3.19 **Variable A/B**

This test checks the linearity of the variable threshold voltages. This test measures linearity at the output going to the input probe. A failure indicates the variable voltages are bad or out of tolerance. Recordings are not affected, unless the threshold that failed is selected. The probes must be connected before running this test.

10.4.3.20 **DVM**

This test requires the installation of DVM cables to the input probe connector. Without jumpers, this test will fail. Install a jumper from the +DVM input to pin 14 of the A8 section input probe connector (lower right hand pin). Install a jumper from the -DVM (ground) to pin 14 of the A0 section input probe connector. The jumpers connect the threshold voltages to the DVM inputs. The external DVM circuitry is tested for accuracy and linearity. If there are threshold failures, the DVM test may fail. Specific voltage measurement failures are displayed.

10.4.3.21 **Calibrate**

This test displays the voltages actually measured and the acceptable tolerances. The display is continually updated every few seconds. Power supply voltages can be adjusted by monitoring this display, but it is recommended that you adjust power supplies by the calibration

procedure. The display that is observed while in the Calibrate mode is shown in Figure 10-122.

The following is a list of the various power supply voltages and the associated circuitry to which they provide power:

a. ±15 V -- Display and threshold circuitry
b. ±10 V -- Threshold voltage generation circuitry
c. -5.2 V -- ECL circuitry within the unit
d. +5 V -- TTL circuitry within the unit
e. -2 V -- Many ECL pull-down resistors
f. Battery -- CMOS RAMs

10.4.4 VOLTAGE TEST

When this test is selected, the submenu shown in Figure 10-123 is displayed.

10.4.5 CLOCK

When this test is selected, the submenu shown in Figure 10-124 is displayed.

10.4.5.1 **Confidence**

This test runs both the Clock Frequency and the Level Memory tests.

10.4.5.2 **Clock Frequency**

This test checks the various internal clock frequencies on which the unit operates. The multiplier frequencies and actual measurements are displayed if a failure is noted.

CALIBRATE

SUPPLY NOMINAL	ACCEPTABLE MINIMUM	ACCEPTABLE MAXIMUM	MEASURED AVERAGE	MEASURED P-P
+15.00 V	+14.40	+15.60	+15.02	+0.03
-15.00 V	-15.60	-14.40	-15.03	+0.05
-10.00 V	-10.10	-9.90	-9.99	+0.00
+5.04 V	+4.84	+5.24	+5.02	+0.01
-5.28 V	-5.48	-5.08	-5.20	+0.09
-2.08 V	-2.16	-2.00	-2.09	+0.04
V BATT	+2.34	+4.00	+3.06	+0.00
GND REF	-0.02	+0.02	-0.00	+0.00
+10V REF	+9.96	+10.04	+10.00	+0.00

USE "PREV" TO RETURN TO MENU

Figure 10-122. Typical Calibrate Display.

VOLTAGE TESTS

PRESS "PREV" KEY TO RETURN TO MAIN MENU.
PRESS "NEXT" KEY TO RUN SELECTED TEST.
USE CURSORS TO SELECT TEST.

CONFIDENCE
ADC CALIBRATION
POWER SUPPLY
THRESHOLD SOURCE
THRESHOLD SELECTOR
PROBE LOADING
VAR A/B
DVM
CALIBRATE

PROBES MUST BE INSTALLED FOR CONFIDENCE TEST AND
FOR PROBE LOADING AND VAR A/B TESTS.
DVM TEST FIXTURE IS REQUIRED FOR DVM TEST.

Figure 10-123. Voltage Test Submenu.

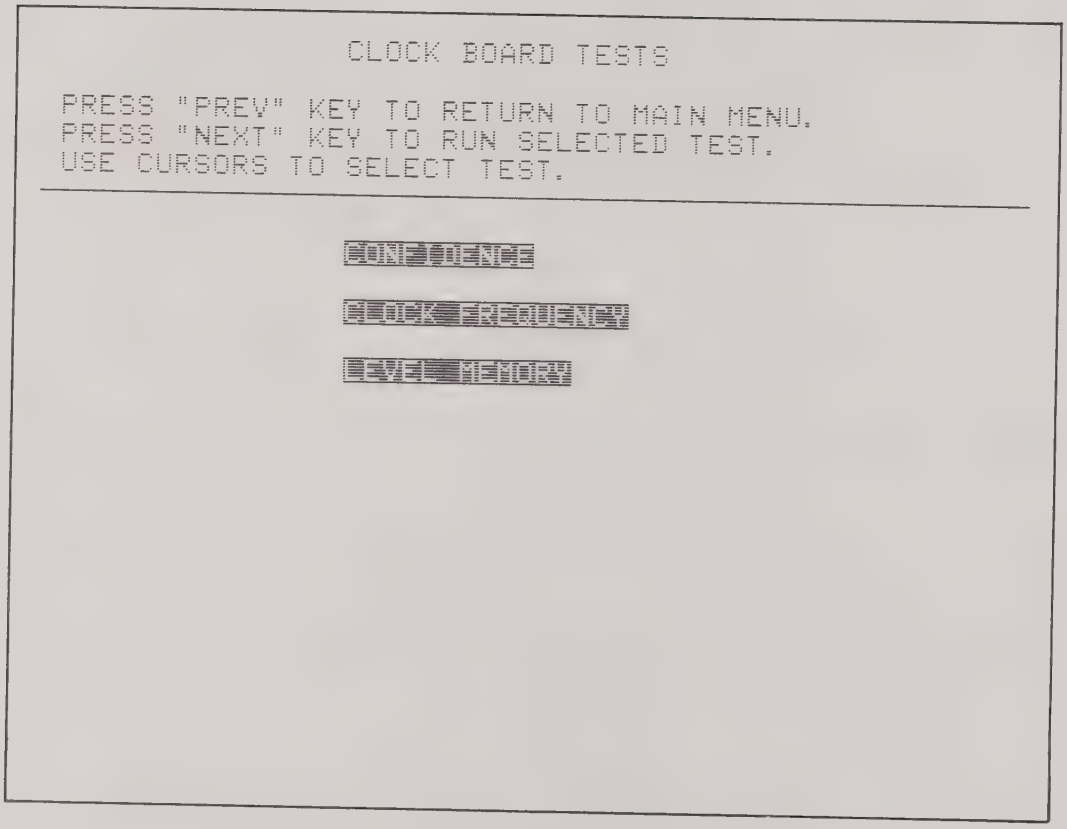


Figure 10-124. Clock Test Submenu.

10.4.5.3 **Level Memory**

This test checks the ability of the level memory RAMs to store the level at which trace control samples were recorded. Failures are displayed by memory location. A failure here indicates the memory will not be accurate.

10.4.6 TRACE CONTROL

When this test is selected, the submenu shown in Figure 10-125 is displayed.

10.4.6.1 **Trace Confidence**

This test runs all of the tests in the menu.

10.4.6.2 **Force Conditions**

This test checks the ability of the unit to perform basic trace control functions. A failure indicates the unit may not perform trace control functions, depending upon the failure.

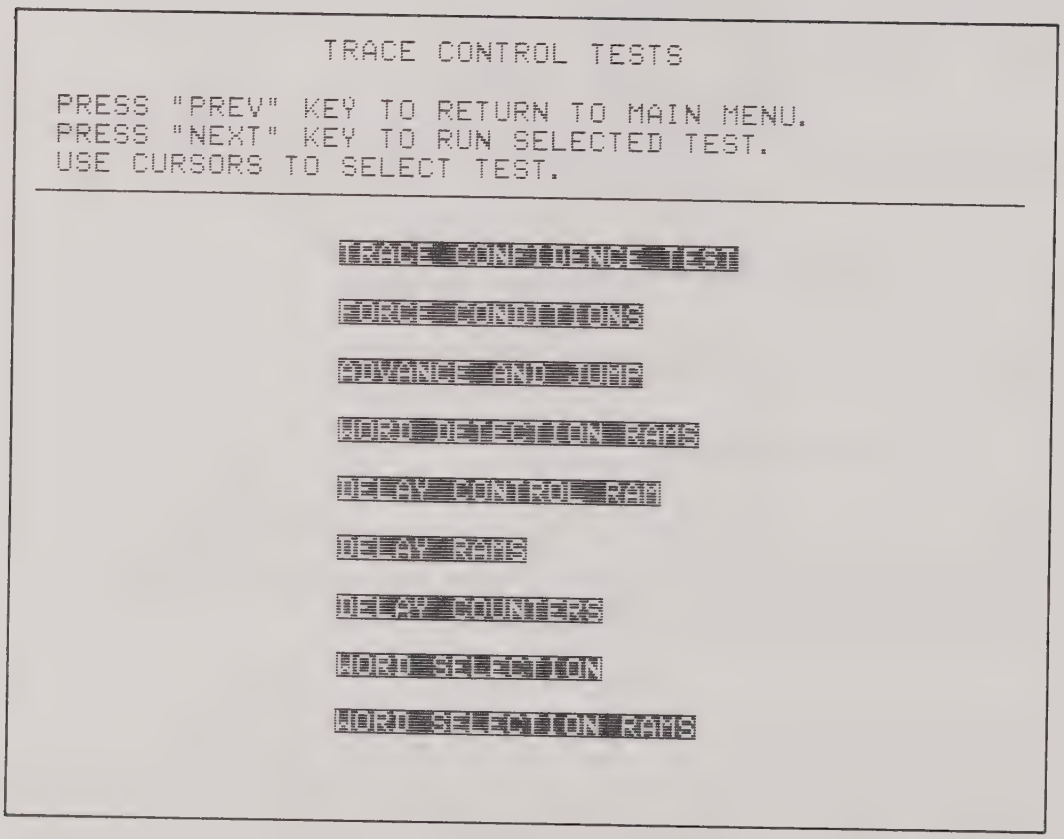


Figure 10-125. Trace Control Test Submenu.

10.4.6.3 **Advance and Jump**

This test checks the ability of the unit to ADVANCE and JUMP to the various levels of trace control. A failure indicates the unit may not record properly, depending upon the failure and the functions the logic analyzer is trying to perform.

10.4.6.4 **Word Detection RAMs**

This test checks the RAMs' capability to store data that control the word detection circuitry. A failure indicates the unit may not recognize the S, J, A, and T word recognizers used in the trace control commands. This test takes several minutes to run.

10.4.6.5 **Delay Control RAM**

This test checks the RAMs' capability to store data that control the delay control circuitry. A failure indicates the unit will not perform delay functions, depending on the failure.

10.4.6.6 **Delay RAMs**

This test checks the ability of the RAMs to store data that control the amount of delay in tracing functions. A failure indicates the unit may not delay by the proper amount of clocks or events, depending on the failure.

10.4.6.7 **Delay Counters**

This test checks the ability of the unit to count the correct number of clocks or events. A failure indicates the unit may not delay by the proper amount when tracing, depending upon the failure.

10.4.6.8 **Word Selection**

This test checks the ability of the unit to recognize each S, J, A, and T word. A failure indicates the word selection circuitry may not tell the word detection RAMs when a condition is satisfied.

10.4.6.9 **Word Selection RAMs**

This test checks the ability of the RAMs to store data that control the word selection circuitry. A failure indicates the unit may not recognize S, J, A, and T words in the trace control commands.

10.4.7 KEYBOARD

When this test is selected, the keyboard test routine is automatically entered and a display appears as in Figure 10-126. The unit is prompting you to press **DATA**. After you press **DATA**, the display changes and prompts you to press **GRAPH**. To complete the test (and exit the test routine) you must press each key in the proper sequence as prompted by the display (by columms, left to right, going up from bottom row to top row). A BAD KEY error message appears if a key is pressed out of sequence or if the key immediately preceeding the one just pressed is actually bad. (In other words, an actual bad key is not indicated until the next key is pressed.) All 56 keys must be pressed before you can exit the test: there is no way to abort the test.

10.4.8 CRT ALIGNMENT

CRT alignment simply provides a test grid on the CRT in order to adjust it for proper visual linearity (see Figure 10-127).

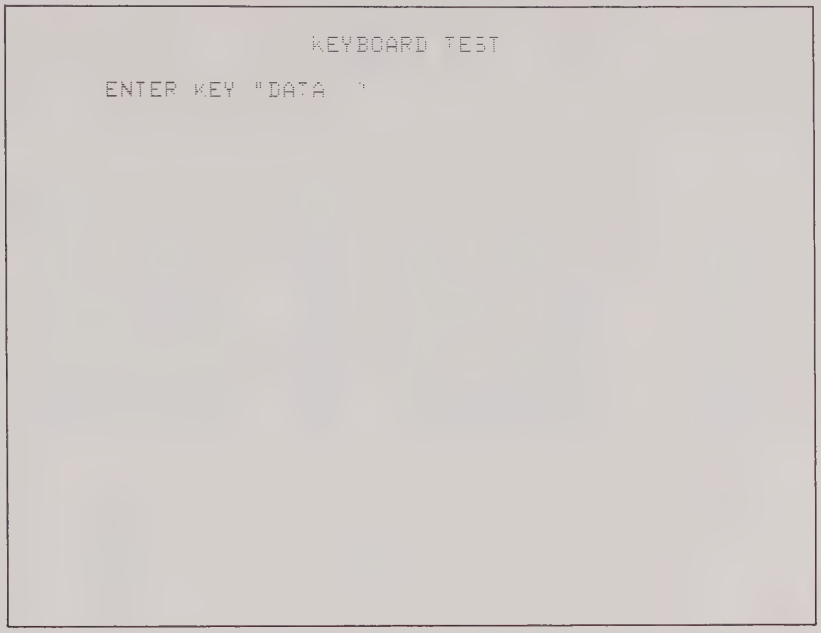


Figure 10-126. First Keyboard Test Display.

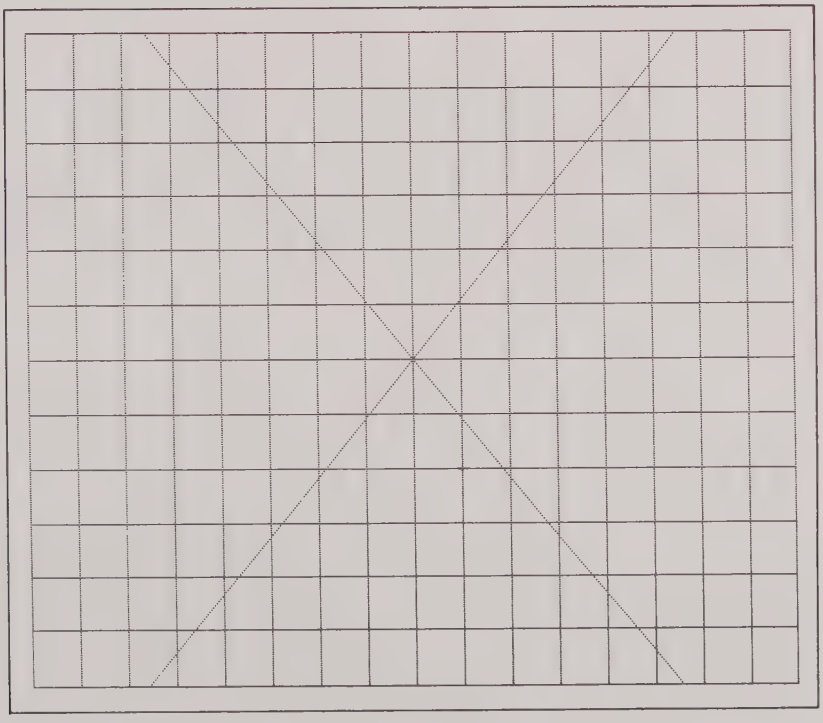


Figure 10-127. Alignment Test Grid.

10.4.9 PARAMETERS

The submenu that is shown when parameters is selected is shown in Figure 10-128. Parameters enhances all of the Self-Test diagnostics. The lower section of the display provides a cumulative total of errors detected during the Self-Test diagnostics. (The totals are reset to zero upon entering Self-Test.) The first field allows you to choose three types of error display modes, which are selectable by the **NEXT** key. The selections are as follows:

a. **Page.** If a failure occurs in a chosen diagnostic test, the unit displays one page (display) of errors only.

b. **Scroll.** If a failure occurs, the display scrolls through the entire list of errors.

c. **No Print.** No errors are displayed even if a failure occurs.

LOOP ON TEST may be selected as YES or NO. If YES is selected the unit continuously performs one Self-Test after another. Once it is looping, the only way to exit Self-Test is to turn off the unit. This allows the instrument to be checked for correct performance over extended use. NO stops after one Self-Test cycle.

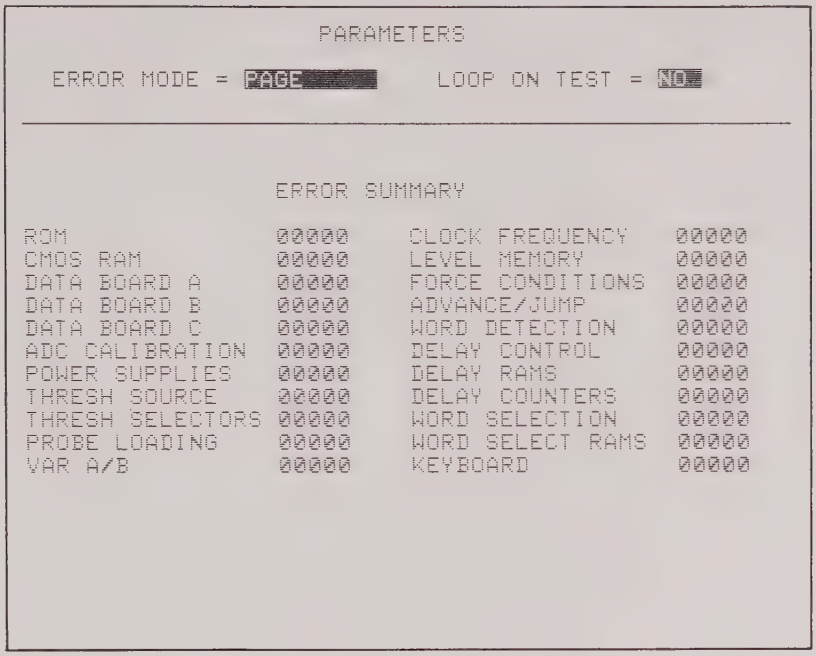


Figure 10-128. Parameters Display Screen.

Section 13

GLOSSARY

This glossary contains terms in general use in the disciplines of hardware and software development and use, and terms specific to the use of the K101-D. The general terms are provided because many users of the K101-D will have experience in either hardware or software, but not both.

The K101-D terms given in this glossary are identified with an asterisk (*) preceding the entry. They are defined for one or more of the following reasons:

a. For special meaning. A term in general use may have a special meaning when used in this manual. For example, "alignment" refers to displaying data events.

b. For convenience, so that terms are available in one location for easy reference.

c. For comparison. Some terms become clearer when compared with others. Although either "trace" or "recording" would be understood in context when reading the manual, comparing the two entries helps in understanding the concepts underlying the functions of the logic analyzer.

Glossary entries are listed below in alphabetic order. Table 13-1 shows the logical relationships of many K101-D specific glossary entries. By looking up groups of entries related in the figure, and reading those associated entries, you can get a quick overview of concepts useful for understanding the logic analyzer.

Table 13-1. Logical Relationships of Selected K101-D Terms

Probe Connection
- Input Signals
  - Input Data
  - Clock Signals

Specification
- Threshold
- Logic Polarity
- Input Modes
  - Sample Mode
  - Glitch Mode
  - Latch Mode
  - Demux Mode
- Data Format
- Clocking Modes
- Trace Control
  - Advance
  - Jump
  - Stop
  - Trace

Recording
- Recording Cycle
- Recording Process
- Arm Mode

Recording Analysis
- Data Display
- Graph Display
- Timing Display

ACCURACY

The degree of freedom from error, that is, the degree of conformity to truth or to a rule. Accuracy is contrasted with precision. For example, four-place numerals are less precise than six-place numerals; nevertheless a properly computed four-place numeral might be more accurate than an improperly computed six-place numeral.

ADDRESS

A group of bits that identify a specific memory location or I/O device. An 8080 microcomputer uses 16 bits to identify a specific memory location and 8 bits to identify an I/O device.

ADDRESS BUS

A unidirectional bus over which digital information appear for identification of either a particular memory location or a particular I/O device. The 8080 address bus is a group of 16 lines. See also **Bus, Control Bus.**

* **ADVANCE**

One of four Trace Control commands. It advances you to the next level of trace control, for example, from level three to level four.

* **ALIGNMENT**

This term has a special meaning when referring to trace recording. Alignment refers to the process of grouping related events into a single record item for later display, although those events happened at different times. See **Latch Mode** and **Demultiplex.**

ALPHANUMERIC

A character set comprised of both letters and digits.

ALPHANUMERIC CODE

A code whose set consists of letters, digits, and associated special characters.

ANALOG

Data in the form of continuously variable physical quantities, such as voltage. Compare to **Digital.**

ANALYZER (GENERAL)

Evaluates and/or measures one or more specific parameters (e.g., voltage, current, frequency, logic level, bit time, distortion, etc.).

ANALYZER, LOGIC

See logic analyzer.

* **AND**

1. An operation in Boolean algebra. When two or more terms are ANDed together (combined using the AND operation), the result is true if and only if all terms are true.

* 2. One of the two operations used in specifying clocking modes. The other, also defined, is **OR.**

AND GATE

A binary circuit with two or more inputs and a single output, in which the output is logic 1 only when all inputs are logic 1, and the output is logic 0 if any one of the inputs is logic 0.

* **ARM**

The act of initializing a recording cycle in a logic analyzer. See also **Arm Mode.**

*** ARM MODE**

The K101-D has two basic arm modes, manual and automatic. Arm modes control the recording process. In manual mode, the recording process stops after one complete cycle of tracing based on the set of trace control instructions and the conditions in the system under test at the time of recording. (This cycle is called a recording cycle.) In the automatic modes, recording cycles may be repeated under the control of user-specified conditions.

*** ASCII**

1. American Standard Code for Information Interchange. A national standard, ASCII is seven-bit code, now usually seen in eight-bit form (the eighth bit can be forced to 1 or 0, or can be a parity bit), specifying letters, numbers, and certain control functions. See **Code** and **EBCDIC.**

* 2. One of the K101-D data formats. It decodes seven bits.

ASSEMBLER

A program that translates symbolic operation codes into machine language and symbolic addresses to memory addresses. Assigns values to all program symbols and translates source programs to object programs.

ASSEMBLY LANGUAGE

A collection of symbolic labels, mnemonics, and data which are translated into binary machine codes by the assembler.

ASYNCHRONOUS

Not occurring at the same time or not bearing a fixed relationship in time. Not synchronous.

ASYNCHRONOUS DEVICE

A device in which the operation is not related to any in the system to which it is connected.

*** ASYNCHRONOUS RECORDING**

A recording in which the data are sampled by a clock that is not synchronized to the data, for example, as when using a logic analyzer's internal clock. See also **synchronous recording.**

*** AUTOMATIC ARMING**

See **Arm Mode.**

BASE

Also called the radix. The total number of distinct symbols used in a numbering system. For example, since the decimal numbering system uses ten symbols, the radix is 10. In the octal numbering system, the radix is 8. In the binary numbering system, the radix is 2 because there are only two symbols (0 and 1).

*** BINARY**

1. The base 2 number system. All numbers are expressed as powers of 2. As a consequence, only two symbols (0 and 1) are required.

* 2. One of the K101-D data formats.

BINARY CODE

A code in which each code element is one of two distinct states, usually symbolized as 0 and 1. See also **logic polarity.**

BINARY COUNTER

An interconnection of flip-flops having a single input and so arranged to permit binary counting. Each time a pulse appears at the input, the counter changes state and tabulates the number of input pulses for readout in binary form. It has 2^n possible counts, where n is the number of flip-flops or stages.

BIT

The smallest unit of information which can be represented. A bit may be in one of two states, represented by the binary digits 0 and 1.

BLOCK DIAGRAM

A simplified functional diagram of a system or assembly.

BOOLEAN ALGEBRA

A system of mathematical logic dealing with classes, propositions, on-off circuit elements, and so on, associated by operators such as AND, OR, NOT, XOR, . . . etc., thereby permitting computations and demonstration, as in any mathematical system. Named after George Boole, English mathematician and logician, who introduced it in 1847.

*** BOOLEAN EXPRESSIONS**

Used to define combinations of external clocks or latch enables for describing sample events evaluated by K101-D.

BOOLEAN SYMBOL

A symbol used to represent a specific Boolean operation.

BRANCH INSTRUCTION

An instruction that causes a program to jump to a specified address and execute the instruction at that address, may be conditional or unconditional. During the execution of the branch instruction, the central processor replaces the contents of the program counter with the specified address.

BRANCHING, CONDITIONAL

A method of selecting, on the basis of results, the next operation for a computer program to execute.

BREAKPOINT

Pertains to a type of instruction, instruction digit, or other condition used to interrupt or stop a computer at a particular place in a program. Allows outside examination of the system state at that point. A place in a program where such an interruption occurs or can be made to occur.

BUS

A path over which digital information is transferred, from any of several sources to any of several destinations. Only one transfer of information can take place at any one time. While such transfer of information is taking place, all other sources that are tied to the bus must be disabled. See also **Address Bus, Control Bus.**

BYTE

A sequence of adjacent binary digits operated on as a unit and usually eight bits long.

CALL OR SUBROUTINE

A special type of jump in which the central processor is required to "remember" the contents of the program counter at the time that the jump occurs. This allows the processor to later resume execution of the main program, when it is finished with the last instruction of the subroutine.

CHANNEL

1. A path along which signals can be sent, e.g., data channel, output channel.

2. The portion of a storage medium that is accessible to a given reading or writing station, e.g., track, band.

CHARACTER

A letter, digit, or other symbol that is used as part of the organization, control, or representation of data.

CHARACTER CODE

See **Code**.

*** CHOICE KEYS**

Provide review and selection of all available choices for each parameter field.

CIRCUIT

A conductor or system of conductors through which an electric current can flow.

CLOCK

A pulse generator that controls the timing of clocked logic devices and regulates the speed at which such devices operate. It serves to synchronize all operations in a digital system.

*** CLOCK INPUT**

1. That terminal on a flip-flop whose condition or change of condition controls the admission of data into a flip-flop through the synchronous inputs, and thereby controls the output state of the flip-flop. The clock signals performs two functions: (1) permit data signals to enter the flip-flop and (2) after entry, direct the flip-flop to change state accordingly.

* 2. Where an external clock signal enters the K101-D.

CLOCK PULSE

A complete logic cycle from logic 0 to logic 1 and back to logic 0 (positive clock pulse), or from logic 1 to logic 0 and back to logic 1 (negative clock pulse).

*** CLOCK SIGNALS**

The 12 input signals (probes) that carry clocking information. See **Input Signals.**

*** CLOCKING MODES**

Specification of the clocking source or sources to be used by the K101-D for sampling data and for clocking it into memory. There are six clocking modes, based on the ability to specify Sample clocks, or Master clocks, or both, as having an internal clock source, external clock source, or mixed internal and external clock source. The setup menu for clocking allows the specification of clock source combinations using Boolean algebra.

CODE (1)

1. A set of unambiguous rules specifying the way in which data may be represented, e.g., the set of correspondences in the standard code for information interchange. Synonymous with coding scheme.

2. In telecommunications, a system of rules and conventions according to which the signals representing data can be formed, transmitted, received, and processed.

3. In data processing, to represent data or a computer program in a symbolic form that can be accepted by a data processor.

*** CODE (2)**

In this manual, refers to a standard for information interchange, such as ASCII or EBCDIC. In these codes, letters, numbers, special characters, and certain control functions have a standard bit-pattern form. The Data Display mode of the K101-D can decode those ASCII and EBCDIC patterns that can be displayed.

CODE CONVERSION

The changing of the bit grouping for a character in one code into the corresponding bit grouping in another code.

COMMUNICATION

The act of imparting, conveying, or exchanging ideas, knowledge, information, etc., whether by speech, writing, or signals.

*** COMPREHENSIVE SAMPLE**

Refers to the ability of the K101-D to make one sample word contain events that happened at different times. This allows, for example, a single sample to contain several events (up to six) for simultaneous trace evaluation even though the events are valid at different times. A specific example would be monitoring system activity at the machine cycle level so that each sample includes all address, data, status, and flag signals in their valid states for that machine cycle. For further information, see **Latch Mode** and **Demux Mode.**

COMPUTER WORD

A sequence of bits or characters treated as a unit and capable of being stored in one computer location.

CONDITIONAL

Subject to the result of a comparison made during computation.

CONDITIONAL JUMP

Also called conditional transfer of control. An instruction to a computer to use the proper one of two (or more) addresses in obtaining the next instruction, depending on some property of one or more numerical expressions or other conditions.

CONNECTOR

A coupling device employed to connect conductors of one circuit with those of another circuit.

CONTROL

Those parts of a computer which carry out instructions in proper sequence, interpret instructions, and apply proper signals.

CONTROL BUS

A set of signals that regulate the operation of the microcomputer system, including I/O devices and memory. They function much like "traffic" signals or commands. They may also originate in the I/O devices, generally to transfer signals to or receive signals from the CPU. See also **Bus, Addrss Bus.**

CPU

Central Processing Unit. The computer module that fetches, decodes, and executes instructions, consisting of a control unit, an arithmetic and logic unit, and related facilities such as registers and clocks.

CYCLE

1. A time interval in which one set of events or phenomena is completed.

2. Any set of operations that is repeated regularly in the same sequence. The operations may be subject to variations on each repetition.

DATA

1. A representation of facts, concepts, or instructions in a formalized manner suitable for communication, interpretation, or processing by humans or mechanical devices.

2. Any representations such as characters or analog quantities to which meaning is or might be assigned.

3. Information.

DATA BUS

A multiline, parallel path over which digital data are transferred from any of several destinations. Only one transfer of information can take place at any one time. While such transfer is taking place, all other sources that are tied to the bus must be disabled.

*** DATA DISPLAY**

One of three display modes for the K101-D, it displays the recorded information in the form specified by the Data Format. It gives exact information about the state of events in the system under test as specified by the conditions for each trace recording, and is sometimes called the state display. Functions are available for searching this display for particular patterns and comparing the current display and a reference display. The other display modes, also defined, are **Graph Display** and **Timing Display.**

DATA DOMAIN

See **Data Display.**

*** DATA FORMAT**

Specification interpreting input data. Individual inputs are recorded as 1 or 0. They can be displayed as binary numbers or grouped and displayed as octal numbers, hexadecimal numbers, ASCII codes, or EBCDIC codes. The data format specification controls the data display and the possibilities available for trace control and for search patterns. The data format is independent of actual data capture. Not all data inputs need to be specified in the format; inputs can be captured even if not specified. The data format can be changed after data capture.

DATA, RAW

Unprocessed, unanalyzed information, from which you wish to extract more meaningful, useful information.

DATA REDUCTION

The conversion of raw data into more concise, meaningful information.

De MORGAN'S THEOREM

A theorem which states that the inversion of a series of AND implications is equal to the same series of inverted OR implications, or the inversion of a series of OR implications is equal to the same series of inverted AND implications. In symbols:

$$\overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C} \qquad \cdot = \text{AND} \quad + = \text{OR}$$

$$\overline{A + B + C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$$

DEBUG

Detect, locate, and correct problems in a program or hardware.

DECIMAL

1. Pertaining to a characteristic or property involving a selection, choice, or condition in which there are ten possibilities.

2. Pertaining to the number representation system with a radix of ten.

*** DELAY TIME**

1. The time by which a signal is retarded.

* 2. A time interval specified in master clock periods that can be specified in each trace control level for comparison to that level's sample count.

DEMULTIPLEXER

A digital device that directs information from a single input to one of several outputs. Information for output channel selection usually is presented to the device in binary-weighted form and is decoded internally. The device also acts as a single-pole multipositional switch that passes digital information in a direction opposite to that of a multiplexer. See also **Multiplexing.**

*** DEMUX MODE**

An Input Mode, used to demultiplex data available on the same signal inputs at different times. For example, address information and the related data available on a shared bus. Operates on eight input lines. See also **Input Modes,** and especially **Latch Mode.**

DIAGNOSTICS

Methods used for detecting and isolating faults in a unit under test.

DIAGNOSTIC TEST

A test performed for the purpose of isolating a malfunction in the unit under test.

DIGIT

A symbol that represents one of the non-negative integers smaller than the radix. For example, in decimal notation, a digit is one of the characters from 0 to 9. Synonymous with numeric character.

DIGITAL

Data in the form of discrete states. In binary logic there are two states (represented as 1 or 0, ON or OFF, etc.). Compare to **Analog.**

DIGITAL CLOCK

A series of synchronized pulses that determines the bit times (data rate) of a digital pattern.

*** DIGITAL WAVEFORM**

1. A graphical representation of a digital signal, showing the variations in logic state as a function of time. This type of representation is also known as a timing diagram.

* 2. The timing display of the K101-D shows digital waveforms.

DIGITIZE

To translate analog data into digital form.

DIP

Dual In-line Package. A standard integrated circuit (IC) package in rectangular form with two rows of pins at opposite edges.

*** DISPLAY** (noun)

1. A device, such as a CRT monitor, that provides a visual presentation of an electronic signal.

* 2. A specific screen or mode used to present various menus and to review recordings.

DISPLAY (verb)

To visually present or exhibit; to show.

DUMP

1. To copy the contents of all or part of a storage, usually from an internal storage to an external storage.

2. A process as in definition 1 above.

3. The data resulting from the process as in definition 1 above.

*** EBCDIC**

1. The Extended Binary Coded Decimal Interchange Code, a digital code primarily used by IBM. It is eight-bit code for specifying letters, numbers, and certain control functions. See Code and ASCII.

* 2. One of the K101-D data formats. It decodes eight bits.

*** ECL**

One of the threshold choices for the K101-D.

ECL CIRCUITS

Bipolar emitter-coupled logic circuits, also called current-mode logic circuits.

EDGE

The transition from logic 0 to logic 1, or from logic 1 to logic 0, in a clock pulse. When a sample is taken.

EDGE TRIGGERING

Activation of a circuit at the edge of the pulse as it begins its change. Circuits then trigger at the beginning or end of the input pulse rather than sensing a level.

*** EDIT**

1. To insert, delete, or modify the form or format of data.

* 2. To rearrange, reformat, or change the K101-D data and/or displays.

EMULATE

To imitate one system with another such that the imitating system accepts the same data, executes the same programs, and achieves the same results as the imitated system. The results will be the same in form and function, but not necessarily in the same time.

to ENABLE

To permit the passage of a digital signal into or through a digital device or circuit.

to ENCODE

To use a code, frequently one composed of binary numbers, to represent individual characters or groups of characters in a message. For example, given positional information about the location of keys on a keyboard, to encode character codes for those keys. To change from one digital code to another. If the codes are greatly different, the process is called code conversion.

ERASE

To obliterate information from a storage medium, e.g., to clear, to overwrite.

ERROR

Any discrepancy between a computed, observed, or measured quantity and the true, specified, or theoretically correct value or condition.

EXECUTIVE

That portion of a computer cycle during which a selected control word or instruction is accomplished.

FALL TIME

The time required for the negative trailing edge of a pulse to decrease from 90% to 10% of its initial value. In digital electronics, the measured length of time required for an output voltage of a digital circuit to change from a high voltage level (logic 1) to a low voltage level (logic 0).

FAULT ISOLATION

The process of identifying and locating failures in a unit under test.

*** FIELD**

1. In a record, a specified area used for a particular category of data, e.g., a group of card columns used to represent a wage rate, a set of bit locations in a computer word used to express the address of the operand, etc.

* 2. For the K101-D, refers to areas on the setup screens where specifications are entered.

FIXED LOGIC LEVELS

Digital data with high and low levels that are not programmable or adjustable.

FLOW CHART

A symbolic representation of the algorithm required to solve a problem.

FORMAT

The arrangement of data.

FREQUENCY

The number of recurrences of a periodic phenomenon in a unit of time. Electrical frequency is specified as cycles per second (hertz).

FULL DUPLEX

A data transmission mode which provides simultaneous and independent transmission and reception. Compare to **Half Duplex.**

GATE (GATING DEVICE)

A circuit that regulates the passage of data inputs. A gate has two or more inputs and one output. One of the inputs can be clearly identified as a data input, with the remaining inputs being gating inputs. The logic state of the gating inputs determines whether or not the input data appear at the output.

to GATE

To control the passage of a digital signal through a digital circuit.

GATE PULSE

A pulse that enables a gate circuit to pass data signal. The gate pulse generally has a longer duration than the signal to ensure time coincidence.

GATE SIGNAL

Same as **gate pulse.**

GLITCH

An unwanted pulse or logic state, usually caused by poor design and/or propagation delays. A spurious event not necessarily synchronous with the system under test.

* **GLITCH MODE**

A special mode in the logic analyzer for detecting glitches. A glitch is detected when it crosses a threshold measurement of energy, that is a combination of time and voltage-level. It can be short and intense or long and barely above the threshold voltage. Either case can be detected.

* **GPIB**

1. General Purpose Interface Bus. An interface bus standard, also known as the IEEE-488 standard, and in Europe as the IEC Bus.

* 2. One of two communications options for the K101-D.

* **GRAPH DISPLAY**

One of three display modes of the K101-D, it displays a graph of data over time showing general relationships. It is the only display which can show the entire recording on one screen. The graph display can be expanded vertically or horizontally, and can be clipped to emphasis a particular region. The other displays, also defined, are **Data Display** and **Timing Display.**

GROUND

A conducting connection by which an electric circuit or equipment connects to the earth, or to some conducting body that serves in place of the earth.

HALF DUPLEX

A data transmission mode which provides both transmission and reception, though not simultaneously. Compare to **Full Duplex.**

HANDSHAKE

Interactive communication between two system components, such as between the CPU and a peripheral; often required to prevent loss of data. The two system components "agree" that one will send and the other receive data, and also exchange information about the success of the transfer.

HARDWARE

Physical equipment: mechanical, electrical, or electronic devices.

HERTZ

The unit of frequency, one cycle per second (Hz).

*** HEXADECIMAL**

1. A number system based upon the radix 16, in which the decimal numbers 0 through 9 and the letters A through F represent the sixteen distinct states in the code. A four-bit binary code, sometimes called base 16.

* 2. One of the K101-D data formats.

HIGH ADDRESS BYTE

The eight most significant bits in the memory address word for a microprocessor chip. Abbreviated H or HI.

*** IEEE-488**

1. An interface bus standard, also known as the GPIB standard, and in Europe as the IEC Bus.

* 2. One of two communications options for the K101-D.

*** INPUT**

1. Electrical currents or signals sent to a machine. The data conveyed by these signals.

* 2. Physical connectors where current or signals enter the K101-D.

*** INPUT DATA**

Input data comes into the K101-D from probes. Each input data line is interpreted as a binary 0 or 1, depending on the threshold voltage and the logic polarity assigned to that probe. There are 48 data inputs.

INPUT/OUTPUT

General term for the equipment used to communicate with a computer, the data involved in the communication, and the process of communication. Abbreviated I/O.

*** INPUT SIGNAL**

General K101-D term for the 60 probe inputs; 48 of these carry data and 12 carry clocking information.

*** INPUT MODES**

Possible modes of sampling input signals to the K101-D. Four modes are available. See **Sample Mode**, **Glitch Mode**, **Latch Mode**, and **Demux Mode**.

INCREMENT

To increase the value of a binary word by one.

INITIALIZE

To establish an initial condition or starting state; for example, to set logic elements in a digital circuit or the contents of a storage location to a known state so that subsequent application of digital test patterns will drive the logic elements to another known state.

INSTRUCTION

In programming, a statement that specifies an operation and the values or locations of its operands.

INSTRUCTION CODE

A unique binary number that encodes an operation that the microprocessor chip can perform.

INSTRUCTION CYCLE

A successive group of machine cycles, which together perform a single microprocessor instruction within the microprocessor chip.

INTERFACE

A shared boundary. An interface might be a hardware component to link two devices or it might be a portion of storage or registers accessed by two or more computer programs. Typically describes connection of a peripheral device to a computer system.

INTERFACING

The joining of members of a group, such as people, instruments, etc., so they can function in a compatible and coordinated fashion.

INTERRUPT

In a computer, a break in the normal flow of a system or routine such that the flow can be resumed from that point at a later time. The source of the interrupt may be internal or external.

I/O DEVICE

Input/output device. Any digital device, including a single integrated circuit chip, that transmits data or strobe pulses to a computer or receives data or strobe pulses from a computer.

*** JUMP**

1. To cause the next instruction to be selected from a specified storage location in a computer.

2. A deviation from the normal sequence of execution of instructions in a computer.

* 3. One of four trace control commands. Causes a jump from one level of trace to a new level, for example from level three to level seven.

See also **Branch**.

*** LABEL**

1. One or more characters used to identify a statement or an item of data in a computer program.

* 2. For the K101-D, refers to user-supplied labels that identify data inputs on the timing display.

LATCH

A simple logic storage element. A feedback loop used in a symmetrical digital circuit, such as a flip-flop, to retain a logic state.

*** LATCH ENABLE INPUTS**

The location where latch signals enter the K101-D.

*** LATCH MODE**

An input mode used to align two events separate in time so that they will be available for simultaneous evaluation. Latched information is captured at one time and sampled at a later time. Latch mode uses the latch enable expression to control when information is held and when it is released. When the latch enable expression moves from true to false, information is held, and when the latch enable expression goes true again, the latched information is available as a sample. For other input modes, see **Input Modes.**

*** LEVEL**

1. The degree of subordination in a hierarchy.

* 2. One of 16 programmable elements of K101-D's trace control.

LEVEL-TRIGGERED

The state of the logic input, being either logic 0 or logic 1, carries out a transfer of information or completes an action without requiring any change in the state.

LISTENER

Device that inputs data from a data bus (as defined specifically for the IEEE-488 bus). An output port is a listener. See also **Talker.**

LOGIC

1. The science dealing with the basic principles and applications of truth tables, switching, gating, etc.

2. Symbolic logic: A mathematical approach to the solution of complex situations by the use of symbols to define basic concepts. The three basic logic symbols are AND, OR, and NOT. When used in Boolean algebra, these symbols are somewhat analogous to addition and multiplication.

3. In computers and information processing networks, the systematic method that governs the operations performed on information, usually with each step influencing the one that follows.

4. The systematic plan that defines the interactions of signals in the design of a system for automatic data processing.

LOGIC ANALYZER

A test system specifically designed to record and/or analyze the operation of logic systems. Logic analyzers typically have 16 or more input lines and can store sequences of records showing the logical states of all inputs at consecutive moments in time.

LOGICAL DECISION

The ability of a computer to make a choice between two alternatives; basically, the ability to answer "yes" or "no" to certain fundamental questions concerning equality and relative magnitude.

*** LOGIC POLARITY**

1. Defines the usage of the logic symbols 0 (zero) and 1 (one). May be either positive or negative logic polarity. Positive logic polarity defines as 1 a voltage that is more positive than the threshold voltage. Negative logic polarity defines as 1 a voltage that is more negative than the threshold voltage.

* 2. Polarity can be set for all K101-D data inputs.

LOOP

A sequence of instructions that is repeated.

LOW ADDRESS BYTE

The eight least significant bits in the memory address word for an microprocessor chip. Abbreviated L or LO.

LSB (LEAST SIGNIFICANT BIT)

The digit with the lowest weighting in a binary number.

MACHINE CODE

A binary code that a computer decodes to execute a specific function.

MACHINE CYCLE

A subdivision of an instruction cycle during which time a related group of actions occur within the microprocessor chip. In the 8080 microprocessor, there are nine different machine cycles. All instructions are combinations of one or more of these machine cycles.

MACHINE LANGUAGE

Binary language (often represented in hex) that is directly understood by the processor. All other programming languages must be translated into binary code before they can be entered into the processor.

*** MANUAL ARMING**

See **Arm Modes.**

MEMORY

Part of a computer system into which information can be inserted and held for future use. Storage and memory are interchangeable terms. Common memory types are core, disk, tape, and semiconductor (which includes ROM and RAM).

*** MEMORY A, MEMORY B, MEMORY M**

The three K101-D memories: each consists of 515 words of 52 bits. 512 words contain recorded events. The first three words are part of the sampling logic of the K101D; the sample register and pipelines 1 and 2, which are used for delay during evaluation of the contents.

Memory M is the basic high-speed memory of the device. It is used for information capture. (Information capture is dependent on trace control.) Memory A is display memory; after the capture of information, a copy of memory M contents is transferred to memory A for display. Memory B is the reference memory, used for comparison with memory A. It may contain prior memory A information, or reference information entered by hand or by communication from a computer. See also **Word.**

MEMORY ADDRESS

A binary number that specifies the precise memory location of a memory word among the different possible memory locations.

MICROCOMPUTER

A fully operational digital computer that is based upon a microprocessor chip or microprocessor chip family. A complete system, including CPU, memory, and I/O interfaces.

MICROPROCESSOR

Central processing unit (CPU) fabricated on one or two chips. The processor consists of the arithmetic and logic unit, control block and registers.

MICROPROCESSOR DEVELOPMENT AID

Aids a design engineer in simulating or analyzing a logic circuit with one or more microprocessors.

MICROPROCESSOR EMULATOR

Imitates the functions of a specific microprocessor; a software routine or a device.

MNEMONIC CODE

Codes designed to assist the human memory. The microprocessor language consists of binary words, which are a series of 0's and 1's, making it difficult for the programmer to remember the instructions corresponding to a given operation. To assist the human memory, the binary numbered codes are assigned groups of letters (or mnemonic symbols) that suggest the definition of the instruction. For example, the code A9 might mean load accumulator and be represented by the mnemonic LDA.

MNEMONIC LANGUAGE

A programming language that is based upon easily remembered symbols and that can be assembled into machine code by a computer.

MNEMONIC INSTRUCTION

Computer instructions that are written in a meaningful notation, e.g., ADD, SUB, MOV, MPY, DIV, and STO.

MNEMONIC SYMBOL

A symbol chosen so that it assists the human memory; e.g., the abbreviation MPY used for "multiply."

MODEM

From MOdulator-DEModulator. A device that modulates and demodulates signals transmitted over communication facilities.

MSB (MOST SIGNIFICANT BIT)

Bit in the leftmost position of a word, which has the greatest numerical weight.

MULTIPLEXING

Process of transmitting more than one signal via a single link. The most common technique used in microprocessor systems is time division multiplexing, in which one signal line is used for different information at different times. See also **Demultiplexer.**

NAND GATE

A combination of a NOT function and an AND function in a binary circuit that has two or more inputs and one output. The output is logic 0 only if all inputs are logic 1; it is logic 1 if any input is logic 0.

NEGATIVE EDGE

The transition from logic 1 to logic 0 in a clock pulse.

NEGATIVE-EDGE TRIGGERED

Transfer of information occurs on the negative edge of the clock pulse.

NEGATIVE LOGIC

The logic false state is represented by the more positive voltage in the system, and the logic true state is represented by the more negative voltage in the system. For TTL, 0 becomes +2.4 volts or greater, and 1 becomes +.4 volts or less.

NESTED

A subroutine that is called by another subroutine or a loop within a larger loop is said to be nested.

NOISE

Unwanted disturbances superimposed upon a useful signal that tend to obscure the signal's information content.

NOR GATE

An OR gate followed by an inverter to form a binary circuit in which the output is logic 0 if any of the inputs is logic 1 and is logic 1 only if all the inputs are logic 0.

NOT GATE

A binary circuit with a single output that is always the opposite of the single input. Also called an inverter circuit.

*** OCTAL**

1. A number system based upon the radix 8, in which the decimal numbers 0 through 7 represent the eight distinct states. Also called base 8. Decodes the three-bit patterns 000 through 111 as 0 through 7.

* 2. One of the K101-D data formats.

OPERATION

Moving or manipulating data in the CPU or between the CPU and peripherals.

*** OR**

1. An operation in Boolean algebra. When two or more terms are ORed together (combined using the OR operation), the result is true if at least one of the terms is true.

* 2. One of the two operations used in specifying clocking modes. The other, also defined, is **AND**.

OSCILLOSCOPE

An instrument which repetitively displays the instantaneous value of one or more varying electrical quantities as a function of time.

OUTPUT PORT

Circuit that allows the microprocessor system to output signals to other devices.

OVERFLOW

Results when an arithmetic operation generates a quantity beyond the capacity of the register. An overflow status bit (the carry) in the flag register is set if an operation causes an overflow.

*** PAGE**

A unit of displayed information. In Timing display, each page displays six inputs. In Data display, it is a single column of information.

PARALLEL

Simultaneous processing, transmission, or storage of data bits. Compare to **Serial**.

PARAMETER

A variable that is given a constant value for a specific purpose or process.

*** PASS COUNT**

1. A variable that is used to count the number of occurrences of some particular event.

* 2. For the K101-D, a pass counter can be used to specify the number of recording processes to be done automatically.

PERIPHERAL EQUIPMENT

Units which work in conjunction with a computer but are not part of it.

*** POD**

An external device containing the actual probe circuitry used to monitor the target system. Eight sample inputs plus two clock or latch enable inputs are contained in each pod. Six pods are used with the K101-D.

*** POLARITY**

See **Logic Polarity.**

POLLING

Determing something by the process of sequential inquiry. One method used to identify the source of interrupt request. The CPU must poll (read) the devices to determine which one caused the interrupt.

PORT

Point at which the I/O devices are connected to the computer.

POSITIVE EDGE

The transition from logic 0 to logic 1.

POSITIVE-EDGE TRIGGERED

Transfer of information occurs on the positive edge of the clock pulse.

POSITIVE LOGIC

A form of logic in which the more positive voltage level represents logic 1 and the more negative level represents logic 0.

PRECISION

Number of digits. Contrasts with **Accuracy.**

PRIORITY

Number assigned to an event or device that determines the order in which it will receive service if more than one request is made simultaneously.

* **PROBE CONNECTION**

Process of specifying and connecting the probes between the K101-D and the system under test. Of the 60 probe lines, 48 carry data and 12 carry clocking information. The probe information is referred to as "input signals", further divided into "input data" and "clock signals."

* **PROBES**

The connections between the K101-D and the system under test. See **Probe Connection** for further information. See also **Pod.**

PROGRAM

Procedure for solving a problem, coded into a form suitable for use by a computer. Frequently referred to as software.

PROPAGATION DELAY

A measure of the time required for a logic signal to travel through a logic device or a series of logic devices. It occurs as the result of four types of circuit delays: storage, rise, fall, and turn on. It is the time between the input signal crossing the threshold voltage point and the responding voltage at the output crossing the same voltage point.

*** RADIX, RADICES**

1. Also called the base. The total number of distinct marks or symbols used in a numbering system. For example, since the decimal numbering system uses ten symbols, the radix is 10. In the binary numbering system, the radix is 2, because there are only two marks or symbols (0 and 1). In the octal numbering system, the radix is 8, and in the hexadecimal numbering system, the radix is 16.

* 2. Radix is used on the K101-D setup screens to refer to any of the three number bases used in Data display: binary, octal, or hexadecimal, and also to the ASCII and EDCDIC codes. See also, **Code**.

READ

To retreive or acquire data that have been stored. In semiconductors: To transmit data from a semiconductor memory to some other digital electronic device. The term "read" also applies to computers and other types of memory devices. To READ is to recall.

REAL-TIME CLOCK

Refers to a device that provides interrupts at regular time intervals, frequently twice the AC line frequency. It allows maintenance of an accurate time-of-day clock and the measurement of elapsed time.

* **RECORDING**

The result of the tracing process in the K101-D. More information may be traced than can be recorded, because when memory fills prior data is replaced by newly traced data.

* **RECORDING ANALYSIS**

The process of analyzing the recording obtained by the K101-D to see whether a solution has been obtained, or when necessary to record again, what changes might be made in the conditions for recording. Three modes of displaying data are available to aid in recording analysis, with many other functions available for manipulating and analyzing these displays. See also **Data Display**, **Graph Display**, and **Timing Display**.

* **RECORDING CYCLE**

A complete cycle of tracing based on the set of trace control instructions and the conditions in the system under test at the time of recording. Depending on the Arm Mode, the recording cycle may end the recording process or may be repeated. See **Arm Mode**.

* **RECORDING PROCESS**

Depending on the Arm mode set for the K101-D, the process of making a recording may end with one recording cycle or may be repeated. The recording process consists of one or more recording cycles. See **Recording Cycle**.

RETURN

A special type of jump in which the CPU resumes execution of the main program by returning to the location of the instruction which had previously caused the main program to be interrupted. See also **Subroutine.**

RISE TIME

The time required for the positive edge of a pulse to rise from 10% to 90% of its final value. It is a measure of the steepness of the wavefront. In digital electronics, the measured length of time required for an output voltage of a digital circuit to change from a low voltage level (logic 0) to a high voltage level (logic 1).

ROUTINE

A group of instructions that causes the computer to perform a specified function.

* **RS232-C**

1. An Electronic Industries Association standard for connecting computer components or peripherals to the main computer.

* 2. One of two communications options for the K101-D.

SAMPLE-AND-HOLD CIRCUIT

A circuit that monitors a voltage level during a short time period and accurately stores that voltage level for a much longer time period.

* **SAMPLE COUNT**

A variable which counts the number of times that the inputs to the logic analyzer have been sampled. The number of master clock (or A pattern) occurrences since entering a trace level. Sample count is reset to zero on each level entry; the resulting count is then used for comparison to that level's specified delay value.

*** SAMPLE INPUTS**

Where data enter the K101-D, 48 sample inputs are provided.

*** SAMPLE MODE**

Inputs are sampled only at each active edge of the specified sample clock. See **Input Modes.**

*** SELF-TEST**

1. Test performed by a product on itself.
* 2. One of the K101-D diagnostic routines.

SEQUENCING

Control method for placing a set of steps in a particular order or occurrence.

SERIAL

Transmitting data bits one at a time over a single wire instead of using one wire for each bit. Compare to **Parallel.**

SERIAL OPERATION

The organization of data manipulation within circuitry wherein the digits of a word are transmitted one at a time along a single line. The serial mode of operation is slower than parallel operation, but utilizes fewer lines.

*** SETUP**

The parameters specified for a particular recording.

*** SETUP SCREENS**

Display screens used for specifying recording conditions for the K101-D. The screens have fields where choices may be selected from preset options or may be entered. The screens are interactive, and change their presentation of possibilities according to the information entered.

SETUP TIME

The minimum amount of time that data must be present at an input to ensure data acceptance when the device is clocked.

SHIFT

To move the characters of a unit of information right or left. For a binary number, this is equivalent to multiplying or dividing by two for each shift.

SOFTWARE

The totality of programs and routines used to extend the capabilities of computers, including compilers, assemblers, linker-loaders, narrators, translators, and subroutines.

*** SPECIFICATION**

In the K101-D, the process of specifying conditions for making a recording of activity in the system under test. Specification is done by selecting or entering information in the Setup Menus (Setup Screens).

SPIKE

A distortion in the form of a pulse waveform of relatively short duration superimposed on an otherwise regular or desired pulse waveform. See also **Glitch.**

STATE

The logic condition of an input or output of a circuit, either logic 1 or a logic 0. The state of a circuit (gate or flip-flop) refers to its output. A flip-flop is said to be in the logic 1 state when its output is 1. A gate is in the logic 1 state when its output is 1.

*** STATE DISPLAY**

See **Data Display.**

STATUS

Present condition of the device. Usually indicated by registers.

*** STOP**

One of four trace control commands. Causes trace control to stop; transfers traced samples from memory M to display memory, memory A.

SUBROUTINE

A routine that causes the execution of a specified function and which also provides for transfer of control back to the calling routine upon completion of the function. Also known as **Call.**

SUT

System under test; the device being studied. Also referred to as the target system.

SYNC

Short for synchronous, synchronization, synchronizing, etc.

to SYNCHRONIZE

To lock one element of a system in step with another.

SYNCHRONOUS

Operation of a switching network by a clock pulse generator. All circuits in the network switch in a fixed relation to the clock signal.

SYNCHRONOUS CIRCUIT

A circuit in which all ordinary operations are controlled by signals from a master clock.

SYNCHRONOUS LOGIC

The type of digital logic used in a system in which logical operations take place synchronously with clock pulses.

SYNCHRONOUS OPERATION

Operation of a system under the control of clock pulses.

*** SYNCHRONOUS RECORDING**

A recording in which the data are sampled by a clock that is synchronous with the data. Usually the case when using external clock. See also **Asynchronous Recording.**

SYSTEM

1. An assembly of methods, procedures, or techniques united by regulated interaction to form an organized whole.

2. An organized collection of people, machines, and methods required to accomplish a set of specific functions.

TALKER

A device that outputs data to the data bus (as defined specifically for IEEE-488 bus). See also **Listener.**

TARGET SYSTEM

See **SUT.**

* **TERM**

In Boolean algebra, an element of the Boolean expression. In the K101-D, terms are clock signals being combined to specify clocking modes.

* **THRESHOLD**

1. In digital logic, a voltage limit above or below which a signal is recognized as defined value, usually the binary digit of 1 or 0. See **Logic Polarity.**

* 2. One of the specifications for the K101-D.

TIME DOMAIN

Information that is a direct function of time. An oscilloscope displays information in the time domain.

* **TIMING DISPLAY**

One of three display modes of the K101-D, it displays individual data inputs over time, showing their rise and fall based on the underlying value of 1 or 0 recorded for each line. The display allows comparison of events in time, and can be manipulated to make these relationships clearer. The other displays, also defined, are **Data Display** and **Graph Display.**

TIMING LOOP

A software loop that requires a precise period of time for its execution.

* **TRACE**

1. One of four commands in trace control. Controls whether or not events are entered into memory M.

* 2. To put a sample into memory M.

*** TRACE CONTROL**

A sophisticated digital recording process that can conditionally trace precisely defined, distinct segments of data or program flow. Each segment may be separated by an indefinite time period or number of samples from the other captured segments. The user specifies a chain of unique interactions of time and data patterns to define the desired information capture.

As implemented in the K101-D, this process is accomplished by providing 16 identical levels, each with four concurrently evaluated major commands: STOP, JUMP, ADVANCE, and TRACE. Specification of trace events is independent of event monitoring; the events may be the same or different. STOP, JUMP, and ADVANCE are used to control the monitoring of events in the target system; TRACE controls whether or not the events are entered into memory M. A delay may be associated with each command and level.

TRANSITION

The instance of changing from one state to a second state.

TRIGGER

A pulse, often defined by a combination of states, used to initiate or stop some function, for example, a triggered sweep or delay ramp.

TTL

Bipolar semiconductor transistor-transistor coupled logic circuits.

UUT (UNIT UNDER TEST)

Any system, set, subsystem, assembly or subassembly undergoing testing.

VARIABLE

A quantity that can assume any of a given set of values.

*** WORD**

The maximum number of binary digits that can be stored in a single addressable memory location of a given computer system. The basic unit for storing events in memory. The K101-D has 48 bits for data and four bits for trace level value (0-F). Each data bit corresponds to one input signal.

WRITE

In semiconductors and other types of memory devices, to transmit data into a memory device from some other digital electronic device. To WRITE is to STORE.

Section 14

INPUT CONNECTION GUIDE AND SETUP GUIDE

14.1 INTRODUCTION

Two forms have been created to help you determine how to set up the K101-D to sample your target system, implement that set up, and maintain a permanent record of it for future reference. The Input Connection Guide shows the interconnection between target system signals and K101-D inputs. The Setup Guide shows the specific setup parameters selected for a recording. The Setup Guide interacts with and makes use of the Input Connection Guide information.

A small supply of blank forms is included with this section. If additional forms are needed, photocopying or reprinting them is permitted and recommended. You may obtain additional copies from:

Communication Department
Gould Instrument Division
4600 Old Ironsides Drive
Santa Clara, CA 95050-1279

Please request forms by name and number:

K101-D Input Connection Guide	DWS 45
K101-D Setup Guide	DWS 24

The following is a description of each form with instructions and examples of how to use it. One method of using the form is suggested here. After some use you will likely develop your own method and shorthand notation, especially with the Setup Guide.

For your convenience, suggested connection guides for popular microprocessors are presented after the explanation of each form.

14.2 INPUT CONNECTION GUIDES

Before filling out a connection guide form, it is a good idea to spend some time analyzing the system you want to probe. Determine what information you need to observe. Define what you need to do to obtain a comprehensive sample. Consider the polarity and threshold of each signal, the information contained therein, how the signal relates to other signals, and how you want to sample it. In many cases, you may suspect that a certain area or set of signals or data, and so on, is the source of the problem you are investigating. If you happen to choose the wrong test points or recording analysis, the results obtained with the K101-D will assist you in refining your problem definition. The inherent flexibility of the K101-D allows you to quickly change your test approach, setup, clocking sequences, and so on. The K101-D's ability to easily rearrange the inputs of its Timing Data and Graph displays as well as clocking expressions, however, allows you a lot of flexibility in making your connection selections. You can change your mind without changing connections.

Refer to the front panel of the K101-D (see Figure 14-1). The clock and data inputs of each section (A, B, C) are identical. Therefore, the left side of the form lists the type of K101-D input (clock, data/sample, or ground), an identifying input number or name (0-F, J, K, R, S, GND), and the color of the associated flying lead wire. These are the same for sections A, B, and C. In the target system area of the form, you assign each desired target system signal and precisely identify the target system signal by engineering drawing reference designation, IC type, pin number, and signal name.

14.2.1 SN74L192 DECADE COUNTER

Assume you need to asynchronously observe all input and output signals of an SN74L192 decade counter. The pinout and timing diagrams are shown

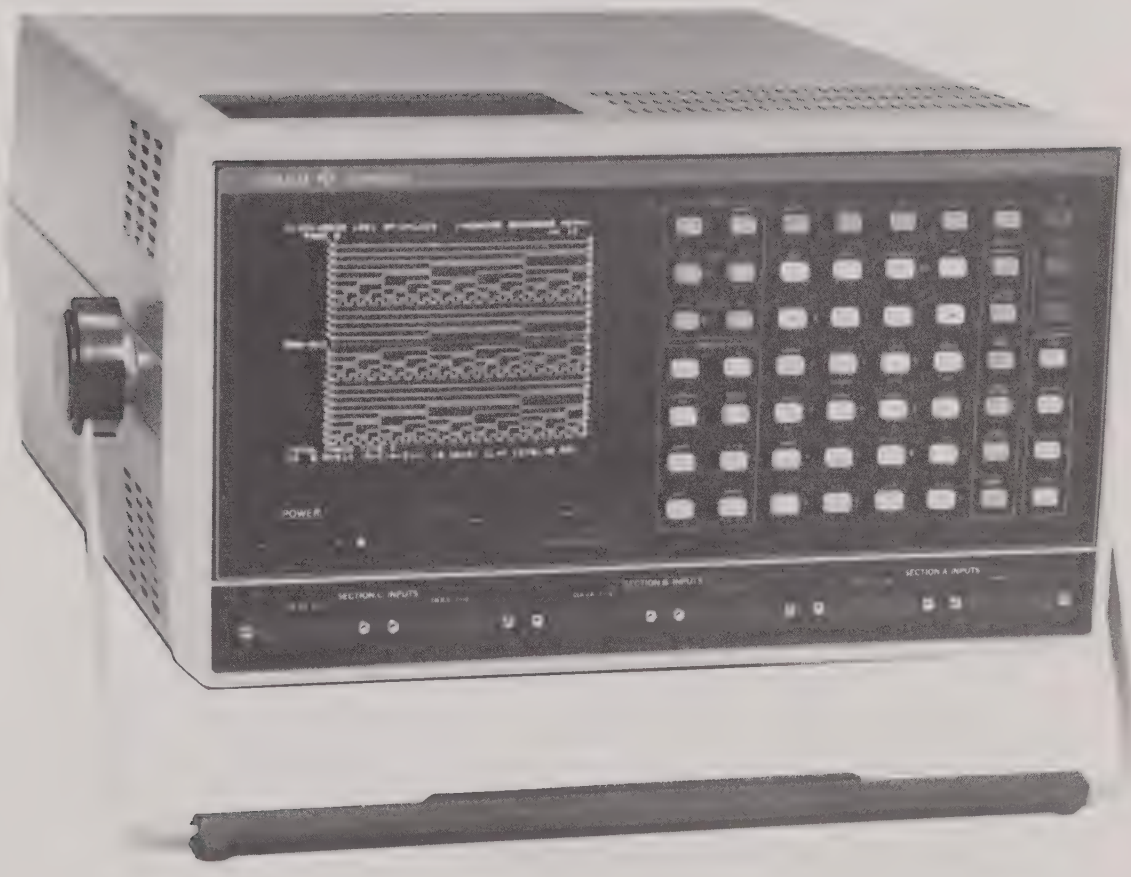


Figure 14-1. K101-D Front Panel.

in Figure 14-2.[1] The K101-D Input Connection Guide for this example is shown in Figure 14-3.

14.2.2 8085A MICROPROCESSOR

Assume you need to synchronously observe the operation and bus activity of an 8085A microprocessor. The pinout connections of the 8085A are shown in Figure 14-4. A study of the basic system timing indicated that the connections as shown in Figure 14-5 should be made.

14.3 SETUP GUIDES

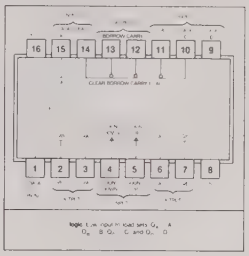
Each form contains one block for each of the five recording setup menus: Clock Select, Input Mode, Trace Control, Logic Polarity, and Data Format. They are organized in the order you are most likely to think of them when setting up a recording. Even setup menus that actually consist of multiple screens (Clock Select, Data Format, and Trace Control) are accommodated by this single form. Blanks exist for any possible parameter or group of parameters you may wish to select. There are numerous notes throughout the form to help remind you of the possible parameter choice. The format resembles but does not exactly duplicate the format you see on the CRT screen. There are also blanks for a parameter's QUICK key number (to speed up keyboard entry). Often, you only need to fill in the blanks for those parameters you are using. For example, if you are not using a particular section, the parameter associated with that section may be ignored.

a. **Clock Select:** Refer back to your Input Connection Guide for the signals of a specific section to determine how you want to sample that section's inputs. Specify the exact internal clock period or external expression needed and mark the

1. Reprinted by permission of Texas Instruments from the TTL Date Book, Second Edition.

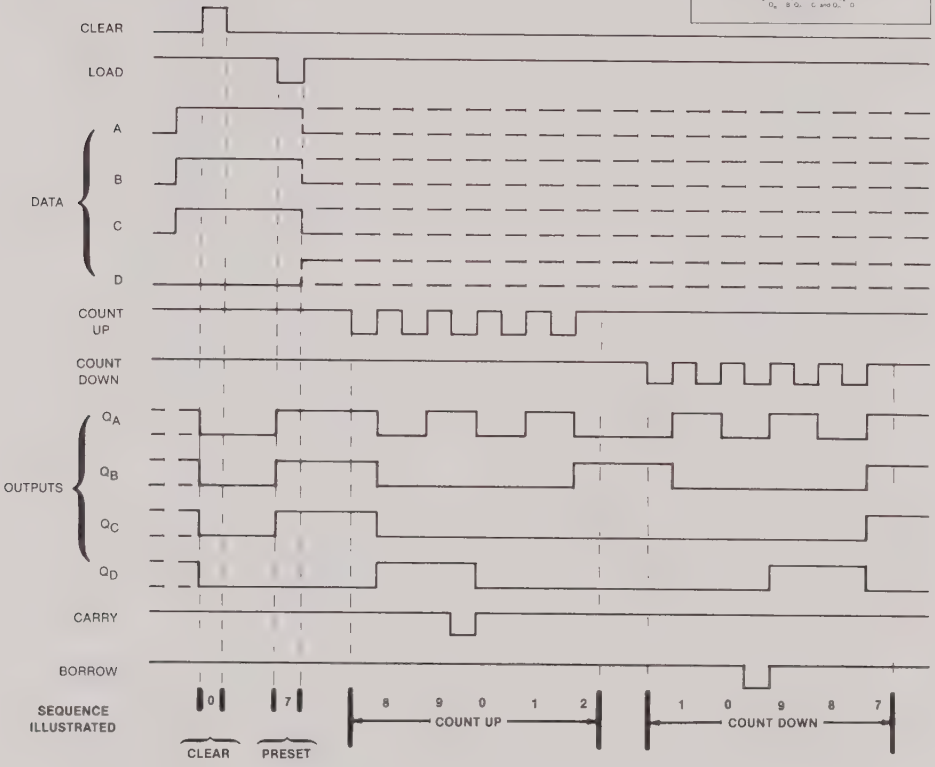
TYPES SN54192, SN54L192, SN54LS192, SN74192, SN74L192, SN74LS192
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

'192, 'L192, 'LS192 DECADE COUNTERS



Typical clear, load, and count sequences

Illustrated below is the following sequence:
1. **Clear outputs to zero.**
2. **Load (preset) to BCD seven.**
3. **Count up to eight, nine, carry, zero, one, and two.**
4. **Count down to one, zero, borrow, nine, eight, and seven.**



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

Reprinted by permission of Texas Instruments from the TTL Data Book, Second Edition.

Figure 14-2. Types SN54192, SN54L192, SN54LS192, SN74192, SN74L192, and SN74LS192 Synchronous 4-Bit Up/Down Counters (Dual Clock with Clear).

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM DECADE COUNTER SET UP # 1.1 OF ____ DATE _____

K101-D			TARGET SYSTEM								
			SECTION C			SECTION B			SECTION A		
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J									
CLK	GRY	K									
DATA	VIO	F									
DATA	BLU	E									
DATA	GRN	D									
DATA	YEL	C							14	CLEAR	74L192
DATA	ORG	B							11	LOAD	74L192
DATA	RED	A							15	DATA A	74L192
DATA	BRN	9							1	DATA B	74L192
DATA	BLK	8							10	DATA C	74L192
GND	LT BRN	GND							9	DATA D	74L192
									8	GND	74L192
CLK	WHT	R									
CLK	GRY	S									
DATA	VIO	7									
DATA	BLU	6							5	COUNT UP	74L192
DATA	GRN	5							4	COUNT UP	74L192
DATA	YEL	4							3	QA	74L192
DATA	ORG	3							2	QB	74L192
DATA	RED	2							6	QC	74L192
DATA	BRN	1							7	QD	74L192
DATA	BLK	0							12	CARRY	74L192
GND	LT BRN	GND							13	BORROW	74L192
									8	GND	74L192

DWS45-12.5183

Figure 14-3. Decade Counter Connection Guide.

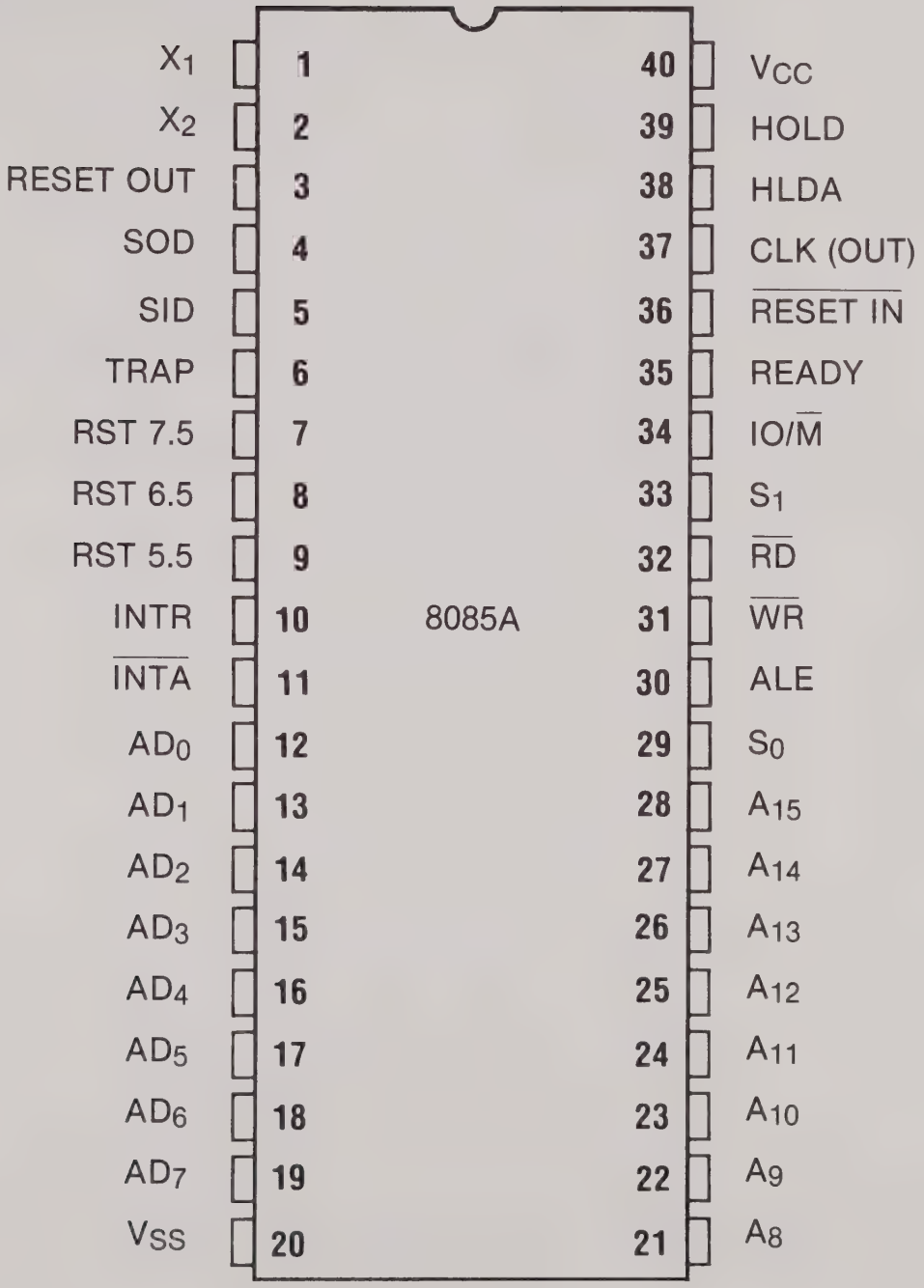


Figure 14-4. 8085A Pinout Diagram.

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM 8085 A SET UP # 1.2 OF ____ DATE _____

K101-D			TARGET SYSTEM								
			SECTION C			SECTION B			SECTION A		
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J	11	$\overline{INTA}$	8085A	31	$\overline{WR}$	8085 A	32	$\overline{RD}$	8085 A
CLK	GRY	K							37	CLK(OUT)	8085 A
DATA	VIO	F				6	TRAP	8085 A			
DATA	BLU	E				7	RST 7.5	8085 A			
DATA	GRN	D				8	RST 6.5	8085 A			
DATA	YEL	C				9	RST 5.5	8085 A			
DATA	ORG	B				10	INTR	8085 A			
DATA	RED	A				34	IO/$\overline{M}$	8085 A			
DATA	BRN	9				33	S1	8085 A			
DATA	BLK	8				29	S0	8085 A			
GND	LT. BRN	GND				20	Vss	8085A			
CLK	WHT	R							30	ALE	8085 A
CLK	GRY	S									
DATA	VIO	7				28	A 15	8085 A	19	AD 7	8085 A
DATA	BLU	6				27	A 14	8085 A	18	AD 6	8085 A
DATA	GRN	5				26	A 13	8085 A	17	AD 5	8085 A
DATA	YEL	4				25	A 12	8085 A	16	AD 4	8085 A
DATA	ORG	3				24	A 11	8085 A	15	AD 3	8085 A
DATA	RED	2				23	A 10	8085 A	14	AD 2	8085 A
DATA	BRN	1				22	A 9	8085 A	13	AD 1	8085 A
DATA	BLK	0				21	A 8	8085 A	12	AD 0	8085 A
GND	LT BRN	GND				20	Vss	8085 A	20	Vss	8085 A

DWS45-12.5183

Figure 14-5. 8085A Connection Guide.

appropriate box. Do this for each section. When you are finished, refer to the clocking notes to determine what mode you need. For example, if you chose the same internal rate for each section, then you should select Internal mode. If section C is an external expression, section A internally clocked, and section B a different external expression, then you must select Mixed Multiphase mode. If you are using an internal clock, fill in the desired internal clock period and check off the appropriate unit's box. If you are externally clocking any section, the master clock expression must be defined. Regardless, a master clock must always be specified as either an external expression or an internal clock period. If you are going to be latching or demultiplexing any section, then you must specify the enable expression for that section.

Notice that above the dotted blank lines of the external sample clock expressions is the name of the specific section clock input that is associated with that blank. Similarly, the name of each specific section enable clock input is listed above its associated dotted blank line in the enable expression. When creating a Boolean expression, you can either fill in the name of the K101-D clock input or the name of your target system signal. In this manual, the clock input name is used. For each clock input used, you must also select its active edge or logic polarity. Remember that resultant clocks are always active on their rising edge and resultant enable expressions use positive logic.

b. **Input Mode:** For every group of section inputs you are using, you need to specify an input mode and threshold type. If the threshold is variable, then you must specify a value.

You must select one of the six arm modes. If you want to limit the number of automatic recordings or set cursor

boundary limits on autocomparing, then you must specify those values. The input notes list all possible choices.

c. **Logic Polarity:** For each data input use, put a + or - in the appropriate blank in the table of input names vs. section letter. (If all inputs are positive, you may just want to put one large plus sign in the middle of the table rather than fill in each blank individually.)

d. **Data Format:** Refer back to your Input Connection Guide when choosing and filling out your desired data format. For mixed modes, put on the top line the letter representing the radix chosen for a group of inputs. The specific signal identifiers (CF-A0) comprising that character go in the column beneath the radix letter. The most significant bit of each character is always at the top of the column. The "height" of the column depends on the number of characters in the chosen radix or code. For the fixed formats, the instrument determines the radix and inputs for you. Simply copy the fixed format onto the form. There are 48 columns available. If you display no more than 24 characters, you will find it easier to use two columns per character rather than one. You may want to write the name of your selected data format in the space to the right of the DATA FORMAT heading and fill in the associated QUICK key number.

e. **Trace Control:** Each form has space for four levels of trace control. There is a space for comments about the purpose and activity of each level. If your trace program requires more than four levels, simply use more forms. Beginning with level 0, fill in the particular STOP, JUMP, ADVANCE, and TRACE commands you need. Since TRACE is independent of the other three commands, it is easiest to think first about what samples you want traced into memory. Second, determine the

event you want to occur in order to advance out of the level you are currently in. Third, any exception to the order of trace control flow or branching should be implemented as a JUMP command. Finally, decide the conditions you want to stop the entire recording. If you select NEVER or ALWAYS for a command, there is no need to fill in the associated word recognizer. For the other seven commands, the word recognizer must be specified.

To speed up your final program entry, refer to the trace control notes and write down the QUICK key value of each command. If delay is used in any command, you must then specify its type and value. If not, that field may be left blank. However, if you are delaying by A PATTERNS, the A word recognizer must be specified even if its command is ALWAYS or NEVER. Remember that each space on the word recognizer line corresponds to the data format column aligned above it, as it does on the actual Trace Control screen. If you are using an end level other than F, then it must be filled in.

14.3.1 DEFAULT MENU

If the default menu setups were translated into a completely filled out setup form, they would appear as in Figure 14-6. Press **SHIFT, RECALL** to call up the default menus so you can compare them to the form. A shorthand version of the same form would look like that shown in Figure 14-7.

14.3.2 SN74L102 SETUP

Refer back to the input connection example shown in Figure 14-3. Asynchronously sampling all inputs and outputs of the SN74L192 requires that section A be internally sampled. The clock period is selected from studying the chips' timing characteristics (not shown here). The input

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # 2.0 OF ___ DATE _____

QUICK KEY (See back for notes) (3) **DATA FORMAT** MIXED USER SEQN.

RADIX: H H H H H H H H H H H H

MSB	
I 6	
D N 5	
A P 4	
T U 3	CEC8C7C3 BEBBB7B3 AEA8A7A3
A T 2	CECAC6C2 BEBAB6B2 AEAAA6A2
S 1	CDC9C5C1 BDB9B5B1 ADA9A5A1
LSB	CCC8C4C0 BCB8B4B0 ACA8A4A0

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each sub-trace:
TRACE ON / INCREMENT / STOP for priority from JUMP
JUMP TO / ADVANCE
QUICK KEY

0 DATA = D
1 ALWAYS
F NEVER
1 DATA D = Sample Count Delay
4 DATA D = Sample Count Delay
5 DATA D = Sample Count Delay
6 DATA D = Pattern Count Delay
7 DATA D = Sample Count Delay
E DATA D = Sample Count Delay

D S T A = Pattern Recognition Trigger type

TRACE CONTROL

QUICK KEY LEVEL 0 (0-F) DELAY = DEC (DEC/HEX) 515 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (0-F) — COMMENTS

(3) STOP IF DATA = 5 AND SAMPLE COUNT > DELAY

S = X X X X X X X X X X X X

(2) JUMP TO 0 (0-F) NEVER

J = X X X X X X X X X X X X

(2) ADVANCE NEVER

A = X X X X X X X X X X X X

(1) TRACE ALWAYS

T = X X X X X X X X X X X X

QUICK KEY LEVEL ___ (0-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F) — COMMENTS

(.....) STOP

S =

(.....) JUMP TO ___ (0-F)

J =

(.....) ADVANCE

A =

(.....) TRACE

T =

QUICK KEY LEVEL ___ (0-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F) — COMMENTS

(.....) STOP

S =

(.....) JUMP TO ___ (0-F)

J =

(.....) ADVANCE

A =

(.....) TRACE

T =

QUICK KEY LEVEL ___ (0-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (0-F) — COMMENTS

( ) STOP

S =

( ) JUMP TO ___ (0-F)

J =

(.....) ADVANCE

A =

(.....) TRACE

T =

Figure 14-6. Default Setup (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM DEFAULT SET UP # 2.0a OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (0) MODE = INTERNAL

	CJ	BJ	AJ	CK	BK	AK
INTERNAL CLOCK PERIOD = 20				☐ NANOSECONDS (20-1600) ☐ MICROSECONDS (1-1600) ☐ MILLISECONDS (1-160)		
MASTER = ■ INTERNAL ☐ EXT	(_____●_____●_____) + (_____+_____+_____)					
SECTION C = INT ■ SAME AS MASTER ☐ 10 NANOSECONDS						
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)						
SECTION B = INT ■ SAME AS MASTER ☐ 10 NANOSECONDS						
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)						
SECTION A = INT ■ SAME AS MASTER ☐ 10 NANOSECONDS						
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____+_____+_____)						

ENABLE CLOCKS: Used only in Latch and Demux

	CR	BR	AR	CS	BS	AS
SECTION C =	(CR ↑●_____●_____) + (_____+_____+_____)					
SECTION B =	(CR ↑●_____●_____) + (_____+_____+_____)					
SECTION A =	(CR ↑●_____●_____) + (_____+_____+_____)					

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence
1	OCTAL Fixed octal format & CF-A0 sequence
2	BINARY Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN Any radix any sequence
4	MIXED CF-A0 SEQN Any radix fixed CF-A0 sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE-816 attached OR DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL

1 EXTERNAL — SINGLE PHASE

2 EXTERNAL — MULTI PHASE

3 MASTER — SINGLE PHASE

4 MASTER — MULTI PHASE

5 MASTER — SLAVE

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8	SAMPLE	TTL	+1.40
C7 — C0	SAMPLE	TTL	+1.40
BF — B8	SAMPLE	TTL	+1.40
B7 — B0	SAMPLE	TTL	+1.40
AF — A8	SAMPLE	TTL	+1.40
A7 — A0	SAMPLE	TTL	+1.40

PASS COUNTER: LIMIT = 0000 (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = 0 TO 514 (CURSORS C: 0-512 R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	−1.30 VDC
A	VARA	−9.99 TO +9.99 VDC
B	VARB	−9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A < B
3	AUTO STOP IF A > B
4	AUTO STOP IF A < B WITHIN LIMITS
5	AUTO STOP IF A > B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
GROUP B	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
GROUP A	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
−	NEGATIVE

DWS24-12.5183

Figure 14-6. Default Setup (Sheet 2 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM DEFAULT SET UP # 2.06 OF ___ DATE _____

QUICK KEY (See back for notes) (3) **DATA FORMAT** MIXED USER SEQN.

RADIX: H H H H H H H H H H H H

MSB															
I	6														
D	N	5													
A	P	4													
T	U	3	C	F	C	8	C	7	C	3	B	F	B	8	B
A	T	2	C	E	C	A	C	6	C	2	B	E	B	A	B
S		1	C	D	C	9	C	5	C	1	B	D	B	9	B
LSB			C	C	C	8	C	4	C	0	B	C	B	8	B

7	6	5	4	3	2	1	0	
B	7	B	6	B	5	B	4	
A	7	A	6	A	5	A	4	
B	3	B	2	B	1	B	0	
A	3	A	2	A	1	A	0	

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is [illegible]
STOP [illegible]
JUMP [illegible]
ADVANCE [illegible]
At [illegible]
[illegible]
Quick Key [illegible]

0 If DATA ≠ D
1 Always
2 Never
3 If DATA = [illegible]
4 If DATA ≠ [illegible]
5 If DATA = [illegible]
6 If DATA < [illegible]
7 If DATA = [illegible]
8 If DATA ≠ [illegible]

ID = S, J, A, or T which are assigned by command type

TRACE CONTROL

QUICK KEY (3) LEVEL 0 O-F DELAY = DEC 515 DEC/HEX 0-65 K CLOCKS CLOCKS/A PATTERNS END LEVEL F O-F — COMMENTS

(3) STOP IF DATA = 5 AND SAMPLE COUNT > DELAY
S = X X X X X X X X X X X X X X X X

(2) JUMP TO 0 O-F NEVER
J = _____

(2) ADVANCE NEVER
A = _____

(1) TRACE ALWAYS
T = _____

QUICK KEY (.....) LEVEL ___ O-F DELAY = _____ DEC/HEX 0-65 K _____ CLOCKS/A PATTERNS END LEVEL ___ O-F — COMMENTS

(.....) STOP _____
S = _____

(.....) JUMP TO ___ O F _____
J = _____

(.....) ADVANCE _____
A = _____

(.....) TRACE _____
T = _____

QUICK KEY (.....) LEVEL ___ O-F DELAY = _____ DEC/HEX 0-65 K _____ CLOCKS/A PATTERNS END LEVEL ___ O-F — COMMENTS

(.....) STOP _____
S = _____

(.....) JUMP TO ___ O F _____
J = _____

(.....) ADVANCE _____
A = _____

(.....) TRACE _____
T = _____

QUICK KEY (.....) LEVEL ___ O-F DELAY = _____ DEC/HEX 0-65 K _____ CLOCKS/A PATTERNS END LEVEL ___ O-F — COMMENTS

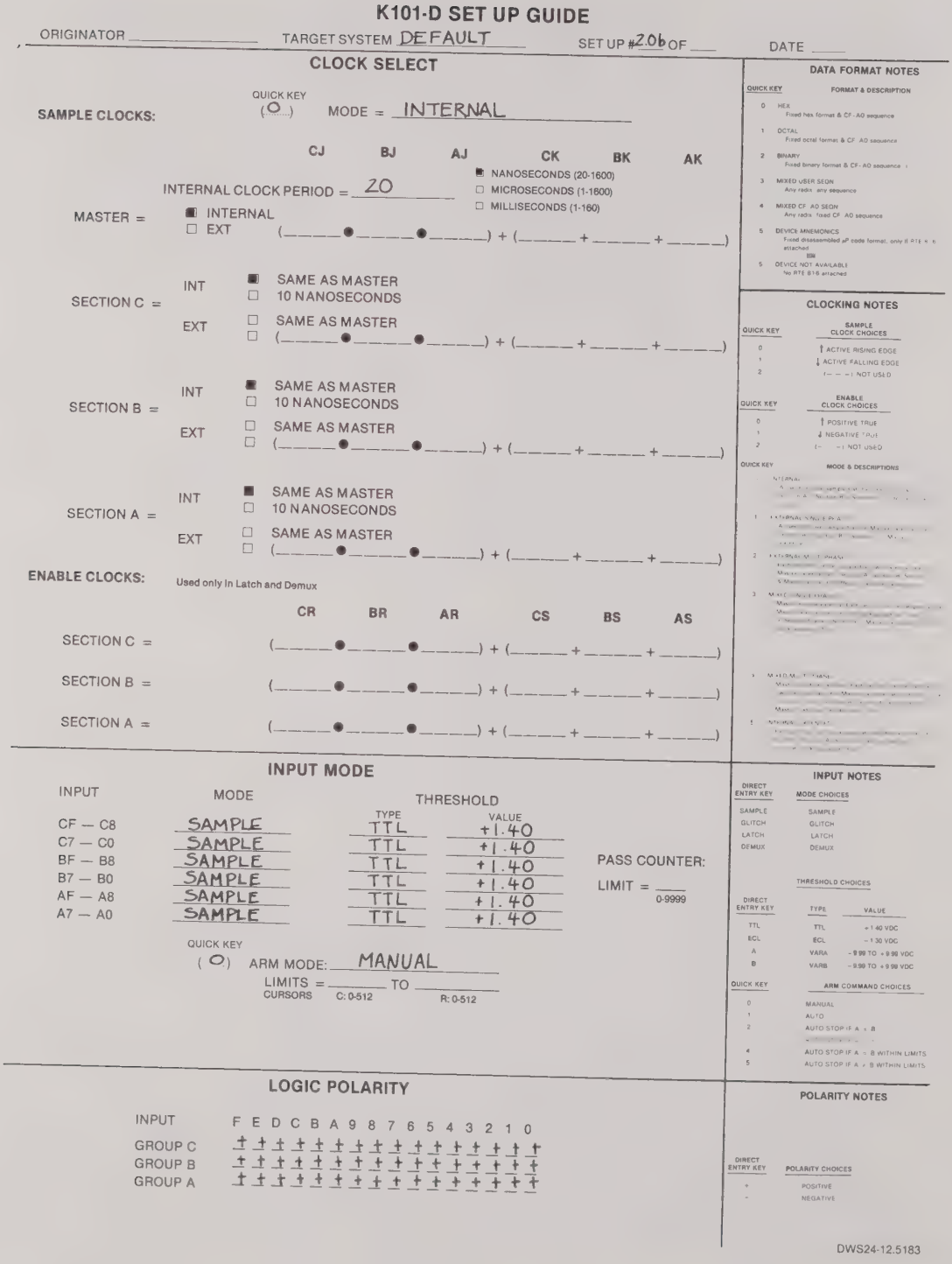
(.....) STOP _____
S = _____

(.....) JUMP TO ___ O F _____
J = _____

(.....) ADVANCE _____
A = _____

(.....) TRACE _____
T = _____

Figure 14-7. "Shorthand" Version of Default Setup (Sheet 1 of 2).



K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM DEFAULT SET UP #20b OF ___ DATE ___

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (0) MODE = INTERNAL

	CJ	BJ	AJ	CK	BK	AK
INTERNAL CLOCK PERIOD = 20				■ NANOSECONDS (20-1600) □ MICROSECONDS (1-1600) □ MILLISECONDS (1-160)		

MASTER = ■ INTERNAL □ EXT (_____●_____●_____) + (_____+_____+_____)

SECTION C = INT ■ SAME AS MASTER □ 10 NANOSECONDS; EXT □ SAME AS MASTER □ (_____●_____●_____) + (_____+_____+_____)

SECTION B = INT ■ SAME AS MASTER □ 10 NANOSECONDS; EXT □ SAME AS MASTER □ (_____●_____●_____) + (_____+_____+_____)

SECTION A = INT ■ SAME AS MASTER □ 10 NANOSECONDS; EXT □ SAME AS MASTER □ (_____●_____●_____) + (_____+_____+_____)

ENABLE CLOCKS: Used only in Latch and Demux

	CR	BR	AR	CS	BS	AS
SECTION C =	(_____●_____●_____) + (_____+_____+_____)					
SECTION B =	(_____●_____●_____) + (_____+_____+_____)					
SECTION A =	(_____●_____●_____) + (_____+_____+_____)					

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX — Fixed hex format & CF-A0 sequence
1	OCTAL — Fixed octal format & CF-A0 sequence
2	BINARY — Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN — Any radix any sequence
4	MIXED CF-A0 SEQN — Any radix fixed CF-A0 sequence
5	DEVICE MNEMONICS — Fixed disassembled µP code format, only if RTE 6/16 attached
5	DEVICE NOT AVAILABLE — No RTE 6/16 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL

1 INTERNAL SINGLE PHASE

2 INTERNAL MULTI PHASE

3 MASTER/SLAVE

4 MASTER/SLAVE

5 MASTER/SLAVE

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8	SAMPLE	TTL	+1.40
C7 — C0	SAMPLE	TTL	+1.40
BF — B8	SAMPLE	TTL	+1.40
B7 — B0	SAMPLE	TTL	+1.40
AF — A8	SAMPLE	TTL	+1.40
A7 — A0	SAMPLE	TTL	+1.40

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ (CURSORS C: 0-512, R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
GROUP B	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
GROUP A	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 14-7. "Shorthand" Version of Default Setup (Sheet 2 of 2).

mode should be Sample or Glitch and the arm mode Manual. Positive logic should be used. The most important signals to observe in the data domain are the four output bits. Therefore, display them as individual bits and as a single hex character for easier recognition of the "decimal" output. The CLEAR signal is included in the format only to serve as a trigger bit. To recreate the previously illustrated timing diagram, the trace control program needs to record what happens after the CLEAR signal. The simple two-level program shown in Figure 14-8 will do that.

14.3.3 8085A SETUP

Refer back to the input connection example shown in Figure 14-5. The DATA, ADDRESS, and CONTROL signals should be sampled synchronously with the 8085A clock output (see Figure 14-9). A comprehensive master sample should then be taken by the ANDed combination of the three control lines READ, WRITE, and INTA. Since the data and low order address bits are multiplexed, inputs A7 through A0 need to be in Demux mode; ALE is used to enable the Demux latching. A TTL threshold level is required and arming should be manual. Polarity is all positive. For the data format it is most logical to group the address, then data, and then status bits. Remember that even though inputs AF through A8 are not connected, they contain the low order address bits latched and sampled off of inputs A7 through A0. For the first run, the trace control program should simply fill memory from anywhere in the program stream.

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM DECADE COUNTER SET UP # 2.1 OF ___ DATE _____

QUICK KEY (See back for notes) (3.) DATA FORMAT MIXED USER SEQN.

RADIX: B B B B H B

MSB	
I 6	
D N 5	
A P 4	
T U 3	A2
A T 2	A3
S 1	A4
LSB	A2 A3 A4 A5 A5 AD

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

TRACE CONTROL

QUICK KEY LEVEL 0 (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(2.) STOP NEVER

S = _____

(2.) JUMP TO 0 (O-F) NEVER

J = _____

(0.) ADVANCE IF DATA = A

A = X X X X X 1

(1.) TRACE ALWAYS

T = _____

COMMENTS

ADVANCE ON CLEAR PULSE.

QUICK KEY LEVEL 1 (O-F) DELAY = DEC (DEC/HEX) 500 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(3.) STOP IF DATA = 5 AND SAMPLE COUNT > DELAY

S = X X X X X X

(2.) JUMP TO 0 (O-F) NEVER

J = _____

(2.) ADVANCE NEVER

A = _____

(1.) TRACE ALWAYS

T = _____

COMMENTS

FILL MEMORY AND STOP.

QUICK KEY LEVEL ___ (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP _____

S = _____

(.....) JUMP TO ___ (O-F) _____

J = _____

(.....) ADVANCE _____

A = _____

(. .) TRACE _____

T = _____

COMMENTS

QUICK KEY LEVEL ___ (O-F) DELAY = ____ (DEC/HEX) ____ (0-65 K) ____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.) STOP _____

S = _____

(. .) JUMP TO ___ (O-F) _____

J = _____

(.....) ADVANCE _____

A = _____

(.) TRACE _____

T = _____

COMMENTS

Figure 14-8. Decade Counter Setup (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM DECADE COUNTER SET UP # 2.1 OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (0) MODE = INTERNAL

	CJ	BJ	AJ	CK	BK	AK
INTERNAL CLOCK PERIOD = 20				■ NANOSECONDS (20-1600) □ MICROSECONDS (1-1600) □ MILLISECONDS (1-160)		
MASTER = ■ INTERNAL □ EXT	(_____●_____●_____) + (_____ + _____ + _____)					
SECTION C = INT □ SAME AS MASTER □ 10 NANOSECONDS						
EXT □ SAME AS MASTER □ (_____●_____●_____) + (_____ + _____ + _____)						
SECTION B = INT □ SAME AS MASTER □ 10 NANOSECONDS						
EXT □ SAME AS MASTER □ (_____●_____●_____) + (_____ + _____ + _____)						
SECTION A = INT ■ SAME AS MASTER □ 10 NANOSECONDS						
EXT □ SAME AS MASTER □ (_____●_____●_____) + (_____ + _____ + _____)						

ENABLE CLOCKS: Used only in Latch and Demux

	CR	BR	AR	CS	BS	AS
SECTION C =	(_____●_____●_____) + (_____ + _____ + _____)					
SECTION B =	(_____●_____●_____) + (_____ + _____ + _____)					
SECTION A =	(_____●_____●_____) + (_____ + _____ + _____)					

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF AO sequence
1	OCTAL Fixed octal format & CF AO sequence
2	BINARY Fixed binary format & CF AO sequence
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF-AO SEQN Any radix fixed CF-AO sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE 816 attached OR
5	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— —) NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL

1 EXTERNAL SINGLE PHASED

2 EXTERNAL MULTI PHASED

3 MIXED SINGLE PHASE

4 MIXED MULTI PHASE

5 INTERNAL LATCH ENABLE

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8	SAMPLE	TTL	+1.40
A7 — A0	SAMPLE	TTL	+1.40

PASS COUNTER: LIMIT = ____ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ (CURSORS C: 0-512, R: 0-512)

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	−1.30 VDC
A	VARA	−9.99 TO +9.99 VDC
B	VARB	−9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP B	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GROUP A	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
	NEGATIVE

DWS24-12.5183

Figure 14-8. Decade Counter Setup (Sheet 2 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM 8085A SET UP # 2.2 OF ___ DATE _____

QUICK KEY (See back for notes) (3) **DATA FORMAT** MIXED USER SEQN.

RADIX: H H H H H H O

MSB								
	6							
D	5							
A	4							
T	3	B7	B3	AE	A8	A7	A3	
A	2	B6	B2	AD	AA	A6	A2	BA
S	1	B5	B1	AC	A9	A5	A1	B9
LSB		B4	B0	AB	A4	A0		B8

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

Format Notes:
TRACE is independent of Analyzer connection
STOP has priority over JUMP
JUMP has priority over ADVANCE
At most one of these conditions can be true on any one machine cycle
Quick Key Command Definition

0	DATA D
1	ALWAYS
2	NEVER
3	If DATA = D and Sample Count > Delay
4	If DATA = D and Sample Count = Delay
5	If DATA = D and Sample Count < Delay
6	If DATA = D or Sample Count > Delay
7	If DATA = D and Sample Count > Delay
8	If DATA = D and Sample Count = Delay

ID = S J A or T which are assigned by command type.

TRACE CONTROL

QUICK KEY LEVEL 0 (O-F) DELAY = DEC (DEC/HEX) 515 (0-65 K) CLOCKS (CLOCKS/A PATTERNS) END LEVEL F (O-F)

(3) STOP IF DATA = S AND SAMPLE COUNT > DELAY

S = X X X X X X X

(2) JUMP TO 0 (O-F) NEVER

J =

(2) ADVANCE NEVER

A =

(1) TRACE ALWAYS

T =

COMMENTS: FILL MEMORY AND STOP.

QUICK KEY LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP

S =

(.....) JUMP TO ___ (O F)

J =

(.....) ADVANCE

A =

(.....) TRACE

T =

COMMENTS

QUICK KEY LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP

S =

(.....) JUMP TO ___ (O F)

J =

(.....) ADVANCE

A =

(.....) TRACE

T =

COMMENTS

QUICK KEY LEVEL ___ (O-F) DELAY = ___ (DEC/HEX) ___ (0-65 K) ___ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP

S =

(.....) JUMP TO ___ (O F)

J =

(.....) ADVANCE

A =

(.....) TRACE

T =

COMMENTS

Figure 14-9. 8085A Setup Guide (Sheet 1 of 2).

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM 8085 A SET UP # 2.2 OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (2) MODE = EXT. MULTI-PHASED

INTERNAL CLOCK PERIOD = _____
☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

	CJ	BJ	AJ	CK	BK	AK
MASTER = ☐ INTERNAL ■ EXT	↑	●	↑	●		↑
SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS						
SECTION C = EXT ☐ SAME AS MASTER ☐		●		●		
SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS						
SECTION B = EXT ☐ SAME AS MASTER ■		●		●		↓
SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS						
SECTION A = EXT ☐ SAME AS MASTER ■		●		●		↓

ENABLE CLOCKS: Used only in Latch and Demux

	CR	BR	AR	CS	BS	AS
SECTION C =		●		●		
SECTION B =		●		●		
SECTION A =		●	↑			

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8	SAMPLE	TTL	+1.40
B7 — B0	SAMPLE	TTL	+1.40
AF — A8	DEMUX	TTL	+1.40
A7 — A0	DEMUX	TTL	+1.40

PASS COUNTER: LIMIT = ___ (0-9999)

QUICK KEY (0) ARM MODE: MANUAL

LIMITS = _____ TO _____ (CURSORS C: 0-512 R: 0-512)

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C																
GROUP B	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
GROUP A	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX — Fixed hex format & CF - A0 sequence
1	OCTAL — Fixed octal format & CF - A0 sequence
2	BINARY — Fixed binary format & CF - A0 sequence
3	MIXED USER SEQN — Any radix, any sequence
4	MIXED CF - A0 SEQN — Any radix, fixed CF - A0 sequence
5	DEVICE MNEMONICS — Fixed disassembled µP code format, only if RTE-816 attached OR
5	DEVICE NOT AVAILABLE — No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(— — —) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(— — —) NOT USED

QUICK KEY — MODE & DESCRIPTIONS

0 INTERNAL

1 EXTERNAL - SINGLE PHASED

2 EXTERNAL - MULTI-PHASED

3 MASTER - SINGLE PHASED

4 MIXED M.P. PHASED

5 INTERNAL EXTENDED

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	-1.30 VDC
A	VARA	-9.99 TO +9.99 VDC
B	VARB	-9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
-	NEGATIVE

DWS24-12.5183

Figure 14-9. 8085A Setup Guide (Sheet 2 of 2).

14.4 SUGGESTED CONNECTION FOR POPULAR MICROPROCESSORS

The remainder of this section suggests ways to connect a K101-D to various popular microprocessors. These are by no means the only ways to probe these microprocessors. Especially with a K101-D, you will likely want to probe more and different signals. The following microprocessors are covered:

a. 8080 family (Figure 14-10)
b. 8085 family (Figure 14-11)
c. NSC 800 (Figure 14-12)
d. 8086 (Figure 14-13)
e. 8088 (Figure 14-14)
f. Z80 family (Figure 14-15)
g. 68000 (Figure 14-16)
h. 6502 (Figure 14-17)
i. 6512 (Figure 14-18)
j. 6800/6802 (Figure 14-19)
k. 6809 (Figure 14-20)

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM 8080/8080A/8080A-1/8080A-2 SET UP # ____ OF ____ DATE _____

K101-D			TARGET SYSTEM								
			SECTION C			SECTION B			SECTION A		
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J				18	$\overline{WR}$	8080	17	DBIN	8080
CLK	GRY	K							22	ϕ1	8080
DATA	VIO	F				36	A15	8080			
DATA	BLU	E				39	A14	8080			
DATA	GRN	D				38	A13	8080			
DATA	YEL	C				37	A12	8080			
DATA	ORG	B				40	A11	8080			
DATA	RED	A				1	A10	8080			
DATA	BRN	9				35	A9	8080			
DATA	BLK	8				34	A8	8080			
GND	LT. BRN	GND				2	GND	8080	2	GND	8080
CLK	WHT	R							19	SYNC	8080
CLK	GRY	S									
DATA	VIO	7				33	A7	8080	6	D7	8080
DATA	BLU	6				32	A6	8080	5	D6	8080
DATA	GRN	5				31	A5	8080	4	D5	8080
DATA	YEL	4				30	A4	8080	3	D4	8080
DATA	ORG	3				29	A3	8080	7	D3	8080
DATA	RED	2				27	A2	8080	8	D2	8080
DATA	BRN	1				26	A1	8080	9	D1	8080
DATA	BLK	0				25	A0	8080	10	D0	8080
GND	LT. BRN	GND				2	GND	8080	2	GND	8080

DWS45-12.5183

Figure 14-10. 8080 Family.

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM 8085A/8085A-2 SET UP # ____ OF ____ DATE _____

K101-D			TARGET SYSTEM								
			SECTION C			SECTION B			SECTION A		
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J	11	$\overline{INTA}$	8085A	31	$\overline{WR}$	8085A	32	$\overline{RD}$	8085A
CLK	GRY	K							37	CLK(OUT)	8085A
DATA	VIO	F	37	CLK(OUT)	8085A	6	TRAP	8085A			
DATA	BLU	E	30	ALE	8085A	7	RST 7.5	8085A			
DATA	GRN	D	32	$\overline{RD}$	8085A	8	RST 6.5	8085A			
DATA	YEL	C	31	$\overline{WR}$	8085A	9	RST 5.5	8085A			
DATA	ORG	B	11	$\overline{INTA}$	8085A	10	INTR	8085A			
DATA	RED	A	34	IO/$\overline{M}$	8085A	34	IO/$\overline{M}$	8085A			
DATA	BRN	9	33	S1	8085A	33	S1	8085A			
DATA	BLK	8	29	S0	8085A	29	S0	8085A			
GND	LT. BRN	GND	20	V_{SS}	8085A	20	V_{SS}	8085A	20	V_{SS}	8085A
CLK	WHT	R							30	ALE	8085A
CLK	GRY	S									
DATA	VIO	7				28	A15	8085A	19	AD7	8085A
DATA	BLU	6				27	A14	8085A	18	AD6	8085A
DATA	GRN	5				26	A13	8085A	17	AD5	8085A
DATA	YEL	4				25	A12	8085A	16	AD4	8085A
DATA	ORG	3				24	A11	8085A	15	AD3	8085A
DATA	RED	2				23	A10	8085A	14	AD2	8085A
DATA	BRN	1				22	A9	8085A	13	AD1	8085A
DATA	BLK	0				21	A8	8085A	12	AD0	8085A
GND	LT BRN	GND				20	V_{SS}	8085A	20	V_{SS}	8085A

DWS45-12.5183

Figure 14-11. 8085 Family.

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM NSC 800 SET UP # ____ OF ____ DATE _____

K101-D			TARGET SYSTEM										
			SECTION C			SECTION B			SECTION A				
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J				31	$\overline{WR}$	800	32	$\overline{RD}$	800
CLK	GRY	K							9	CLK	800
DATA	VIO	F				21	$\overline{NMI}$	800			
DATA	BLU	E				24	$\overline{RSTC}$	800			
DATA	GRN	D				23	$\overline{RSTB}$	800			
DATA	YEL	C				22	$\overline{RSTA}$	800			
DATA	ORG	B				25	$\overline{INTR}$	800			
DATA	RED	A				34	IO/$\overline{M}$	800			
DATA	BRN	9				27	S1	800			
DATA	BLK	8				29	S0	800			
GND	LT. BRN	GND				20	GND	800	20	GND	800
CLK	WHT	R									
CLK	GRY	S							30	ALE	800
DATA	VIO	7				8	A15	800	19	AD7	800
DATA	BLU	6				7	A14	800	18	AD6	800
DATA	GRN	5				6	A13	800	17	AD5	800
DATA	YEL	4				5	A12	800	16	AD4	800
DATA	ORG	3				4	A11	800	15	AD3	800
DATA	RED	2				3	A10	800	14	AD2	800
DATA	BRN	1				2	A9	800	13	AD1	800
DATA	BLK	0				1	A8	800	12	AD0	800
GND	LT. BRN	GND				20	GND	800	20	GND	800

DWS45-12.5183

Figure 14-12. NSC 800.

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM 8086/8086-2/8086-4 SET UP # ____ OF ____ DATE _____

K101-D			TARGET SYSTEM								
			SECTION C			SECTION B			SECTION A		
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J	24	$\overline{\text{INTA}}$(QS1)	8086	29	$\overline{\text{WR}}$($\overline{\text{LOCK}}$)	8086	32	$\overline{\text{RD}}$	8086
CLK	GRY	K							19	CLK	8086
DATA	VIO	F	29	$\overline{\text{WR}}$($\overline{\text{LOCK}}$)	8086						
DATA	BLU	E	32	$\overline{\text{RD}}$	8086						
DATA	GRN	D	17	NMI	8086						
DATA	YEL	C	18	INTR	8086						
DATA	ORG	B	35	A19/S6	8086						
DATA	RED	A	36	A18/S5	8086						
DATA	BRN	9	37	A17/S4	8086						
DATA	BLK	8	38	A16/S3	8086						
GND	LT. BRN	GND	20	GND	8086	20	GND	8086	20	GND	8086
CLK	WHT	R							25	ALE(QS0)	8086
CLK	GRY	S									
DATA	VIO	7	28	IO/$\overline{\text{M}}$($\overline{\text{S2}}$)	8086	39	AD15	8086	9	AD7	8086
DATA	BLU	6	27	DT/$\overline{\text{R}}$($\overline{\text{S1}}$)	8086	2	AD14	8086	10	AD6	8086
DATA	GRN	5				3	AD13	8086	11	AD5	8086
DATA	YEL	4	34	$\overline{\text{BHE}}$/S7	8086	4	AD12	8086	12	AD4	8086
DATA	ORG	3	35	A19/S6	8086	5	AD11	8086	13	AD3	8086
DATA	RED	2	36	A18/S5	8086	6	AD10	8086	14	AD2	8086
DATA	BRN	1	37	A17/S4	8086	7	AD9	8086	15	AD1	8086
DATA	BLK	0	38	A16/S3	8086	8	AD8	8086	16	AD0	8086
GND	LT BRN	GND	20	GND	8086	20	GND	8086	20	GND	8086

DWS45-12.5183

Figure 14-13. 8086.

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM 8088 SET UP # ____ OF ____ DATE _____

K101-D			TARGET SYSTEM								
			SECTION C			SECTION B			SECTION A		
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J	24	$\overline{INTA}$(QS1)	8088	29	$\overline{WR}$($\overline{LOCK}$)	8088	32	$\overline{RD}$	8088
CLK	GRY	K							19	CLK	8088
DATA	VIO	F	29	$\overline{WR}$($\overline{LOCK}$)	8088						
DATA	BLU	E	32	$\overline{RD}$	8088						
DATA	GRN	D	17	NMI	8088						
DATA	YEL	C	18	INTR	8088						
DATA	ORG	B	35	A19/S6	8088						
DATA	RED	A	36	A18/S5	8088						
DATA	BRN	9	37	A17/S4	8088						
DATA	BLK	8	38	A16/S3	8088						
GND	LT. BRN	GND	20	GND	8088	20	GND	8088	20	GND	8088
CLK	WHT	R							25	ALE(QS0)	8088
CLK	GRY	S									
DATA	VIO	7	28	IO/$\overline{M}$($\overline{S2}$)	8088	39	A15	8088	9	AD7	8088
DATA	BLU	6	27	DT/$\overline{R}$($\overline{S1}$)	8088	2	A14	8088	10	AD6	8088
DATA	GRN	5				3	A13	8088	11	AD5	8088
DATA	YEL	4	34	$\overline{SSO}$(HIGH)	8088	4	A12	8088	12	AD4	8088
DATA	ORG	3	35	A19/S6	8088	5	A11	8088	13	AD3	8088
DATA	RED	2	36	A18/S5	8088	6	A10	8088	14	AD2	8088
DATA	BRN	1	37	A17/S4	8088	7	A9	8088	15	AD1	8088
DATA	BLK	0	38	A16/S3	8088	8	A8	8088	16	AD0	8088
GND	LT BRN	GND	20	GND	8088	20	GND	8088	20	GND	8088

DWS45-12.5183

Figure 14-14. 8088.

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM Z80/Z80A/Z80B SET UP # ____ OF ____ DATE _____

K101-D			TARGET SYSTEM								
			SECTION C			SECTION B			SECTION A		
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J	20	$\overline{IORQ}$	Z80	22	$\overline{WR}$	Z80	21	$\overline{RD}$	Z80
CLK	GRY	K							6	ϕ	Z80
DATA	VIO	F				17	$\overline{NMI}$	Z80	37	A7	Z80
DATA	BLU	E				16	$\overline{INT}$	Z80	36	A6	Z80
DATA	GRN	D				24	$\overline{WAIT}$	Z80	35	A5	Z80
DATA	YEL	C				18	$\overline{HALT}$	Z80	34	A4	Z80
DATA	ORG	B				27	$\overline{M1}$	Z80	33	A3	Z80
DATA	RED	A				19	$\overline{MREQ}$	Z80	32	A2	Z80
DATA	BRN	9				20	$\overline{IORQ}$	Z80	31	A1	Z80
DATA	BLK	8				27	$\overline{M1}$	Z80	30	A0	Z80
GND	LT. BRN	GND				29	GND	Z80	29	GND	Z80
CLK	WHT	R									
CLK	GRY	S									
DATA	VIO	7				5	A15	Z80	13	D7	Z80
DATA	BLU	6				4	A14	Z80	10	D6	Z80
DATA	GRN	5				3	A13	Z80	9	D5	Z80
DATA	YEL	4				2	A12	Z80	7	D4	Z80
DATA	ORG	3				1	A11	Z80	8	D3	Z80
DATA	RED	2				40	A10	Z80	12	D2	Z80
DATA	BRN	1				39	A9	Z80	15	D1	Z80
DATA	BLK	0				38	A8	Z80	14	D0	Z80
GND	LT. BRN	GND				29	GND	Z80	29	GND	Z80

DWS45-12.5183

Figure 14-15. Z80 Family.

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM 68000 SET UP # ____ OF ____ DATE ____

K101-D			TARGET SYSTEM										
			SECTION C			SECTION B			SECTION A				
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J				10	DTACK	68000	6	AS	68000
CLK	GRY	K							15	CLK	68000
DATA	VIO	F	7	UDS	68000	44	A16	68000	54	D15	68000
DATA	BLU	E	8	LDS	68000	43	A15	68000	55	D14	68000
DATA	GRN	D	9	R/W	68000	42	A14	68000	56	D13	68000
DATA	YEL	C	23	IPL2	68000	41	A13	68000	57	D12	68000
DATA	ORG	B	24	IPL1	68000	40	A12	68000	58	D11	68000
DATA	RED	A	25	IPL0	68000	39	A11	68000	59	D10	68000
DATA	BRN	9	26	FC2	68000	38	A10	68000	60	D9	68000
DATA	BLK	8	27	FC1	68000	37	A9	68000	61	D8	68000
GND	LT BRN	GND	49	GND	68000	49	GND	68000	16	GND	68000
CLK	WHT	R									
CLK	GRY	S									
DATA	VIO	7	28	FC0	68000	36	A8	68000	62	D7	68000
DATA	BLU	6	52	A23	68000	35	A7	68000	63	D6	68000
DATA	GRN	5	51	A22	68000	34	A6	68000	64	D5	68000
DATA	YEL	4	50	A21	68000	33	A5	68000	1	D4	68000
DATA	ORG	3	48	A20	68000	32	A4	68000	2	D3	68000
DATA	RED	2	47	A19	68000	31	A3	68000	3	D2	68000
DATA	BRN	1	46	A18	68000	30	A2	68000	4	D1	68000
DATA	BLK	0	45	A17	68000	29	A1	68000	5	D0	68000
GND	LT BRN	GND	49	GND	68000	49	GND	68000	16	GND	68000

DWS45-12.5183

Figure 14-16. 68000.

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM 6502 _____ SET UP # ____ OF ____ DATE _____

K101-D			TARGET SYSTEM								
			SECTION C			SECTION B			SECTION A		
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J				3	ϕ1	6502			
CLK	GRY	K				39	ϕ2	6502			
DATA	VIO	F				2	RDY	6502	25	AB15	6502
DATA	BLU	E				4	$\overline{IRQ}$	6502	24	AB14	6502
DATA	GRN	D				6	$\overline{NMI}$	6502	23	AB13	6502
DATA	YEL	C				7	SYNC	6502	22	AB12	6502
DATA	ORG	B				34	R/$\overline{W}$	6502	20	AB11	6502
DATA	RED	A				38	S0	6502	19	AB10	6502
DATA	BRN	9							18	AB9	6502
DATA	BLK	8							17	AB8	6502
GND	LT BRN	GND				1	V_{SS}	6502	21	V_{SS}	6502
CLK	WHT	R									
CLK	GRY	S									
DATA	VIO	7				33	DB0	6502	16	AB7	6502
DATA	BLU	6				32	DB1	6502	15	AB6	6502
DATA	GRN	5				31	DB2	6502	14	AB5	6502
DATA	YEL	4				30	DB3	6502	13	AB4	6502
DATA	ORG	3				29	DB4	6502	12	AB3	6502
DATA	RED	2				28	DB5	6502	11	AB2	6502
DATA	BRN	1				27	DB6	6502	10	AB1	6502
DATA	BLK	0				26	DB7	6502	9	AB0	6502
GND	LT BRN	GND				1	V_{SS}	6502	21	V_{SS}	6502

DWS45-12.5183

Figure 14-17. 6502.

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM 6512 SET UP # ____ OF ____ DATE _____

K101-D			TARGET SYSTEM								
			SECTION C			SECTION B			SECTION A		
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J				39	ϕ2(OUT)	6512			
CLK	GRY	K									
DATA	VIO	F				2	RDY	6512	25	AB15	6512
DATA	BLU	E				4	$\overline{IRQ}$	6512	24	AB14	6512
DATA	GRN	D				6	$\overline{NMI}$	6512	23	AB13	6512
DATA	YEL	C				7	SYNC	6512	22	AB12	6512
DATA	ORG	B				34	R/$\overline{W}$	6512	20	AB11	6512
DATA	RED	A				36	DBE	6512	19	AB10	6512
DATA	BRN	9				38	SO	6512	18	AB9	6512
DATA	BLK	8							17	AB8	6512
GND	LT. BRN	GND				1	V_{SS}	6512	21	V_{SS}	6512
CLK	WHT	R									
CLK	GRY	S									
DATA	VIO	7				33	DB0	6512	16	AB7	6512
DATA	BLU	6				32	DB1	6512	15	AB6	6512
DATA	GRN	5				31	DB2	6512	14	AB5	6512
DATA	YEL	4				30	DB3	6512	13	AB4	6512
DATA	ORG	3				29	DB4	6512	12	AB3	6512
DATA	RED	2				28	DB5	6512	11	AB2	6512
DATA	BRN	1				27	DB6	6512	10	AB1	6512
DATA	BLK	0				26	DB7	6512	9	AB0	6512
GND	LT BRN	GND				1	V_{SS}	6512	21	V_{SS}	6512

DWS45-12.5183

Figure 14-18. 6512.

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM 6800/6802 SET UP # ____ OF ____ DATE _____

K101-D			TARGET SYSTEM								
			SECTION C			SECTION B			SECTION A		
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J									
CLK	GRY	K				3	ϕ01(MR)	6800			
DATA	VIO	F				37	ϕ2(E)	6800			
DATA	BLU	E				4	$\overline{IRQ}$	6800	25	A15	6800
DATA	GRN	D				5	VMA	6800	24	A14	6800
DATA	YEL	C				6	$\overline{NMI}$	6800	23	A13	6800
DATA	ORG	B				39	TSC	6800	22	A12	6800
DATA	RED	A				36	DBE(RE)	6800	20	A11	6800
DATA	BRN	9				34	R/$\overline{W}$	6800	19	A10	6800
DATA	BLK	8							18	A9	6800
GND	LT BRN	GND							17	A8	6800
						1	V_{SS}	6800	21	V	
CLK	WHT	R									
CLK	GRY	S									
DATA	VIO	7				33	D0	6800	16	A7	6800
DATA	BLU	6				32	D1	6800	15	A6	6800
DATA	GRN	5				31	D2	6800	14	A5	6800
DATA	YEL	4				30	D3	6800	13	A4	6800
DATA	ORG	3				29	D4	6800	12	A3	6800
DATA	RED	2				28	D5	6800	11	A2	6800
DATA	BRN	1				27	D6	6800	10	A1	6800
DATA	BLK	0				26	D7	6800	9	A0	6800
GND	LT BRN	GND				1	V_{SS}	6800	21	V_{SS}	6800

NOTE: In the 6802, three signals at pins #3, 37, and 36 are different from the 6800. The three signals for the 6802 are given in brackets. All other signals are the same for both the 6800 and 6802.

DWS45-12.5183

Figure 14-19. 6800/6802.

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM 6809 SET UP # ____ OF ____ DATE _____

K101-D			TARGET SYSTEM								
			SECTION C			SECTION B			SECTION A		
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J				35	Q	6809	34	E	6809
CLK	GRY	K									
DATA	VIO	F							23	A15	6809
DATA	BLU	E				2	$\overline{NMI}$	6809	22	A14	6809
DATA	GRN	D				3	$\overline{IRQ}$	6809	21	A13	6809
DATA	YEL	C				4	$\overline{FIRQ}$	6809	20	A12	6809
DATA	ORG	B				5	BS	6809	19	A11	6809
DATA	RED	A				6	BA	6809	18	A10	6809
DATA	BRN	9				32	R/$\overline{W}$	6809	17	A9	6809
DATA	BLK	8				33	$\overline{DMA/BREQ}$	6809	16	A8	6809
GND	LT. BRN	GND				1	V_{SS}	6809	1	V_{SS}	6809
CLK	WHT	R									
CLK	GRY	S									
DATA	VIO	7				24	D7	6809	15	A7	6809
DATA	BLU	6				25	D6	6809	14	A6	6809
DATA	GRN	5				26	D5	6809	13	A5	6809
DATA	YEL	4				27	D4	6809	12	A4	6809
DATA	ORG	3				28	D3	6809	11	A3	6809
DATA	RED	2				29	D2	6809	10	A2	6809
DATA	BRN	1				30	D1	6809	9	A1	6809
DATA	BLK	0				31	D0	6809	8	A0	6809
GND	LT. BRN	GND				1	V_{SS}	6809	1	V_{SS}	6809

DWS45-12.5183

Figure 14-20. 6809.

K101-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # _____ OF _____ DATE _____

K101-D			TARGET SYSTEM								
			SECTION C			SECTION B			SECTION A		
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	J									
CLK	GRY	K									
DATA	VIO	F									
DATA	BLU	E									
DATA	GRN	D									
DATA	YEL	C									
DATA	ORG	B									
DATA	RED	A									
DATA	BRN	9									
DATA	BLK	8									
GND	LT. BRN	GND									
CLK	WHT	R									
CLK	GRY	S									
DATA	VIO	7									
DATA	BLU	6									
DATA	GRN	5									
DATA	YEL	4									
DATA	ORG	3									
DATA	RED	2									
DATA	BRN	1									
DATA	BLK	0									
GND	LT. BRN	GND									

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

DATA FORMAT

QUICK KEY (See back for notes) (.....)

RADIX: _____

MSB _____
I 6 _____
D N 5 _____
A P 4 _____
T U 3 _____
A T 2 _____
S 1 _____
LSB _____

RADIX CHOICES: (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level:
TRACE is independent of the other commands
STOP has priority over JUMP
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count > Delay
4	If DATA = D and Sample Count < Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count ≥ Delay
7	If DATA = D and Sample Count ≤ Delay
8	If DATA = D and Sample Count ≠ Delay

(D = S, J, A, or T, which are assigned by command type.)

TRACE CONTROL

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP _____
S = _____
(.....) JUMP TO ___ (O-F) _____
J = _____
(.....) ADVANCE _____
A = _____
(.....) TRACE _____
T = _____

COMMENTS

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP _____
S = _____
(.....) JUMP TO ___ (O-F) _____
J = _____
(.....) ADVANCE _____
A = _____
(.....) TRACE _____
T = _____

COMMENTS

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP _____
S = _____
(.....) JUMP TO ___ (O-F) _____
J = _____
(.....) ADVANCE _____
A = _____
(.....) TRACE _____
T = _____

COMMENTS

LEVEL ___ (O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP _____
S = _____
(.....) JUMP TO ___ (O-F) _____
J = _____
(.....) ADVANCE _____
A = _____
(.....) TRACE _____
T = _____

COMMENTS

K101-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (.....) MODE = _____

	CJ	BJ	AJ	CK	BK	AK

☐ NANOSECONDS (20-1600)
☐ MICROSECONDS (1-1600)
☐ MILLISECONDS (1-160)

INTERNAL CLOCK PERIOD = _____

MASTER = ☐ INTERNAL ☐ EXT (_____●_____●_____) + (_____ + _____ + _____)

SECTION C = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = INT ☐ SAME AS MASTER ☐ 10 NANOSECONDS
EXT ☐ SAME AS MASTER ☐ (_____●_____●_____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

	CR	BR	AR	CS	BS	AS

SECTION C = (_____●_____●_____) + (_____ + _____ + _____)

SECTION B = (_____●_____●_____) + (_____ + _____ + _____)

SECTION A = (_____●_____●_____) + (_____ + _____ + _____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & CF-A0 sequence
1	OCTAL Fixed octal format & CF-A0 sequence
2	BINARY Fixed binary format & CF-A0 sequence
3	MIXED USER SEQN Any radix, any sequence
4	MIXED CF-A0 SEQN Any radix, fixed CF-A0 sequence.
5	DEVICE MNEMONICS Fixed disassembled μP code format, only if RTE-816 attached OR
5	DEVICE NOT AVAILABLE No RTE-816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	(– – –) NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
2	(– – –) NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the Internal clock rate Section A = Section B = Section C = Internal clock period
1	EXTERNAL SINGLE PHASED All sections are sampled at the Master external rate Section A = Section B = Section C = Master (external)
2	EXTERNAL MULTI-PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, Section C & Master all can be different external expressions
3	MIXED SINGLE PHASED Master must be external. Each section can be sampled at the Master external rate, Internal clock period, or 10ns. Section A, Section B, and/or Section C = Master (external) or Internal clock period or 10ns
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, Internal clock period, or 10ns. Section A, Section B, and/or Section C = Master (external) or Internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the Internal clock rate or 10ns. Section A, Section B, and or Section C = Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
CF — C8			
C7 — C0			
BF — B8			
B7 — B0			
AF — A8			
A7 — A0			

PASS COUNTER: LIMIT = ___ 0-9999

QUICK KEY (.....) ARM MODE: _____

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	–1.30 VDC
A	VARA	–9.99 TO +9.99 VDC
B	VARB	–9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
1	AUTO
2	AUTO STOP IF A = B
3	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP C	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP B	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
GROUP A	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
+	POSITIVE
–	NEGATIVE

K102-D INPUT CONNECTION GUIDE

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ____ OF ____ DATE _____

K102-D		TARGET SYSTEM							
		SECTION B				SECTION A			
TYPE	COLOR	INPUT	DESIGNATION/ PIN #	SIGNAL	IC	INPUT	DESIGNATION/ PIN #	SIGNAL	IC
CLK	WHT	BJ				AJ			
CLK	GRY	BK				AK			
DATA	VIO	BF				AF			
DATA	BLU	BE				AE			
DATA	GRN	BD				AD			
DATA	YEL	BC				AC			
DATA	ORG	BB				AB			
DATA	RED	BA				AA			
DATA	BRN	B9				A9			
DATA	BLK	B8				A8			
GND	LT. BRN	GND				GND			
CLK	WHT	CJ				AR			
CLK	GRY	CK				AS			
DATA	VIO	B7				A7			
DATA	BLU	B6				A6			
DATA	GRN	B5				A5			
DATA	YEL	B4				A4			
DATA	ORG	B3				A3			
DATA	RED	B2				A2			
DATA	BRN	B1				A1			
DATA	BLK	B0				A0			
GND	LT. BRN	GND				GND			

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

DATA FORMAT

QUICK KEY (See back for notes) (.)

RADIX: _____

	MSB	_____
	I	6 _____
D	N	5 _____
A	P	4 _____
T	U	3 _____
A	T	2 _____
	S	1 _____
	LSB	_____

RADIX CHOICES (B) BINARY, (O) OCTAL, (H) HEX, (A) ASCII, or (E) EBCDIC

TRACE CONTROL NOTES

For each level —
TRACE is independent of the other commands
STOP has priority over JUMP.
JUMP has priority over ADVANCE
All four major commands in each level can come true on any of nine conditions.

Quick Key	Command Condition
0	If DATA = D
1	Always
2	Never
3	If DATA = D and Sample Count > Delay
4	If DATA = D and Sample Count < Delay
5	If DATA = D and Sample Count = Delay
6	If DATA = D and Sample Count > = Delay
7	If DATA = D and Sample Count < > Delay
8	If DATA = D and Sample Count < = Delay

(D = S, J, A, or T, which are assigned by command type)

TRACE CONTROL

LEVEL ___ (QUICK KEY, O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP _____

S = _____

(.....) JUMP TO ___ (O F) _____

J = _____

(.....) ADVANCE _____

A = _____

(.....) TRACE _____

T = _____

COMMENTS

LEVEL ___ (QUICK KEY, O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP _____

S = _____

(.....) JUMP TO ___ (O F) _____

J = _____

(.....) ADVANCE _____

A = _____

(.....) TRACE _____

T = _____

COMMENTS

LEVEL ___ (QUICK KEY, O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP _____

S = _____

(.....) JUMP TO ___ (O F) _____

J = _____

(.....) ADVANCE _____

A = _____

(.....) TRACE _____

T = _____

COMMENTS

LEVEL ___ (QUICK KEY, O-F) DELAY = _____ (DEC/HEX) ___ (0-65 K) _____ (CLOCKS/A PATTERNS) END LEVEL ___ (O-F)

(.....) STOP _____

S = _____

(.....) JUMP TO ___ (O F) _____

J = _____

(.....) ADVANCE _____

A = _____

(.....) TRACE _____

T = _____

COMMENTS

K102-D SET UP GUIDE

ORIGINATOR _____ TARGET SYSTEM _____ SET UP # ___ OF ___ DATE _____

CLOCK SELECT

SAMPLE CLOCKS: QUICK KEY (.....) MODE = _____

CJ BJ AJ CK BK AK

INTERNAL CLOCK PERIOD = _____
- ☐ NANOSECONDS (20-1600)
- ☐ MICROSECONDS (1-1600)
- ☐ MILLISECONDS (1-160)

MASTER =
- ☐ INTERNAL
- ☐ EXT (_____●_____●_____) + (_____ + _____ + _____)

SECTION B =
- INT
  - ☐ SAME AS MASTER
  - ☐ 10 NANOSECONDS
- EXT
  - ☐ SAME AS MASTER
  - ☐ (_____●_____●_____) + (_____ + _____ + _____)

SECTION A =
- INT
  - ☐ SAME AS MASTER
  - ☐ 10 NANOSECONDS
- EXT
  - ☐ SAME AS MASTER
  - ☐ (_____●_____●_____) + (_____ + _____ + _____)

ENABLE CLOCKS: Used only in Latch and Demux

AR AS

SECTION B = (_____) + (_____)

SECTION A = (_____) + (_____)

DATA FORMAT NOTES

QUICK KEY	FORMAT & DESCRIPTION
0	HEX Fixed hex format & BF AO sequence
1	OCTAL Fixed octal format & BF AO sequence
2	BINARY Fixed binary format & BF-AO sequence
3	MIXED USER SEQN Any radix any sequence
4	MIXED BF AO SEQN Any radix fixed BF AO sequence
5	DEVICE MNEMONICS Fixed disassembled µP code format, only if RTE 816 attached OR
5	DEVICE NOT AVAILABLE No RTE 816 attached

CLOCKING NOTES

QUICK KEY	SAMPLE CLOCK CHOICES
0	↑ ACTIVE RISING EDGE
1	↓ ACTIVE FALLING EDGE
2	⌐ – – ⌐ NOT USED

QUICK KEY	ENABLE CLOCK CHOICES
0	↑ POSITIVE TRUE
1	↓ NEGATIVE TRUE
.	⌐– – ⌐ NOT USED

QUICK KEY	MODE & DESCRIPTIONS
0	INTERNAL All sections are sampled at the Internal clock rate Section A = Section B = Internal clock period
1	EXTERNAL SINGLE-PHASED All sections are sampled at the Master external rate Section A = Section B = Master (external)
2	EXTERNAL MULTI-PHASED Each section can be sampled at own external rate or Master external rate. Section A, Section B, & Master all can be different external expressions
3	MIXED SINGLE-PHASED Master must be external. Each section can be sampled at the Master external rate, Internal clock period, or 10ns. Section A and/or Section B = Master (external) or Internal clock period or 10ns.
4	MIXED MULTI PHASED Master must be external. Each section can be sampled at own external rate, the Master external rate, Internal clock period, or 10ns. Section A and/or Section B = Master (external) or Internal or 10ns
5	INTERNAL EXTENDED Each section can be sampled at the Internal clock rate or 10ns. Section A and/or Section B = Internal clock period or 10ns

INPUT MODE

INPUT	MODE	THRESHOLD TYPE	THRESHOLD VALUE
BF — B8	_____	_____	_____
B7 — B0	_____	_____	_____
AF — A8	_____	_____	_____
A7 — A0	_____	_____	_____

PASS COUNTER: LIMIT = ____ 0-9999

QUICK KEY (.....) ARM MODE: _____

LIMITS = _____ TO _____
CURSORS C: 0-512 R: 0-512

INPUT NOTES

DIRECT ENTRY KEY	MODE CHOICES
SAMPLE	SAMPLE
GLITCH	GLITCH
LATCH	LATCH
DEMUX	DEMUX

THRESHOLD CHOICES

DIRECT ENTRY KEY	TYPE	VALUE
TTL	TTL	+1.40 VDC
ECL	ECL	–1.30 VDC
A	VARA	–9.99 TO +9.99 VDC
B	VARB	–9.99 TO +9.99 VDC

QUICK KEY	ARM COMMAND CHOICES
0	MANUAL
	AUTO
2	AUTO STOP IF A = B
1	AUTO STOP IF A ≠ B
4	AUTO STOP IF A = B WITHIN LIMITS
5	AUTO STOP IF A ≠ B WITHIN LIMITS

LOGIC POLARITY

INPUT	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
GROUP B	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
GROUP A	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_

POLARITY NOTES

DIRECT ENTRY KEY	POLARITY CHOICES
.	POSITIVE
–	NEGATIVE

Section 15

INDEX

ACQUIRE keys, 4-7, 4-19, 9-15

Active Display set, 4-49, 4-50

ADVANCE, 3-18, 3-19, 3-21, 4-15, 4-16, 4-17, 5-46, 5-47, 5-48, 7-19, 10-176

Arm mode, 3-20, 3-21, 5-16, 5-17, 5-18, 6-2, 6-3, 6-4, 6-6, 6-8, 7-22, 10-143

Asynchronous recording, 5-18, 10-150, 10-151

Boolean expression, 2-17, 5-21, 8-13, 8-14

CHOICE keys, 4-8, 4-9, 4-10, 4-25

Clock input, 3-9, 3-10, 3-12, 3-22, 4-2

Clock modes, 3-8, 3-9

Clock Select screen (menu), 4-13, 5-5, 5-18, 5-19, 5-20, 9-30, 9-32, 14-4, 14-10

Clock signals, 10-26

Clocking modes, 2-17, 5-19, 5-30

Data display, 2-9, 2-11, 2-26, 3-2, 3-17, 3-22, 4-58, 7-2, 7-3, 7-5, 7-6, 7-7, 7-11, 8-26, 10-18, 10-22, 10-23, 10-24

DATA ENTRY keys, 4-29, 4-35

Data format, 2-8, 2-16, 3-17, 3-22, 4-11, 4-18, 4-33, 4-63, 5-3, 7-7, 8-22, 8-26, 10-13, 10-19, 10-20, 10-22

DATA FORMAT keys, 4-29, 4-33

Data Format screen (menu), 4-15, 4-16, 4-17, 4-18, 5-5, 5-35, 5-38, 5-40, 5-41, 7-2, 7-6, 9-34, 9-35, 14-10

DELAY, 5-44

Demux (Demultiplex) mode, 2-7, 2-25, 5-12, 5-14, 5-15, 9-20, 9-23

DISPLAY keys, 4-7, 4-20, 7-2, 9-15

EDIT keys, 4-29, 4-34

Enable clock, 3-7, 3-8

Field, 4-6, 4-9

FIELD keys, 4-6, 4-8, 4-10, 7-5, 9-15

GENERAL keys, 4-7, 4-23, 4-24, 7-5

Glitch mode, 2-7, 2-25, 3-5, 5-10, 5-11, 5-14, 5-16, 8-7, 10-167

GPIB keys, 4-7, 4-38

Graph display, 2-26, 3-2, 7-2, 7-3, 7-5, 7-11, 7-13, 7-14

GRAPH keys, 4-29, 4-36

INPUT MODE keys, 4-29, 4-30

Input Mode screen (menu), 4-14, 5-5, 5-7, 5-8, 5-16, 6-1, 6-4, 6-5, 6-6, 9-33

Input signal, 2-7, 2-12, 3-17, 4-17, 5-3, 5-16, 7-14, 7-15, 8-4, 8-5, 8-6

Interface screen (menu), 4-11, 5-5, 7-18, 9-32

JUMP, 3-18, 4-15, 4-16, 4-17, 5-46, 5-47, 5-48, 7-19, 10-176

Latch mode, 2-7, 2-8, 2-25, 3-5, 3-6, 5-12, 5-13, 5-14, 5-16, 8-7, 10-167

LOGIC POLARITY keys, 4-29

Logic Polarity screen (menu), 5-5, 5-6, 5-7, 9-34, 14-10

Probe Test, 1-8, 3-4, 3-26, 4-2, 10-1, 10-2, 10-3, 10-4, 10-5, 10-6, 10-26, 10-139, 10-142

QUICK keys, 4-8, 4-10, 4-25, 4-26, 9-16, 9-17, 9-18, 9-19, 9-21, 9-22

Sample clock, 3-7

Sample mode, 2-7, 2-25, 3-5, 3-6, 5-9, 5-10, 5-14, 5-16, 8-7

Self-Test, 1-8, 3-4, 3-25, 3-26, 9-49, 10-1, 10-161, 10-163, 10-164, 10-179

SPECIFY keys, 4-6, 4-11, 5-5, 9-15

STOP, 3-18, 3-20, 3-21, 4-15, 4-16, 5-46, 5-47, 7-19

Synchronous recording, 5-18

Threshold, 2-5, 2-15, 3-5, 4-14, 5-10, 5-16, 5-17, 10-5, 10-6, 10-9, 10-10, 10-169, 10-170

Timing display, 2-10, 3-2, 3-22, 4-53, 4-56, 7-2, 7-4, 7-5, 7-14, 7-15, 8-9, 10-139, 10-142

TIMING ENTRY keys, 4-29, 4-37

TRACE, 3-18, 3-19, 4-15, 4-16, 4-17, 4-53, 5-46, 5-47, 5-48, 7-19, 8-22

Trace control, 2-8, 2-18, 2-25, 3-17, 3-22, 4-15, 4-16, 4-17, 4-31, 5-2, 5-43, 5-44, 5-45, 5-46, 5-47, 5-48, 5-50, 8-22, 8-23, 8-27, 10-16, 10-72, 10-126, 10-168, 10-174, 10-175

TRACE CONTROL keys, 4-29, 4-31

Trace Control screen (menu), 4-15, 4-17, 5-5, 5-43, 9-33, 9-34, 14-10, 14-11

www.manualsplus.com

1012334

Gould Inc., Design & Test Systems Division
4600 Old Ironsides Drive, Santa Clara, CA 95050-1279
(408) 988-6800 TWX: 910-338-0509

Printed in U.S.A.

GOULD
Electronics